

Design of a Balanced PIN Diode Attenuator at 1900 MHz

Raymond Waugh and Eric Chan, *Agilent Technologies.*

Abstract – This paper discusses the design and performance evaluations of a balanced PIN diode Attenuator at 1900 MHz, targeted for application in PCS band base station transmitter chain. The balanced configuration employed in this design yields an attenuator with high dynamic range, excellent attenuation flatness and low VSWR across the entire attenuation range and PCS frequency band. Details of circuit simulation on ADS, layout considerations and final circuit evaluations and measurements are presented in this paper.

I. INTRODUCTION

ATTENUATOR with variable attenuation is an important building block in a transmitter chain in a cellular base station. Mobile receivers or handsets will normally feedback the down-link signal strength to the base station and requires the base station transmitter to increase its output power when the mobile units are moving away from the base station, to maintain the clarity of the received signal, or to decrease its output power when the mobile units are moving closer to the base station, to prevent overloading on the receivers of the mobile units. In TDMA system where many mobile units are sharing the same down-link frequency but on different time slot, a variable attenuator is mandatory in the base station transmitter chain where the output power has to be controlled dynamically and rapidly, as different time slots allocated to different mobile units could be requesting different power levels from the base station.

A well known and unique characteristics of a PIN diode is its resistance at RF and microwave frequencies can be varied by changing with biasing current. This important characteristics makes PIN diodes very attractive and useful device in designing variable attenuators for RF and microwave applications. Very simple single PIN diode attenuators can be constructed with minimal components are shown below, in figure 1. However, in these simple designs, good impedance match cannot be achieved due to the fact that diode impedance varies significantly with bias. This is not desirable to a filter preceding the attenuator as the poor matching could alter the transmission response of such a filter.

One solution to poor VSWR across the bandwidth of interest is to employ a constant impedance design where the constant impedance characteristics is achieved by

virtue of the coupling elements as shown in figure 2 where the circulator presents a low VSWR load to the

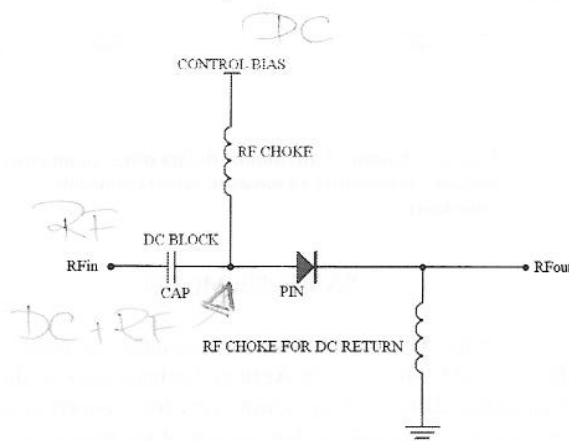


Figure 1. a simple PIN diode attenuator.

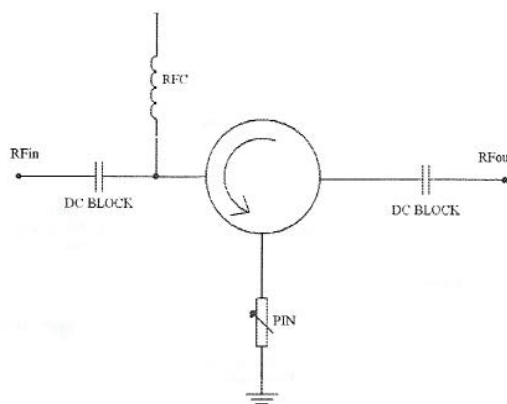


Figure 2. constant impedance PIN diode attenuator using circulator as coupling element.

stage preceding the attenuator. Another constant impedance design with better performance, employing balanced structure with two quadrature couplers as input and output coupling elements is shown in figure 3. By virtue an ideal quadrature coupler, all reflected RF will be channeled to the 50 Ohm termination. Therefore, as long as the load impedances presented to the output ports (0 and 90) are identical and regardless of their actual impedance values, the impedance seen into the input port of the quadrature coupler will be 50 Ohms. The balanced design also provide 3 dB higher IP3 performance than the unbalanced version.

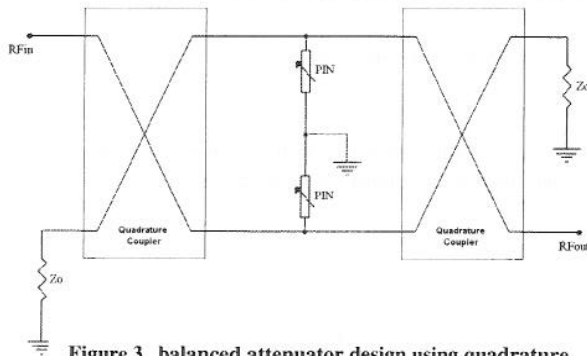


Figure 3. balanced attenuator design using quadrature couplers as coupling elements to achieve constant impedance.

2. PIN DIODE MODEL

In the design of balanced attenuator, we have chosen HSMP-481B from Agilent Technologies as the attenuating elements that exhibit very low distortion and low biasing requirement. Simulation of the balanced attenuator was performed with Agilent's Advanced Design System (ADS) to verify the design and later to

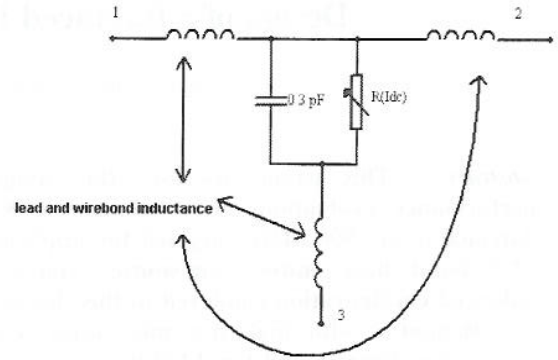


Figure 4. equivalent circuit of a HSMP-481B PIN diode.

optimize circuit parameters to match the attenuator performance required, such as return loss and insertion loss. HSMP-481B was carefully modeled in the simulation and the model is given in figure 4.

Lead inductances of HSMP-481B are taken as 1.5 nH each between cathode and pin 1, 1.5 nH between cathode and pin 2 and 1.0 nH between anode and pin 3. The junction capacitance is 0.3 pF. These values of parasitics

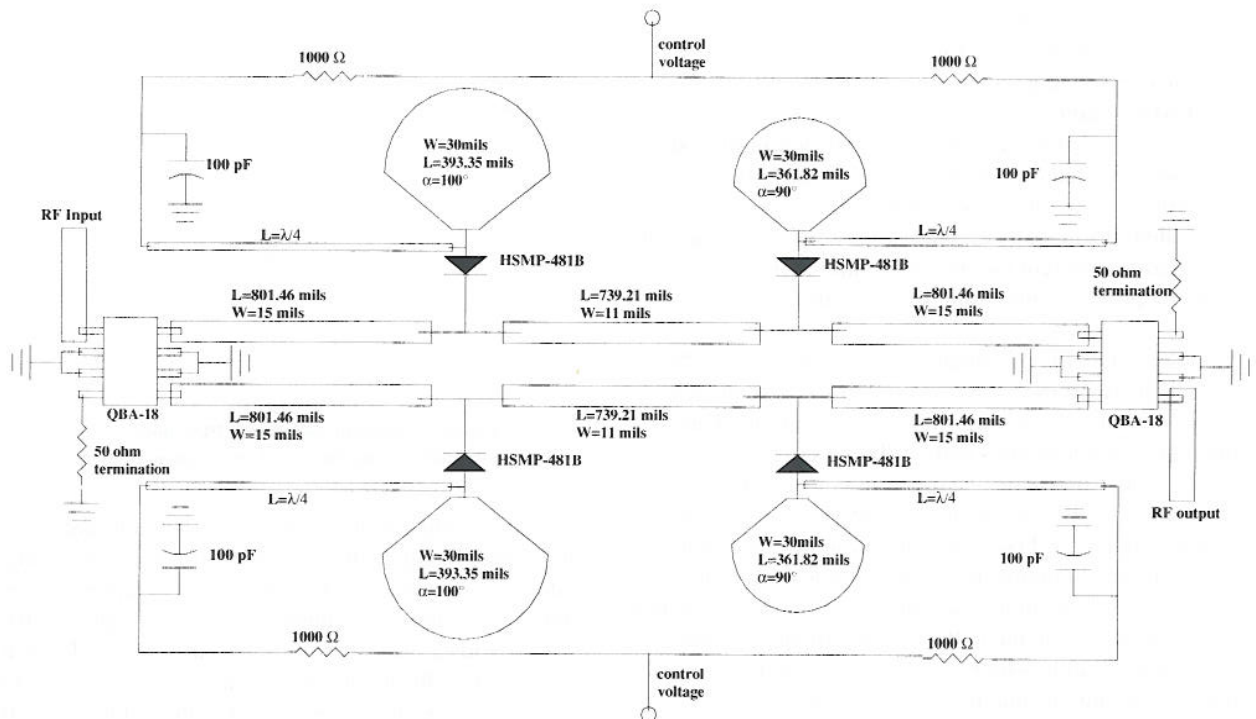


Figure 5. schematic diagram of a 1.9 GHz balanced attenuator using HSMP-481B

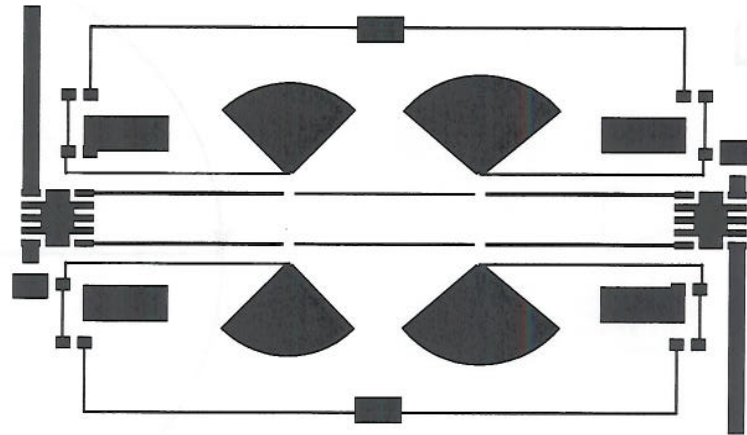


Figure 6. 1.9 GHz Balanced Attenuator PCB layout.

are valid up to at least 3 GHz. At 1.9 GHz, lead inductance has to be taken into consideration during design and in this case, as will be presented in the next section, the lead inductance on all three pins will be absorbed into the circuit.

The current-controlled-characteristics of HSMP-481B is modeled as a current controlled resistor. It is known that the value of resistance should varies from approximately 2000 Ohms, when no bias applied, to about 2 Ohms when high bias, about 20 mA is applied through the PIN.

3. CIRCUIT TOPOLOGY AND SIMULATION

The schematic of a balanced PIN diode attenuator evaluated is shown in figure 5. To achieve high attenuation range (>50 dB), two PINs are used in both upper and lower arms of the attenuator.

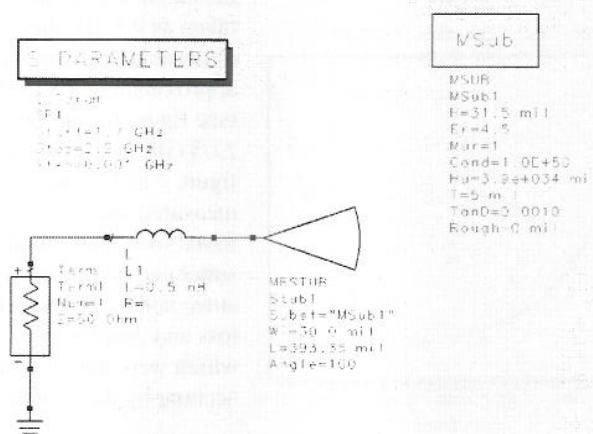


Figure 6a. circuit simulation on left radial stub

Since pin 5 and pin 10 of QBA-18 quadrature coupler are DC connected, the 50 ohm termination can serve as part of DC path providing biasing current to the diodes. The diodes on the upper branch will have the DC returned to ground through pin 10 – pin 5 – 50 ohm termination – ground on left coupler, while the diodes in lower branch will have DC returned to ground through right coupler in a similar manner. This biasing trick eliminates the use of RF choke for ground return which could increase the minimum insertion across frequency band of 1.7 GHz to 2.2 GHz.

The anodes of the PINs are connected to radial stubs instead of RF grounded through capacitors. Together with the lead inductance, the capacitance provided by the radial stub forms a series resonance circuit. The series

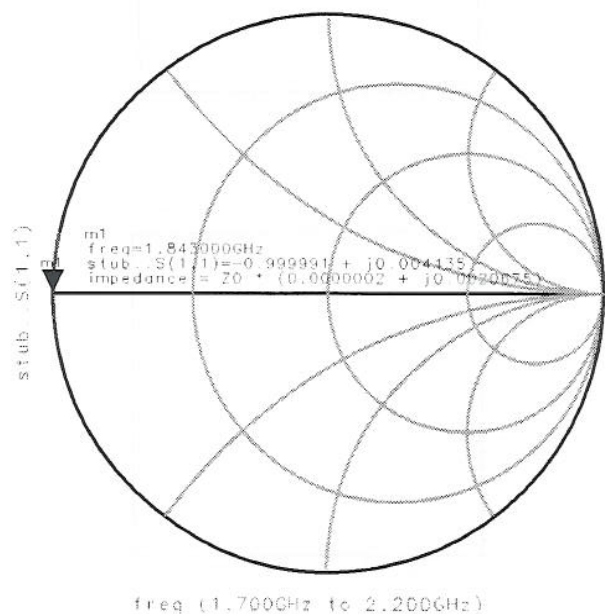


Figure 6b. left radial stub and lead inductance series resonate @ 1.84 GHz

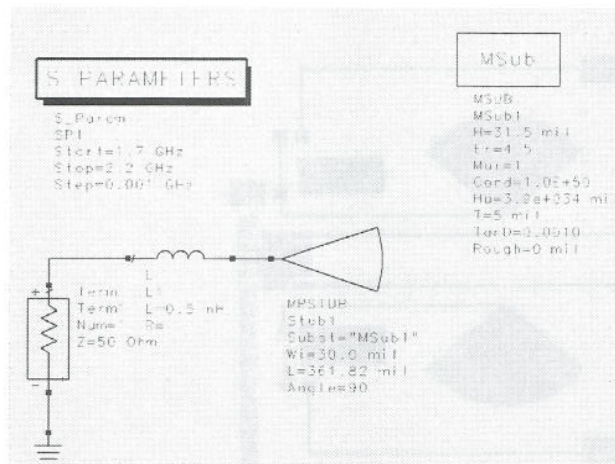


Figure 6c. circuit simulation on right radial stub

resonance will provide a low impedance path connecting the anodes of the diodes to ground. One would expect that the series L-C resonance should occur at center of the desired frequency band, that is 1.9 GHz. While it is true that higher attenuation (at 1.9 GHz) can be achieved with all the radial stubs designed to resonate with the anode lead inductances at band center, simulation reveals that

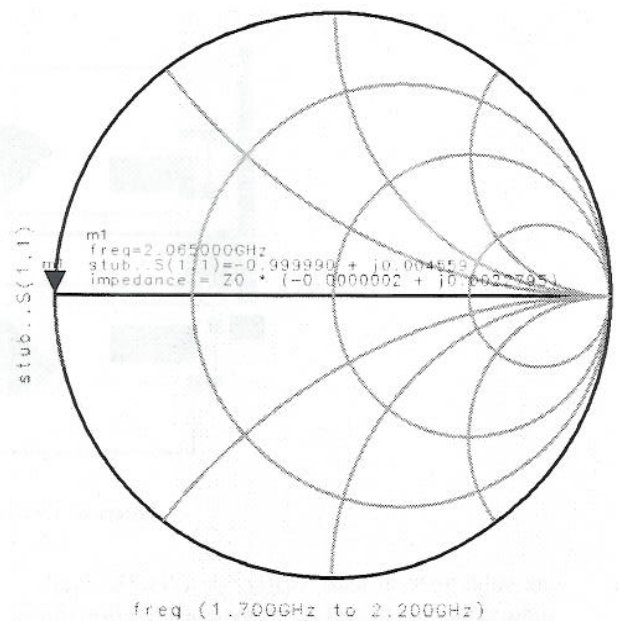


Figure 6d. right radial stub and lead inductance series resonate @ 2.07 GHz

this should not be the case if a flatter attenuation is desired. There is, therefore, a trade off between maximum attenuation and attenuation flatness. This is shown in the simulation results in figure 6. It is observed after the completion of optimization done on ADS, with the attenuation flatness required, dimensions of the left and right radial stubs are somewhat different. With the anode lead inductance taken as 0.5 nH, these stub dimensions correspond to approximately 1.84 GHz (see figure 6a and 6b) and 2.03 GHz as shown in figure 7 and figure 8. The measured insertion loss is found to be more than the simulated values and is attributed to the radiation loss and coupler loss, which were not taken into account by the simulator.

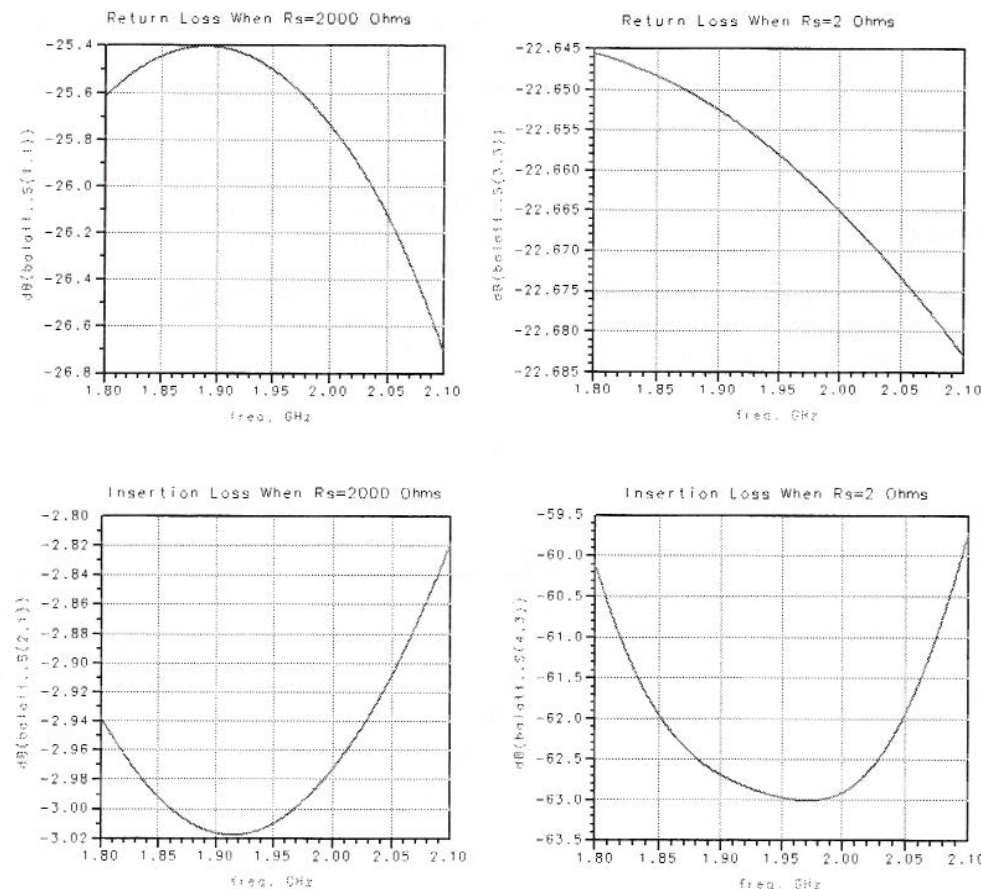


Figure 8. ADS simulation results

4. MEASUREMENT RESULTS

Return Loss Measurements

The balanced attenuator circuit was constructed on FR4 material with thickness of 0.8 mm. The input return loss of the attenuator was measured on a Agilent's 8753E network analyzer. Input drive level from the network analyzer was set to -30 dBm . Input return loss of better than 15 dB was measured on the attenuator board across the entire PCS band at all attenuator current range. There was no noticeable impedance variation when input drive level varied from -40 dBm to 0 dBm .

Deviation of the measured input return loss from the

extremely high return loss from simulation result is attributed to the finite port return loss and finite port-to-port isolation of the quadrature couplers. In theory, with ideal quadrature coupler, there should be no reflected power to the input port as all reflected power will be channeled to the 50 Ohm terminations. The reason of this deviation of return loss from simulation result can be easily explained by the abrupt change impedance introduce by conductance of the shunt PINs placed in points on the transmission lines. As the shunt conductance of the PINs increases with biasing current, difference between the characteristic impedance of the transmission line and the impedance of the point where the PINs are place increases. Therefore high signal reflection can occur at maximum attenuation setting and amount of reflection measured at the input port of the coupler depends largely on the port-to-port isolation and input port return loss of the coupler.

Figure 9 shows the measured input return loss of the attenuator board across the designed frequency band at different attenuator current setting. With 470 Ohms resistors each in series with the PINs for purpose of current control, a control voltage exceeding 12 Volts is required to attain the maximum signal attenuation at about 120 mA.

The output return loss of the attenuator was measured and the result was almost identical to the input return loss measurement as one would expect it to be. Any difference between the input return loss and output return loss is attributed to the minor difference between input and output quadrature couplers. Figure 10 shows the variation of input return loss with attenuator current at 1.8 GHz, 1.9 GHz and 2.05 GHz. As the relationship

Input Return Loss vs Frequency

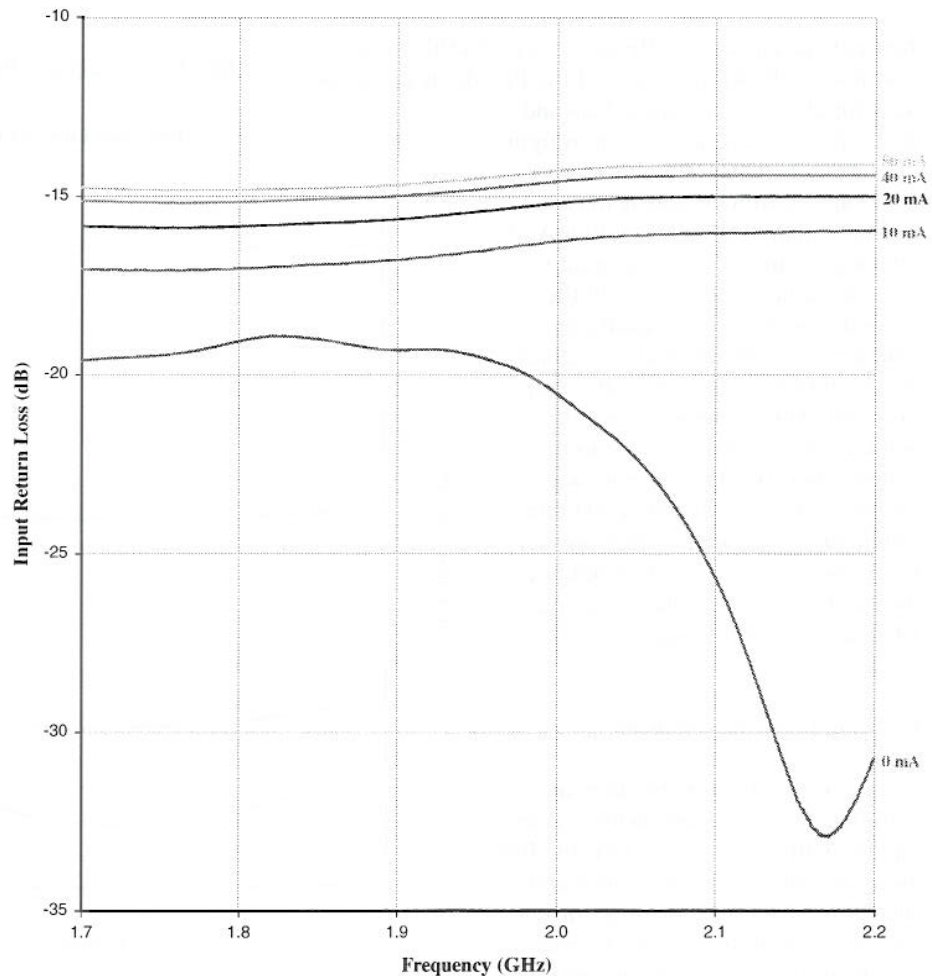


Figure 9. attenuator board input return loss vs frequency at different attenuator current setting.

Input Return Loss vs Attenuator Current

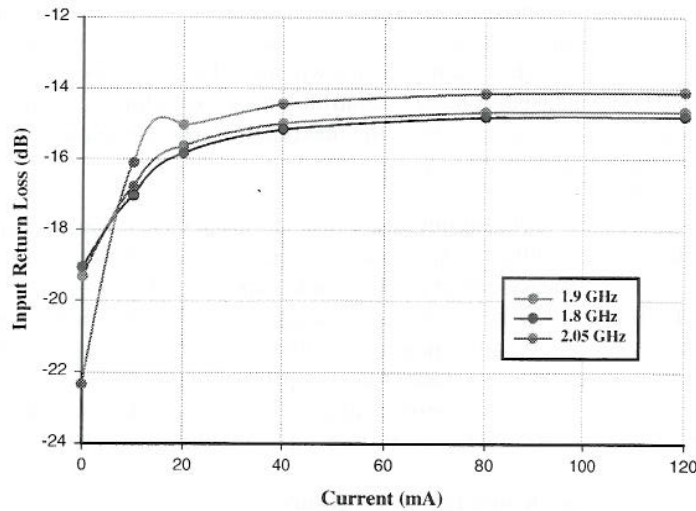


Figure 10. input return loss across attenuator current levels.

between the current and RF resistance of a PIN diode is non-linear, the RF resistance of the PIN diode decreases very rapidly with increasing bias and this explains the results shown in figure 10, where the input return loss curve rises rapidly with increasing bias and begins to flatten off at about 20 mA of attenuator current. It is important to provide 'solid' grounding to all the ground pins of QBA-18 quadrature couplers from Mini-Circuits to achieve good return loss at the input and output port. 50 Ohm termination should be soldered as closed as possible to the coupler two 100 Ohm resistors was parallel to form the required 50 Ohm termination. Capacitor which present low impedance at 1.9 GHz should be used as RF bypass for the $\lambda/4$ delivering DC bias to the PIN diodes.

Insertion Loss Measurement

As expected, when the attenuator current is low, the insertion loss varies rapidly with current. At 80 mA, the PIN diode exhibits low RF resistance and any further increase in biasing current cannot further reduce the RF resistance significantly and therefore the insertion loss becomes relatively insensitive to changes in biasing current. Measurement on a NWA indicates the excellent flatness in the insertion

loss across frequency and high dynamic range in excess of 50 dB as indicated in figure 11. At 0 mA, losses due to quadrature couplers contribute to about 1 dB of the total insertion loss.

Approximately 1 dB of the measured insertion loss is attributed to loss occurred in the transmission line (loss due to material and radiation). Other factors contributing to power loss are amplitude and phase imbalances causing RF power to be dissipated across the 50 Ohm termination of the output quadrature coupler and power combining at the output power becomes incomplete. Figure 12 shows the insertion loss varying with attenuator current. Changes in the insertion loss with varying level of input drive from -30 dBm to +10 dBm is minimal and both minimum and maximum insertion loss setting. This ensures the transmitter chain driving a load with relatively constant impedance with minimal impedance fluctuation with constantly varying RF drive.

Third-Order Intercept Point Measurement

Insertion Loss vs Frequency

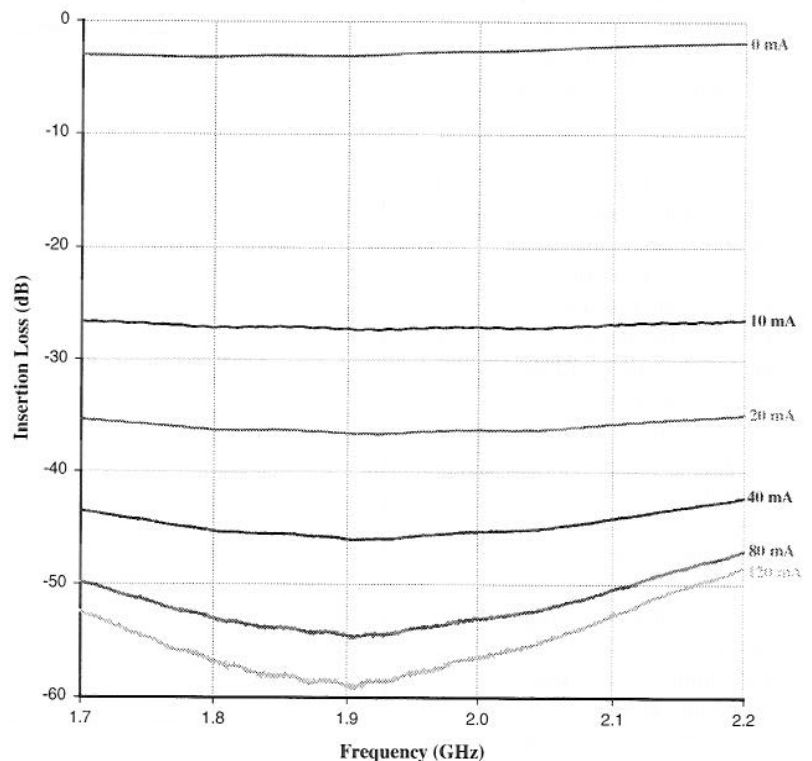


Figure 11. measured insertion loss across frequency on HP8753E NWA

Insertion Loss vs Attenuator Current

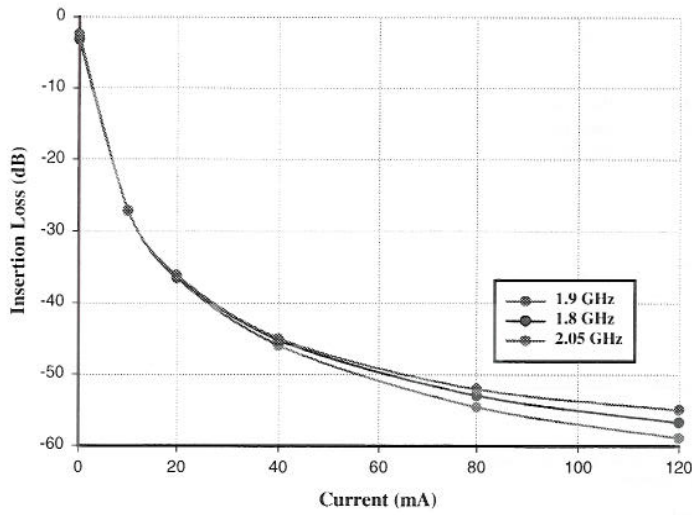


Figure 12. variation of insertion loss across attenuator current range.

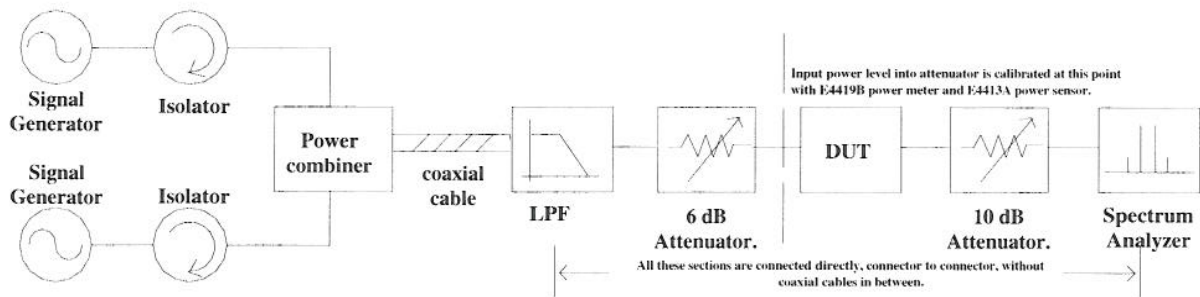


Figure 13. setup diagram for balanced attenuator input IP3 measurement.

The high linearity of the attenuator attained with Agilent's HSMP-481B low distortion PIN diodes makes the input IP3 measurement on this balanced attenuator a difficult one. A setup for such a measurement is shown in figure 13. The frequency separation between the two signal sources is 1 MHz apart. When measuring input IP3 of this attenuator, this fairly large frequency separation was chosen to avoid the side band noise of the signal generator affecting the measurement accuracy. The signal sources used were HP 83712B and HP 83630B synthesized signal generators to generate the two tone required for intermodulation measurement. Two Alcatel Ferrocom 10A1-01 isolators was placed at the output of the signal generators to prevent the signals from one generator intermodulating with the other at the output circuitry of the generators and affects measurement accuracy. The two tones from the output of isolators are then combined in the ANZAC H-8-4 power combiner before delivering to the attenuator board. A Mini-

Circuit's SLP-2400 low pass filter with 2.4 GHz cut-off frequency was used to filter out the second harmonics of the two tones. To further ensure the attenuator input is driven from a wide band low VSWR source, a 6 dB attenuator is placed right before the balanced attenuator input port. The output levels of the signal generators are then adjusted until the power levels at the 6 dB attenuator output reads +2.9 dBm (@ 1901 MHz and 1902 MHz) on a HP E4419B power meter with HP E4413A power sensor. A 10 dB attenuator right after the balanced attenuator output port improves the VSWR of the load seen from the attenuator output port and at the same time, provides additional attenuation to the signal before going into the HP8563E spectrum analyzer. The spectrum analyzer's video bandwidth and resolution bandwidth was set to 1 Hz and measurement span was 10 KHz. As shown in figure 14, excellent input IP3 was measured on the balanced attenuator board

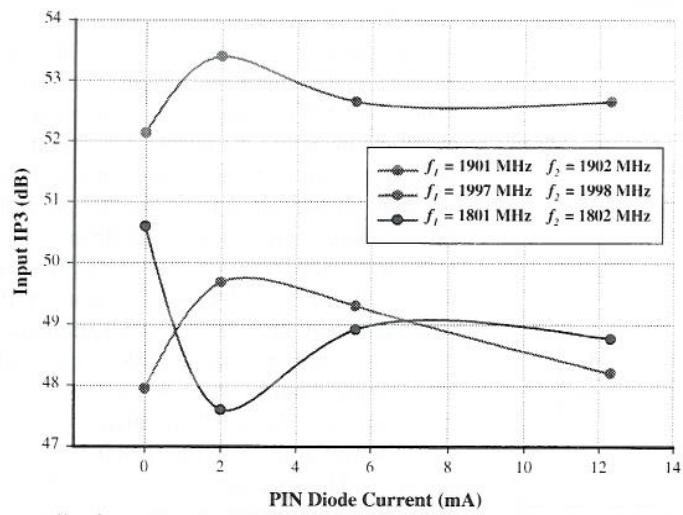
exceeding +50 dBm @ 1.9 GHz across biasing current range.

In theory balanced configuration will measure 3 dB higher IP3 than the unbalanced version. Input IP3 is measured as :

$$IIP_3 = \frac{\Delta}{2} + P_{in}$$

where P_{in} is the power levels of the two tone right at the input port of the attenuator. Δ in this case is taken as the power level difference (at the attenuator output port) between the lowest of the two fundamental tones and the highest of the two third-order spurious products.

Input IP3 vs PIN Diode Current



Note : Input IP3 was calculated as $IP3 \approx \Delta/2 + P_{m}$, where Δ , measured at the output is the difference between the lowest of the two fundamental tones and the highest of the two third-order spurious product.

Figure 14. input IP3 with varying attenuator current.