The equation is:

$$t_{off} = \frac{t_{on(max)} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$$

$$= \frac{20 \times 10^{-6}}{0.37 + 1}$$

$$= 14.6\ \mu s$$

Since $t_{on(max)} + t_{off} = 20\ \mu s$

$$t_{on(max)} = 20\ \mu s - 14.6\ \mu s$$

$$= 5.4\ \mu s$$

Note that the ratio of $t_{on}/(t_{on} + t_{off})$ does not exceed the maximum of 6/7 or 0.857. This maximum is defined by the 6:1 ratio of charge–to–discharge current of timing capacitor C_T (refer to Figure 3).

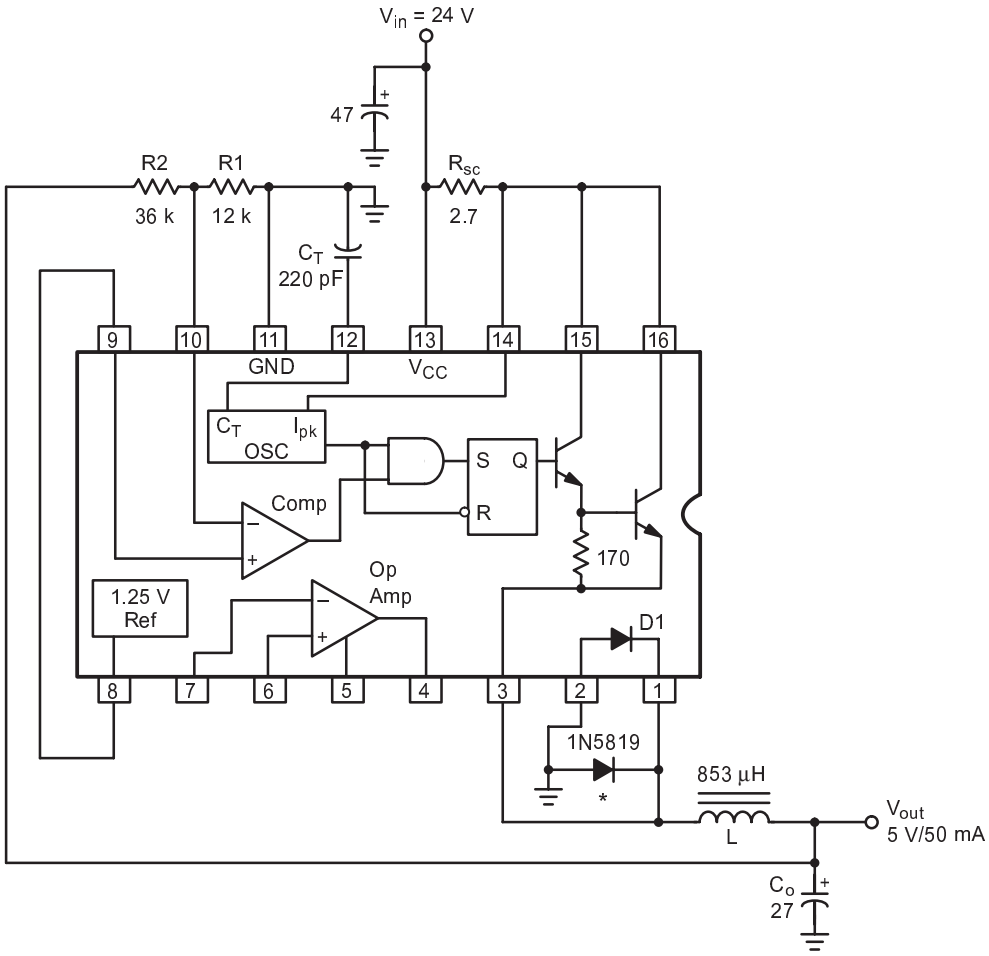
4. The maximum on–time, $t_{on(max)}$, is set by selecting a value for C_T.

$$C_T = 4.0 \times 10^{-5}\, t_{on}$$

$$= 4.0 \times 10^{-5}\, (5.4 \times 10^{-6})$$

$$= 216\ pF$$

Use a standard 220 pF capacitor.



Test	Conditions	Results
Line Regulation	V_{in} = 18 to 30 V, I_{out} = 50 mA	Δ = 16 mV or ± 0.16%
Load Regulation	V_{in} = 24 V, I_{out} = 25 to 50 mA	Δ = 28 mV or ± 0.28%
Output Ripple	V_{in} = 21.6 V, I_{out} = 50 mA	24 mV_{p-p}
Short Circuit Current	V_{in} = 24 V, R_L = 0.1 Ω	105 mA
Efficiency, Internal Diode	V_{in} = 24 V, I_{out} = 50 mA	45.3%
Efficiency, External Diode*	V_{in} = 24 V, I_{out} = 50 mA	72.6%

Figure 9. Step–Down Design Example

5. The peak switch current is:

$$I_{pk(switch)} = 2\ I_{out}$$
$$= 2\ (50 \times 10^{-3})$$
$$= 100\ mA$$

6. With knowledge of the peak switch current and maximum on time, a minimum value of inductance can be calculated.

$$L_{min} = \left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$$
$$= \left(\frac{21.6 - 0.8 - 5.0}{100 \times 10^{-3}}\right) 5.4 \times 10^{-6}$$
$$= 853\ \mu H$$

7. A value for the current limit resistor, R_{sc}, can be determined by using the current level of $I_{pk(switch)}$ when V_{in} = 24 V.

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{sat} - V_{out}}{L_{min}}\right) t_{on(max)}$$
$$= \left(\frac{24 - 0.8 - 5.0}{853 \times 10^{-6}}\right) 5.4 \times 10^{-6}$$
$$= 115\ mA$$
$$R_{sc} = \frac{0.33}{I'_{pk(switch)}}$$
$$= \frac{0.33}{115 \times 10^{-3}}$$
$$= 2.86\ \Omega,\ \text{use } 2.7\ \Omega$$

This value may have to be adjusted downward to compensate for conversion losses and any increase in $I_{pk(switch)}$) current if V_{in} varies upward. Do not set R_{sc} to exceed the maximum $I_{pk(switch)}$ limit of 1.5 A when using the internal switch transistor.

8. A minimum value for an ideal output filter capacitor can now be obtained.

$$C_o = \frac{I_{pk(switch)}\ (t_{on} + t_{off})}{8\ V_{ripple(p-p)}}$$
$$= \frac{0.1\ (20 \times 10^{-6})}{8\ (25 \times 10^{-3})}$$
$$= 10\ \mu F$$

Ideally this would satisfy the design goal, however, even a solid tantalum capacitor of this value will have a typical ESR (equivalent series resistance) of 0.3 Ω which will contribute 30 mV of ripple. The ripple components are not in phase, but can be assumed to be for a conservative design. In satisfying the example shown, a 27 μF tantalum with an ESR of 0.1 Ω was selected. The ripple voltage should be kept to a low value since it will directly affect the system line and load regulation.

9. The nominal output voltage is programmed by the R1, R2 resistor divider. The output voltage is:

$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

The divider current can go as low as 100 μA without affecting system performance. In selecting a minimum current divider R1 is equal to:

$$R1 = \frac{1.25}{100 \times 10^{-6}}$$
$$= 12,500\ \Omega$$

Rearranging the above equation so that R2 can be solved yields:

$$R2 = R1\left(\frac{V_{out}}{1.25} - 1\right)$$

If a standard 5% tolerance 12 k resistor is chosen for R1, R2 will also be a standard value.

$$R2 = 12 \times 10^3\left(\frac{5.0}{1.25} - 1\right)$$
$$= 36\ k$$

Using the above derivation, the design is optimized to meet the assumed conditions. At $V_{in(min)}$, operation is at the onset of continuous mode and the output current capability will be greater than 50 mA. At $V_{in(nom)}$ i.e., 24 V, the current limit will activate slightly above the rated I_{out} of 50 mA.

STEP–UP SWITCHING REGULATOR OPERATION

The basic step–up switching regulator is shown in Figure 7b and the waveform is in Figure 10. Energy is stored in the inductor during the time that transistor Q1 is in the "on" state. Upon turn–off, the energy is transferred in series with V_{in} to the output filter capacitor and load. This configuration allows the output voltage to be set to any value greater than that of the input by the following relationship:

$$V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}}\right) + V_{in} \text{ or } V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}} + 1\right)$$

An explanation of the step–up converter's operation is as follows. Initially, assume that transistor Q1 is off, the inductor current is zero, and the output voltage is at its nominal value. At this time, load current is being supplied only by C_o and it will eventually fall below nominal. This deficiency will be sensed by the control circuit and it will initiate an on–cycle, driving Q1 into saturation. Current will start to flow from V_{in} through the inductor and Q1 and rise at a rate of ΔI/ΔT = V/L. The voltage across the inductor is equal to $V_{in} - V_{sat}$ and the peak current is:

$$I_L = \left(\frac{V_{in} - V_{sat}}{L}\right) t$$

When the on–time is completed, Q1 will turn off and the magnetic field in the inductor will start to collapse generating a reverse voltage that forward biases D1, supplying energy to C_o and R_L. The inductor current will decay at a rate of ΔI/ΔT = V/L and the voltage across it is equal to $V_{out} + V_F - V_{in}$. The current at any instant is: