

AFE7900 4T6R RF Sampling AFE with 12 GSPS DACs and 3 GSPS ADCs

1 Features

- Quad RF sampling 12-GSPS transmit DACs
- Quad RF sampling 3-GSPS receive ADCs
- Dual RF sampling 3-GSPS feedback (auxiliary RX) ADCs
- Maximum RF signal bandwidth:
 - 4TX or 2FB: 1200 MHz or 2TX: 2400 MHz
 - RX: 1200 MHz (no FB), 600 MHz (with FB)
- RF frequency range:
 - TX: 5MHz - 7.4GHz
 - RX/FB: 5MHz - 7.4GHz
- Digital step attenuators (DSA):
 - TX: 40 dB range, 0.125-dB steps
 - RX or FB: 25 dB range, 0.5-dB steps
- Single or dual-band DUC or DDCs for TX and RX
- 16x NCOs per TX or RX and FB
- Optional Internal PLL or VCO for DAC or ADC clocks or external clock at DAC or ADC sample rate
- Sysref Alignment Detector
- SerDes data interface:
 - JESD204B and JESD204C compatible
 - 8 SerDes transceivers up to 29.5 Gbps
 - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

2 Applications

- [Radar](#)
- [Seeker front end](#)
- [Defense radio](#)
- Tactical communications infrastructure
- [Wireless communications test](#)

3 Description

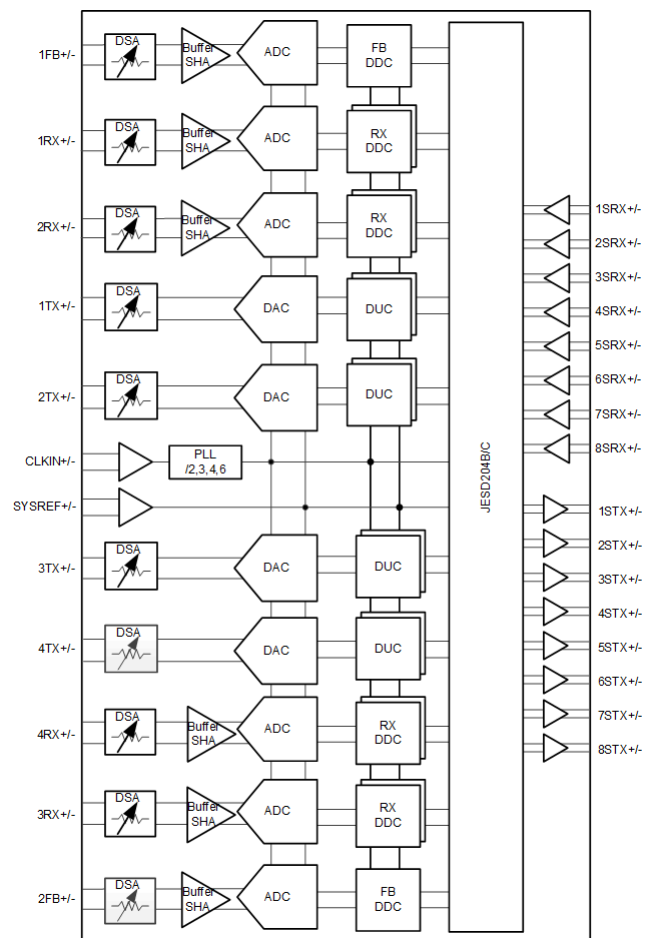
The AFE7900 is a high performance, wide bandwidth multi-channel transceiver, integrating four RF sampling transmitter chains, four RF sampling receiver chains and two RF sampling feedback chains (six RF sampling ADCs total). With operation up to 7.4 GHz, this device enables direct RF sampling in the L, S and C-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

The TX signal paths support interpolation and digital up conversion options that deliver up to 1200 MHz of signal bandwidth for four TX or 2400 MHz for two TX. The output of the DUCs drives a 12-GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40-dB range and 1-dB analog and 0.125-dB digital steps.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE
AFE7900	FC-BGA	17.00 mm × 17.00 mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.



Functional Block Diagram



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4 Description (continued)

Each receiver chain includes a 25-dB range DSA (Digital Step Attenuator), followed by a 3-GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of data bandwidth up to 1200 MHz for four RX without FB paths or 600 MHz with two FB paths (1200 MHz BW each).

The device contains a SYSREF timing detector to allow optimization of the SYSREF input timing relative to the device clock.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2021	*	Initial release.

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6 Pin Configuration and Functions

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y
20	VDD1P2 TXCLK	2TXOUT+	2TXOUT-	VDD1P2 TXCLK	VDD1P8TX	1TXOUT-	1TXOUT+	VDD1P8TX	VSSTX	VDD1P2 PLLCLK REF	VDD1P8 PLLVC0	VSSTX	VDD1P8TX	3TXOUT+	3TXOUT-	VDD1P8TX	VDD1P2 TXCLK	4TXOUT-	4TXOUT+	VDD1P2 TXCLK					
19	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTX	VSSTX	PULL DOWN	SYSREF+	SYSREF-	VSSPLL CLKREF	VSSTX	VSSTX	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK					
18	VSSFBCLK	VSSFBCLK	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSPLL CLKREF	VDD1P2 PLLCLK REF	VDD1P8 PLLVC0 REF	VSSPLL CLKREF	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSFBCLK	VSSFBCLK					
17	VDD1P8 FBCLK	VSSFB	VSSTX	VDD1P2 TXENC	VSSTXENC	VSSTX	VDD1P8 TXDAC	VDD1P8 TXDAC	VSS PLLRCML	REFCLK+	REFCLK-	VSS PLLRCML	VDD1P8 TXDAC	VDD1P8 TXDAC	VSSTX	VSSTXENC	VDD1P2 TXENC	VSSTX	VSSFB	VDD1P8 FBCLK					
16	1FBIN+	VSSFB	VDD1P8FB	VDD1P2FB	VSSTXENC	GTR_7 SPIB2SEN	GTR_17 SPIB1CLK	GTR_14 SPIB1SEN	VSSPLL FBCLM	VDD1P8PLL	VDD1P8PLL	VSSPLL FBCLM	GTL_3 _AUX0	GTL_7 _ALARM1	GTL_15 _GPIO3	GTL_18 _SPIASDO	VSSTXENC	VDD1P2FB	VDD1P8FB	VSSFB	2FBIN+				
15	1FBIN-	VSSFB	VDD1P8FB	VDD1P2FB	VDD1P2FB	GTR_15 _RESETZ	GTR_13 _TRST	GTR_3 _TXDD1	GTR_9 _SPIB2SDO	VDD1P2 PLLRCML	VDD1P2 PLLFBCLM	GTL_3 _AUX0	GTL_2 _ALARM2	GTL_4 _SPIACK	GTL_5 _RXDD2	VDD1P2FB	VDD1P2FB	VDD1P8FB	VSSFB	2FBIN-					
14	VDD1P8 FBCLK	VSSFB	VSSFB	VDD1P2FB	VDD1P2RX	GTR_5 _TDO	GTR_18 _TDI	GTR_4 _TCLK	GTR_2 _SPIB2CLK	GTR_8 _FBTDD1	GTL_8 _AUX1	GTL_9 _AUX2	GTL_17 _SPIASDO	GTL_1 _SPEEP	GTL_5 _SPIASEN	VDD1P2RX	VDD1P2FB	VSSFB	VSSFB	VDD1P8 FBCLK					
13	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_0 _RXGSWAP	GTR_6 _SPIB2 _SDIO	GND_ESD	DVDD0P9	DVDD0P9	GND_ESD	GTL_0 _AUX3	GTL_11 _AUX3	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX					
12	1RXIN+	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_11 _SPIB1 _SDO	GTR_1 _GPIO1	DGND	DVDD0P9	DVDD0P9	DGND	GTL_13 _AUX4	GTL_12 _BIST1	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	3RXIN+					
11	1RXIN-	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P2RX	VDD1P2RX	GTR_10 _TMS	GTR_12 _SPIB1 _SDIO	DGND	DVDD0P9	DVDD0P9	DGND	GTL_14 _AUX5	GTL_10 _BIST0	VDD1P2RX	VDD1P2RX	VDD1P8RX	VDD1P8RX	VSSRX	3RXIN-					
10	VDD1P2RX	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_6 _RXBLNB	GBR_5 _FSPIDB	DGND	DVDD0P9	DVDD0P9	DGND	GBL_5 _GPIO15	GBL_6 _GPIO16	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRX	VDD1P2RX					
9	VDD1P8 RXCLK	VSSRXCLK	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_9 _SYNCB _OUT0-	GBR_7 _SYNCB _OUT0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_7 _SYNCB _OUT1+	GBL_9 _SYNCB _OUT1-	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRXCLK	VDD1P8 RXCLK					
8	2RXIN-	VSSRX	VSSRXCLK	GND_ESD	GBR_10 _FSPICLKA	VDD1P8RX	GBR_13 _GPIO8	GBR_8 _SYNCB _IN0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_8 _GPIO19	GBL_13 _GPIO19	VDD1P8RX	GBL_10 _GPIO17	GND_ESD	VSSRXCLK	VSSRX	4RXIN-					
7	2RXIN+	VSSRX	VSSRXCLK	GND_ESD	GBR_11 _RXALNB	GBR_14 _FSPIDA	GBR_12 _GPIO7	GBR_17 _SYNCB _IN0-	DGND	DVDD0P9	DVDD0P9	DGND	GBL_17 _SYNCB _IN1-	GBL_12 _FSPICLKD	GBL_14 _FSPIDD	GBL_11 _GPIO18	GND_ESD	VSSRXCLK	VSSRX	4RXIN+					
6	VDD1P8 RXCLK	VSSRXCLK	GBR_0 _GPIO4	GBR_19 _GPIO12	GBR_16 _GPIO10	GBR_1 _GPIO5	GBR_15 _GPIO9	VDD1P8 GPIO	DGND	DVDD0P9	DVDD0P9	DGND	VDD1P8 GPIO	GBL_15 _FSPIDC	GBL_1 _FBTDD2	GBL_16 _RXCLNB	GBL_19 _GPIO20	GBL_0 _GPIO13	VSSRXCLK	VDD1P8 RXCLK					
5	VSSRXCLK	VSSRXCLK	GBR_18 _GPIO11	GBR_2 _RXALNB	GBR_4 _GPIO6	GBR_3 _FSPICLKB	IFORCE	VSSGPIO	DGND	DVDD0P9	DVDD0P9	DGND	VSSGPIO	VSSENSE	GBL_3 _GPIO14	GBL_4 _RXDLNB	GBL_2 _FSPICLKC	GBL_18 _TXDD2	VSSRXCLK	VSSRXCLK					
4	VSST	VSST	1STX+	VDDTOP9	2STX+	VDDA1P8	3STX-	VDDA1P8	4STX-	VSST	VSST	5STX-	VDDA1P8	6STX-	VDDA1P8	7STX+	VDDTOP9	8STX+	VSST	VSST					
3	1SRX+	VSST	1STX-	VDDTOP9	2STX-	VDDA1P8	3STX+	VDDA1P8	4STX+	SERDES _AMUX1	SERDES _AMUX2	5STX+	VDDA1P8	6STX+	VDDA1P8	7STX-	VDDTOP9	8STX-	VSST	VSST					
2	1SRX-	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	DVDD0P9	DVDD0P9	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST	VSST					
1	VSST	2SRX+	2SRX-	VSST	3SRX+	3SRX-	VSST	4SRX+	4SRX-	VSST	VSST	5SRX-	5SRX+	VSST	6SRX-	6SRX+	VSST	7SRX-	7SRX+	VSST					

Figure 6-1. ABJ Package, 400-Pin FCBGA, Top View

Table 6-1. Pin Functions

BALL NAME	BALL NUMBER	I/O ⁽¹⁾	DESCRIPTION
RF INTERFACES			
1FBIN-	A15	I	Feedback Channel 1 RF input: negative terminal. Unused RX inputs can be left open.
1FBIN+	A16	I	Feedback Channel 1 RF input: positive terminal. Unused RX inputs can be left open.
2FBIN-	Y15	I	Feedback Channel 2 RF input: negative terminal. Unused RX inputs can be left open.
2FBIN+	Y16	I	Feedback Channel 2 RF input: positive terminal. Unused RX inputs can be left open.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O ⁽¹⁾	DESCRIPTION
1RXIN–	A11	I	Receiver Channel 1 RF input: negative terminal. Unused RX inputs can be left open.
1RXIN+	A12	I	Receiver Channel 1 RF input: positive terminal. Unused RX inputs can be left open.
2RXIN–	A8	I	Receiver Channel 2 RF input: negative terminal. Unused RX inputs can be left open.
2RXIN+	A7	I	Receiver Channel 2 RF input: positive terminal. Unused RX inputs can be left open.
3RXIN–	Y11	I	Receiver Channel 3 RF input: negative terminal.
3RXIN+	Y12	I	Receiver Channel 3 RF input: positive terminal. Unused RX inputs can be left open.
4RXIN–	Y8	I	Receiver Channel 4 RF input: negative terminal. Unused RX inputs can be left open.
4RXIN+	Y7	I	Receiver Channel 4 RF input: positive terminal. Unused RX inputs can be left open.
1TXOUT–	F20	O	Transmitter Channel 1 RF output: negative terminal. Connect to 1.8 V when not used.
1TXOUT+	G20	O	Transmitter Channel 1 RF output: positive terminal. Connect to 1.8 V when not used.
2TXOUT–	C20	O	Transmitter Channel 2 RF output: negative terminal. Connect to 1.8 V when not used.
2TXOUT+	B20	O	Transmitter Channel 2 RF output: positive terminal. Connect to 1.8 V when not used.
3TXOUT–	R20	O	Transmitter Channel 3 RF output: negative terminal. Connect to 1.8 V when not used.
3TXOUT+	P20	O	Transmitter Channel 3 RF output: positive terminal. Connect to 1.8 V when not used.
4TXOUT–	V20	O	Transmitter Channel 4 RF output: negative terminal. Connect to 1.8 V when not used.
4TXOUT+	W20	O	Transmitter Channel 4 RF output: positive terminal. Connect to 1.8 V when not used.
DIFFERENTIAL CLOCKS INPUTS			
REFCLK–	L17	I	Reference Clock Inputs: negative terminal
REFCLK+	K17	I	Reference Clock Inputs: positive terminal
SYSREF–	L19	I	SYSREEF inputs: negative terminals
SYSREF+	K19	I	SYSREEF inputs: positive terminals
SerDes CML INTERFACE			
1SRX–	A2	I	CML SerDes Interface Lane 1 input: negative terminal. Unused Serdes inputs can be left open.
1SRX+	A3	I	CML SerDes Interface Lane 1 input: positive terminal. Unused Serdes inputs can be left open.
2SRX–	C1	I	CML SerDes Interface Lane 2 input: negative terminal. Unused Serdes inputs can be left open.
2SRX+	B1	I	CML SerDes Interface Lane 2 input: positive terminal. Unused Serdes inputs can be left open.
3SRX–	F1	I	CML SerDes Interface Lane 3 input: negative terminal
3SRX+	E1	I	CML SerDes Interface Lane 3 input: positive terminal. Unused Serdes inputs can be left open.
4SRX–	J1	I	CML SerDes Interface Lane 4 input: negative terminal
4SRX+	H1	I	CML SerDes Interface Lane 4 input: positive terminal

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Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O ⁽¹⁾	DESCRIPTION
5SRX–	M1	I	CML SerDes Interface Lane 5 input: negative terminal. Unused Serdes inputs can be left open.
5SRX+	N1	I	CML SerDes Interface Lane 5 input: positive terminal. Unused Serdes inputs can be left open.
6SRX–	R1	I	CML SerDes Interface Lane 6 input: negative terminal. Unused Serdes inputs can be left open.
6SRX+	T1	I	CML SerDes Interface Lane 6 input: positive terminal. Unused Serdes inputs can be left open.
7SRX–	V1	I	CML SerDes Interface Lane 7 input: negative terminal. Unused Serdes inputs can be left open.
7SRX+	W1	I	CML SerDes Interface Lane 7 input: positive terminal. Unused Serdes inputs can be left open.
8SRX–	Y2	I	CML SerDes Interface Lane 8 input: negative terminal. Unused Serdes inputs can be left open.
8SRX+	Y3	I	CML SerDes Interface Lane 8 input: positive terminal. Unused Serdes inputs can be left open.
1STX–	C3	O	CML SerDes Interface Lane 1 output: negative terminal. Unused Serdes outputs can be left open.
1STX+	C4	O	CML SerDes Interface Lane 1 output: positive terminal. Unused Serdes outputs can be left open.
2STX–	E3	O	CML SerDes Interface Lane 2 output: negative terminal. Unused Serdes outputs can be left open.
2STX+	E4	O	CML SerDes Interface Lane 2 output: positive terminal. Unused Serdes outputs can be left open.
3STX–	G4	O	CML SerDes Interface Lane 3 output: negative terminal. Unused Serdes outputs can be left open.
3STX+	G3	O	CML SerDes Interface Lane 3 output: positive terminal. Unused Serdes outputs can be left open.
4STX–	J4	O	CML SerDes Interface Lane 4 output: negative terminal. Unused Serdes outputs can be left open.
4STX+	J3	O	CML SerDes Interface Lane 4 output: positive terminal. Unused Serdes outputs can be left open.
5STX–	M4	O	CML SerDes Interface Lane 5 output: negative terminal. Unused Serdes outputs can be left open.
5STX+	M3	O	CML SerDes Interface Lane 5 output: positive terminal. Unused Serdes outputs can be left open.
6STX–	P4	O	CML SerDes Interface Lane 6 output: negative terminal. Unused Serdes outputs can be left open.
6STX+	P3	O	CML SerDes Interface Lane 6 output: positive terminal. Unused Serdes outputs can be left open.
7STX–	T3	O	CML SerDes Interface Lane 7 output: negative terminal. Unused Serdes outputs can be left open.
7STX+	T4	O	CML SerDes Interface Lane 7 output: positive terminal. Unused Serdes outputs can be left open.
8STX–	V3	O	CML SerDes Interface Lane 8 output: negative terminal. Unused Serdes outputs can be left open.
8STX+	V4	O	CML SerDes Interface Lane 8 output: positive terminal. Unused Serdes outputs can be left open.
GPIO FUNCTIONS			
GBL_0_GPIO13	V6	I/O	GPIO.
GBL_1_FBTDD2	R6	I/O	Default location of FB TDD2 input signal.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O ⁽¹⁾	DESCRIPTION
GBL_2_FSPICLK	U5	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_3_GPIO14	R5	I/O	GPIO.
GBL_4_RXDLNB	T5	I/O	Default location of RX channel D AGC LNA Bypass output signal.
GBL_5_GPIO15	N10	I/O	GPIO.
GBL_6_GPIO16	P10	I/O	GPIO.
GBL_7_SYNCB_OUT1+	N9	I/O	Default location of JESD Sync\ 1 output differential positive terminal.
GBL_8_SYNCB_IN1+	N8	I/O	Default location of JESD Sync\ 1 input differential positive terminal.
GBL_9_SYNCB_OUT1–	P9	I/O	Default location of JESD Sync\ 1 output differential negative terminal.
GBL_10_GPIO17	T8	I/O	GPIO.
GBL_11_GPIO18	T7	I/O	GPIO.
GBL_12_FSPICLK	P7	I/O	Default and recommended location of FSPI D clock (FSPI for factory use only, available as generic GPIO).
GBL_13_GPIO19	P8	I/O	GPIO.
GBL_14_FSPIDD	R7	I/O	Default and recommended location of FSPI D data (FSPI for factory use only, available as generic GPIO).
GBL_15_FSPIDC	P6	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_16_RXCLNB	T6	I/O	Default location of RX channel C AGC LNA Bypass output signal.
GBL_17_SYNCB_IN1–	N7	I/O	Default location of JESD Sync\ 1 input differential negative terminal.
GBL_18_TXTDD2	V5	I/O	Default location of TX TDD2 input signal.
GBL_19_GPIO20	U6	I/O	GPIO.
GBR_0_GPIO4	C6	I/O	GPIO.
GBR_1_GPIO5	F6	I/O	GPIO.
GBR_2_RXALNB	D5	I/O	Default location of RX channel A AGC LNA Bypass output signal.
GBR_3_FSPICLKB	F5	I/O	Default and recommended location of FSPI B clock (FSPI for factory use only, available as generic GPIO).
GBR_4_GPIO6	E5	I/O	GPIO.
GBR_5_FSPIDB	H10	I/O	Default and recommended location of FSPI B data (FSPI for factory use only, available as generic GPIO).
GBR_6_RXBLNB	G10	I/O	Default location of RX channel B AGC LNA Bypass output signal.
GBR_7_SYNCB_OUT0+	H9	I/O	Default location of JESD Sync\ 0 output differential positive terminal.
GBR_8_SYNCB_IN0+	H8	I/O	Default location of JESD Sync\ 0 input differential positive terminal.
GBR_9_SYNCB_OUT0–	G9	I/O	Default location of JESD Sync\ 0 output differential negative terminal.
GBR_10_FSPICLKA	E8	I/O	Default location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_11_RXTDD1	E7	I/O	Default location of RX TDD1 input signal.
GBR_12_GPIO7	G7	I/O	GPIO.
GBR_13_GPIO8	G8	I/O	GPIO.

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Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O ⁽¹⁾	DESCRIPTION
GBR_14_FSPIDA	F7	I/O	Default and recommended location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_15_GPIO9	G6	I/O	GPIO.
GBR_16_GPIO10	E6	I/O	GPIO.
GBR_17_SYNCB_IN0–	H7	I/O	Default location of JESD Sync\ 0 input differential negative terminal.
GBR_18_GPIO11	C5	I/O	GPIO.
GBR_19_GPIO12	D6	I/O	GPIO.
GTL_0_GPIO2	N13	I/O	GPIO.
GTL_1_SLEEP	P14	I/O	Default location of Sleep input signal.
GTL_2_ALARM2	N15	I/O	Default location of Alarm 2 output signal.
GTL_3_AUX0	M15	I/O	GPIO or auxiliary low-speed ADC input 0
GTL_4_SPIACLK	P15	I/O	Fixed Location of SPI A Clock.
GTL_5_SPIASEN	R14	I/O	Fixed Location of SPI A Send Enable.
GTL_6_RXTDD2	R15	I/O	Default location of RX TDD2 input signal.
GTL_7_ALARM1	N16	I/O	Default location of Alarm 1 output signal.
GTL_8_AUX1	L14	I/O	GPIO or auxiliary low-speed ADC input 1.
GTL_9_AUX2	M14	I/O	GPIO or auxiliary low-speed ADC input 2.
GTL_10_BIST0	P11	I/O	Fixed Location for BIST0 Function. Set low when using JTAG, set high for normal operation.
GTL_11_AUX3	P13	I/O	GPIO or auxiliary low-speed ADC input 3.
GTL_12_BIST1	P12	I/O	Fixed Location for BIST1 Function. Set high when using JTAG, set low for normal operation.
GTL_13_AUX4	N12	I/O	GPIO or auxiliary low-speed ADC input 4.
GTL_14_AUX5	N11	I/O	GPIO or auxiliary low-speed ADC input 5.
GTL_15_GPIO3	P16	I/O	GPIO.
GTL_17_SPIASDIO	N14	I/O	Fixed Location of SPI A Serial Data Input (3- and 4-wire mode) or Output (3 wire mode only).
GTL_18_SPIASDO	R16	I/O	Fixed Location of SPI A Serial Data Output in 4-wire mode.
GTR_0_RXGSWAP	G13	I/O	Default location of RX gain swap input.
GTR_1_GPIO1	H12	I/O	GPIO.
GTR_2_SPIB2CLK	J14	I/O	Default and recommended location of SPI B2 clock.
GTR_3_TXTDD1	H15	I/O	Default location of TX TDD1 input signal.
GTR_4_TCLK	H14	I/O	Fixed location for JTAG Test Clock.
GTR_5_TDO	F14	I/O	Fixed location for JTAG Test Data Out.
GTR_6_SPIB2_SDIO	H13	I/O	Default and recommended location of SPI B2 serial data input/output.
GTR_7_SPIB2SEN	F16	I/O	Default and recommended location of SPI B2 enable input.
GTR_8_FBTDD1	K14	I/O	Default location of FB TDD1 input signal.
GTR_9_SPIB2SDO	J15	I/O	Default and recommended location of SPI B2 serial data output (4-wire mode)
GTR_10_TMS	G11	I/O	Fixed location for JTAG Test Mode Select.
GTR_11_SPIB1_SDO	G12	I/O	Default and recommended location of SPI B1 enable input.
GTR_12_SPIB_SDIO	H11	I/O	Default and recommended location of SPI B1 serial data input/output.
GTR_13_TRST	G15	I/O	Fixed location for JTAG Test Reset. Must be pulled low when the JTAG port is not used.
GTR_14_SPIB1SEN	H16	I/O	Default and recommended location of SPI B1 enable input.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O ⁽¹⁾	DESCRIPTION
GTR_15_RESETZ	F15	I/O	Fixed Location for reset function. Chip Reset to default register settings.
GTR_17_SPIB1CLK	G16	I/O	Default and recommended location of SPI B1 clock.
GTR_18_TDI	G14	I/O	Fixed location for JTAG Test Data Input.
POWER SUPPLIES			
DVDD	K2, K5, K6, K7, K8, K9, K10, K11, K12, K13, L2, L5, L6, L7, L8, L9, L10, L11, L12, L13	—	0.9-V digital power supply
VDD1P2FB	D14, D15, D16, E15, U14, U15, U16, T15	—	1.2-V supply for FB ADCs.
VDD1P8FB	C15, C16, V15, V16	—	1.8-V supply for FB ADC.
VDD1P8FBCLK	A14, A17, Y17, Y14	—	1.8-V supply for FB ADC clock.
VDD1P2PLLCLKREF	K20, K18, L18	—	1.2-V supply for PLL.
VDDPLL1P2FBCML	L15	—	1.2-V supply for PLL clock distribution to FB ADC.
VDDPLL1P2RXCML	K15	—	1.2-V supply for clock distribution to RX ADC.
VDD1P8PLL	K16, L16	—	1.8-V supply for PLL.
VDD1P8PLLVCO	L20	—	1.8-V supply for PLL/VCO. This is a sensitive net and requires extra care in layout.
VDD1P2RX	A10, A13, E11, E12, E13, E14, F11, F12, F13, R11, R12, R13, T11, T12, T13, T14, Y10, Y13	—	1.2-V supply for RX ADCs.
VDD1P8RX	C9, C10, C11, D9, D10, D11, E9, E10, F8, F9, F10, R8, R9, R10, T9, T10, U9, U10, U11, V9, V10, V11	—	1.8-V supply for RX ADCs.
VDD1P8RXCLK	A6, A9, Y6, Y9	—	1.8-V supply for RX ADC clocks.
VDD1P2TXENC	D17, U17	—	1.2-V supply for DAC encoder.
VDD1P2TXCLK	A20, D20, U20, Y20	—	1.2-V supply for DAC clock.
VDD1P8TX	E20, H20, N20, T20	—	1.8-V supply for DAC.
VDD1P8TXDAC	G17, H17, N17, P17	—	1.8-V supply for DAC.
VDD1P8GPIO	H6, N6	—	1.8-V supply for GPIO.
VDDA1P8	F3, F4, H3, H4, R3, R4, N3, N4	—	SerDes analog 1.8-V power supply.
VDDT0P9	D3, D4, U3, U4	—	SerDes digital 0.9-V power supply.
GROUND			
DGND	J5, J6, J7, J8, J9, J10, J11, J12, M5, M6, M7, M8, M9, M10, M11, M12	—	Digital core ground
VSSGPIO	H5, N5	—	GPIO ground.
VSSFB	B14, B15, B16, B17, C14, V14, W14, W15, W16, W17	—	Ground for FB ADC supply.
VSSFBCLK	A18, B18, W18, Y18	—	Ground for FB ADC 1.8-V clock supply.
GND_ESD	D7, D8, J13, M13, U7, U8	—	Ground for ESD protection circuits.
VSSRX	B7, B8, B10, B11, B12, C12, D12, B13, C13, D13, W7, W8, W10, W11, W13, U12, V12, W12, U13, V13	—	Ground for RX ADC.
VSSRXCLK	A5, B5, B6, B9, C7, C8, W5, W6, W9, Y5, V7, V8	—	Ground for RX ADC clocks.

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Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	I/O ⁽¹⁾	DESCRIPTION
VSSTX	B19, C17, C18, C19, D18, E18, E19, F17, F18, F19, G18, G19, H18, H19, J20, M20, N18, N19, P18, P19, R17, R18, R19, T18, T19, U18, V17, V18, V19, W19	—	Ground for TX DAC.
VSSTXENC	E16, E17, T16, T17	—	Ground for TX DAC encoder.
VSSTXCLK	A19, D19, U19, Y19	—	Ground for TX DAC clock.
VSSPLL	M19	—	Ground for PLL.
VSSPLLFBCML	J16, M16	—	Ground for FB ADC clock.
VSSPLLCLKREF	J18, M18	—	Ground for CLKREF PLL.
VSSPLLRXCML	J17, M17	—	Ground for RX ADC clock.
VSST	A1, A4, B2, B3, B4, C2, D1, D2, E2, F2, G1, G2, H2, J2, K1, K4, L1, L4, M2, N2, P1, P2, R2, T2, U1, U2, V2, W2, W3, W4, Y1, Y4	—	SerDes ground.
OTHERS			
IFORCE	G5	—	Reserved for TI use only. Do not connect.
PLL_LDOUT	J19	—	Connect with 100-nF capacitor to GND
SerDes_AMUX1	K3	—	Analog test pin for SerDes lane 1-4, can be left floating
SerDes_AMUX2	L3	—	Analog test pin for SerDes lane 5-8, can be left floating
VSENSE	P5	—	Process test: sense voltage (TI use only). Do not connect.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	−0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	−0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCML, VDD1P8GPIO, VDDA1P8	−0.5	2.1	V
Pin Voltage Range	{1/2/3/4}RXIN+/-	−0.5	VDDR1P8+0.3	V
	1FBIN+/-, 2FB+/-	−0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	−0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	−0.3	1.4	V
	{1:8}SRX+/-	−0.3	1.4	V
	{1:8}STX+/-	−0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	−0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	−0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	−0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Condition](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T _A	Ambient temperature	–40		85	°C
T _J	Operating Junction Temperature			110 ⁽¹⁾	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AFE7900	UNIT
		ABJ (FC-BGA)	
		400 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	16.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.42	°C/W
R _{θJB}	Junction-to-board thermal resistance	4.85	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	4.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Transmitter Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC _{RES}	DAC resolution			14		bits
f _{RFout}	RF output frequency range	f _{DAC} = 12 GSPS, 1 st Nyquist	5		6000	MHz
		f _{DAC} = 9 GSPS, 1 st Nyquist	5		4500	
		f _{DAC} = 9 GSPS, 2 nd Nyquist	4500		7400	
		f _{DAC} = 6 GSPS, 1 st Nyquist	5		3000	
		f _{DAC} = 6 GSPS, 2 nd Nyquist	3000		6000	
P _{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f _{out} = 10 MHz, f _{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f _{out} = 30 MHz, f _{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f _{out} = 400 MHz, f _{DAC} = 6GSPS, -0.1dBFS		5.6		dBm
		f _{out} = 850 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		4.3		dBm
		f _{out} = 1800 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		3.2		dBm
		f _{out} = 2600 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS		2.3		dBm
		f _{out} = 3500 MHz, -0.5dBFS		2.9		dBm
		f _{out} = 4900 MHz, -0.5dBFS		-0.6		dBm
		f _{out} = 3500 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-2.3		dBm
		f _{out} = 4900 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-3.4		dBm
		f _{out} = 4900 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-3.9		dBm
R _{TERM}	Output termination resistor	Default setting		100		Ω
ATT _{range}	DSA Attenuation range			40		dB
ATT _{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL) (2)	0 < Atten < 40dB, after calibration		±0.1		dB
		0 < Atten < 40dB, before calibration		±0.2		
ATT _{step}	DSA Gain Steps Phase accuracy, any 8dB range(2)	f _{out} = 30MHz		±1		deg
		f _{out} = 400MHz		±1		deg
		f _{out} = 850MHz		±1		deg
		f _{out} = 1800MHz		±1		deg
		f _{out} = 2600MHz		±1		deg
		f _{out} = 3500MHz		±1		
		f _{out} = 4900MHz		±1		deg
G _{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F _{out} < 4.9G		1.2		

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion	$f_{\text{DAC}} = 6 \text{ GSPS}$, $f_{\text{out}} = 5 \text{ MHz}$ $\pm 1 \text{ MHz}$, -7dBFS each tone		-48		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$, $f_{\text{out}} = 30 \text{ MHz}$ $\pm 1 \text{ MHz}$, -7dBFS each tone		-47		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$, $f_{\text{out}} = 400 \text{ MHz}$ $\pm 2 \text{ MHz}$, -7dBFS each tone		-51		dBc
		$f_{\text{out}} = 850 \text{ MHz} \pm 10 \text{ MHz}$, -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 1800 \text{ MHz} \pm 10 \text{ MHz}$, -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 2600 \text{ MHz} \pm 10 \text{ MHz}$, -7dBFS each tone		-64		dBc
		$f_{\text{out}} = 3500 \text{ MHz} \pm 10 \text{ MHz}$, -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 4900 \text{ MHz} \pm 10 \text{ MHz}$, -7dBFS each tone		-64		dBc
		$f_{\text{out}} = 5 \text{ MHz} \pm 1 \text{ MHz}$, -13dBFS each tone		-72		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$, $f_{\text{out}} = 30 \text{ MHz}$ $\pm 1 \text{ MHz}$, -13dBFS each tone		-71		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}$, $f_{\text{out}} = 400 \text{ MHz}$ $\pm 2 \text{ MHz}$, -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 850 \text{ MHz} \pm 10 \text{ MHz}$, -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 1800 \text{ MHz} \pm 10 \text{ MHz}$, -13dBFS each tone		-75		dBc
		$f_{\text{out}} = 2600 \text{ MHz} \pm 10 \text{ MHz}$, -13dBFS each tone		-79		dBc
		$f_{\text{out}} = 3500 \text{ MHz} \pm 10 \text{ MHz}$, -13dBFS each tone		-77		dBc
		$f_{\text{out}} = 4900 \text{ MHz} \pm 10 \text{ MHz}$, -13dBFS each tone		-77		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 30 \text{ MHz}$, $f_{\text{DAC}} = 6000 \text{ MSPS}$, interleave mode, 20Gbps SerDes rate		45		dBc
		$f_{\text{out}} = 400 \text{ MHz}$, $f_{\text{DAC}} = 6000 \text{ MSPS}$, interleave mode, 20Gbps SerDes rate		48		dBc
		$f_{\text{out}} = 850 \text{ MHz}$, $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		62		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$, $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		56		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$, $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		39		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$, $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		42		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$, $f_{\text{DAC}} = 11796.48 \text{ MSPS}$		60		dBc
$f_s/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24 \text{ MSPS}$, interleave mode		-47		dBc
		$f_{\text{DAC}} = 8847.36 \text{ MSPS}$, interleave mode		-43		dBc
		$f_{\text{DAC}} = 11796.48 \text{ MSPS}$, interleave mode		-43		dBc

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2 nd Harmonic Distortion (within Nyquist zone)	$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 5 \text{ MHz}$		-72		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 30 \text{ MHz}$		-75		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 100 \text{ MHz}$		-73		dBc
		$f_{\text{out}} = 400 \text{ MHz}$		-46		dBc
		$f_{\text{out}} = 850 \text{ MHz}$		-65		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-68		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-47		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-59		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-48		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-74		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-67		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-69		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-59		dBc
HD3	3 rd Harmonic Distortion (within Nyquist zone)	$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 5 \text{ MHz}$		-46		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 30 \text{ MHz}$		-48		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 100 \text{ MHz}$		-49		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 400 \text{ MHz}$		-49		dBc
		$f_{\text{out}} = 850 \text{ MHz}$		-56		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-58		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-60		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-63		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-66		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 5 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-83		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 30 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-83		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{DAC}} = 6 \text{ GSPS}, f_{\text{out}} = 400 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-88		dBc

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 5\text{ MHz}$		-58		dBc
		$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 30\text{ MHz}$		-60		dBc
		$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 100\text{ MHz}$		-61		dBc
		$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 400\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 850\text{ MHz}$		-85		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-90		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-84		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-87		dBc
		$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 5\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-92		dBc
		$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 30\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-94		dBc
		$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 100\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 400\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-85		dBc
		$f_{\text{out}} = 850\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-89		dBc
		$f_{\text{out}} = 1800\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-92		dBc
		$f_{\text{out}} = 2600\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 3500\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-88		dBc
		$f_{\text{out}} = 4900\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-89		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{DAC}} = 6\text{ GSPS}$, $f_{\text{out}} = 400\text{ MHz}$		87		dBc
		$f_{\text{out}} = 850\text{ MHz}$, $f_{\text{DAC}} = 11796.48\text{ MSPS}$		84		dBc
		$f_{\text{out}} = 1800\text{ MHz}$, $f_{\text{DAC}} = 11796.48\text{ MSPS}$		78		dBc
		$f_{\text{out}} = 2600\text{ MHz}$, $f_{\text{DAC}} = 11796.48\text{ MSPS}$		80		dBc
		$f_{\text{out}} = 3500\text{ MHz}$, $f_{\text{DAC}} = 11796.48\text{ MSPS}$		81		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{ MSPS}$, $f_{\text{OUT}} = f_{\text{DAC}}/4\text{-}50\text{MHz}$		-95		dBFS
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$, $f_{\text{OUT}} = f_{\text{DAC}}/4\text{-}50\text{MHz}$		-88		dBFS
		$f_{\text{DAC}} = 11796.48\text{ MSPS}$, $f_{\text{OUT}} = f_{\text{DAC}}/4\text{-}50\text{MHz}$		-76		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{ MSPS}$, $f_{\text{OUT}} = f_{\text{DAC}}/2\text{-}50\text{MHz}$		-52		dBFS
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$, $f_{\text{OUT}} = f_{\text{DAC}}/2\text{-}50\text{MHz}$		-45		dBFS
		$f_{\text{DAC}} = 11796.48\text{ MSPS}$, $f_{\text{OUT}} = f_{\text{DAC}}/2\text{-}50\text{MHz}$		-49		dBFS

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3*f_s/4$	Fixed Spur	2nd Nyquist, $f_{\text{DAC}} = 5898.24\text{MSPS}$, $f_{\text{OUT}} = 3*f_{\text{DAC}}/4 - 50\text{MHz}$		-82		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 8847.36\text{MSPS}$, $f_{\text{OUT}} = 3*f_{\text{DAC}}/4 - 50\text{MHz}$		-75		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $f_{\text{OUT}} = 3*f_{\text{DAC}}/4 - 50\text{MHz}$		-49		dBFS
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-70		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-66		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-62		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-51		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 1.8425\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-71		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-66		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-61		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-50		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-72		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-66		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-60		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-49		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-71		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-65		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-58		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-47		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-69		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-64		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-58		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-47		dBc

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-65		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-59		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-53		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-41		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-63		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-56		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-49		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-38		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-63		dBc
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-56		dBc
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-51		dBc
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{out}}=-13\text{dBFS}$		-41		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{OUT}}=-13\text{dBFS}$		0.16		%
		$F_{\text{out}} = 1.8425\text{ GHz}$, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{OUT}}=-13\text{dBFS}$		0.21		%
		$F_{\text{out}} = 2.6\text{ GHz}$, $f_{\text{DAC}} = 11796.48\text{MSPS}$, $P_{\text{OUT}}=-13\text{dBFS}$		0.24		%
		$F_{\text{out}} = 3.5\text{ GHz}$, $P_{\text{OUT}}=-13\text{dBFS}$		0.27		%
		$F_{\text{out}} = 4.9\text{ GHz}$, $P_{\text{OUT}}=-13\text{dBFS}$		0.38		%
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 5\text{ MHz}$	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-148		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-143		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-139		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-129		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 30\text{ MHz}$	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-154		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-146		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-142		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, $P_{\text{out}}=-12\text{dBFS}$		-132		dBFS/Hz

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 100\text{ MHz}$	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-158		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-150		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-146		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-136		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 400\text{ MHz}$	Atten=0dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-160		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-153		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-150		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 6000\text{MSPS}$, 20Gbps SerDes rate, Pout=-12dBFS		-139		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-158.8		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-152.7		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-148.7		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-137.9		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-157.9		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-151.3		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-145.6		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-134.8		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-158.3		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-151.6		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-144.9		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-134.0		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 3.5\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-158.2		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-150.9		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-144.4		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-133.4		dBFS/ Hz

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD _{dBFS}	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-154.6		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-147.0		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-140.7		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 11796.48\text{MSPS}$, Pout=-13dBFS		-129.9		dBFS/ Hz
S22	Output Return Loss, +/- $f_c \times 10\%$	with matching		-12		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT ⁽¹⁾	$f_{\text{out}} = 10\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽³⁾		-96		dB
		$f_{\text{out}} = 30\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽³⁾		-97		dB
		$f_{\text{out}} = 100\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽³⁾		-102		dB
		$f_{\text{out}} = 400\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽⁴⁾		-85		dB
		$f_{\text{out}} = 900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-80		dB
		$f_{\text{out}} = 1850\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-77		dB
		$f_{\text{out}} = 2600\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-64		dB
		$f_{\text{out}} = 3500\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-61		dB
		$f_{\text{out}} = 4900\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-60		dB
Isolation	Far Channel: 1/2TXOUT to 3/4TXOUT	$f_{\text{out}} = 10\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽³⁾		-104		dB
		$f_{\text{out}} = 30\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽³⁾		-100		dB
		$f_{\text{out}} = 100\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽³⁾		-105		dB
		$f_{\text{out}} = 400\text{ MHz}$, $f_{\text{DAC}} = 6000\text{MSPS}$, straight mode ⁽⁴⁾		-97		dB
		$f_{\text{out}} = 900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-90		dB
		$f_{\text{out}} = 1850\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-91		dB
		$f_{\text{out}} = 2600\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-93		dB
		$f_{\text{out}} = 3500\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-94		dB
		$f_{\text{out}} = 4900\text{ MHz}$, $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-83.2		dB

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$ below 6GHz and $f_{\text{DAC}} = 9000\text{MSPS}$ above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN _{TXADD}	Additive Phase Noise External Clock Mode ⁽⁵⁾	$f_{\text{out}} = 3.7\text{GHz}$, $f_{\text{OFFSET}} = 100\text{Hz}$		-97		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$, $f_{\text{OFFSET}} = 1\text{kHz}$		-106		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$, $f_{\text{OFFSET}} = 10\text{kHz}$		-117		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$, $f_{\text{OFFSET}} = 100\text{kHz}$		-128		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$, $f_{\text{OFFSET}} = 1\text{MHz}$		-138		dBc/Hz
		$f_{\text{out}} = 3.7\text{GHz}$, $f_{\text{OFFSET}} = 10\text{MHz}$		-144		dBc/Hz

- (1) Measured with differential 100 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
- (2) After DSA calibration procedure
- (3) measured with 1 μH DC feed inductor
- (4) measured with 0.39 μH DC feed inductor
- (5) Input clock phase noise subtracted.

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7.6 RF ADC Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$ below 6GHz and $f_{\text{ADC}} = 3000\text{MSPS}$ above 6GHz; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC _{RES}	ADC resolution			14		bits
F _{RFin}	RF input frequency range		5		7400	MHz
P _{FS_CW,min}	Min Full scale input power, at device pins ⁽¹⁾	$f_{\text{IN}} = 5\text{ MHz}$, DSA=0dB, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-0.4		dBm
		$f_{\text{IN}} = 30\text{ MHz}$, DSA=0dB, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-2.2		dBm
		$f_{\text{IN}} = 410\text{ MHz}$, DSA=0dB, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 12		-2.5		dBm
		$f_{\text{IN}} = 830\text{ MHz}$, DSA=0dB		-2.9		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA=0dB		-2.8		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA=0dB		-1.8		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA=0dB		-0.4		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA=0dB		0.1		dBm
P _{FS_CW,MAX}	MAX Full scale input power - reliability limited, at device pins	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		19.7		dBm
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		17.8		dBm
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		17.6		dBm
		$f_{\text{IN}} = 830\text{ MHz}$		16.7		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$		17.0		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$		18		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$		18.5		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$		19.3		dBm
R _{TERM}	Input reference impedance			100.0		Ω
ATT _{range}	DSA Attenuation range			25.0		dB
ATT _{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	$\Delta = \text{Gatt}(X) - \text{Gatt}(X-1)$, $F_{\text{in}} = 3610\text{MHz}$, after calibration		0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}} = 3610\text{MHz}$, after calibration		0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}} = 4910\text{MHz}$, after calibration		1.8		deg
G _{flat}	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		dB
		Measured Over 400MHz BW		1.1		dB

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$ below 6GHz and $f_{\text{ADC}} = 3000\text{MSPS}$ above 6GHz; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 3dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density ⁽³⁾ (small signal = -30dBFS)	$f_{\text{IN}} = 5\text{ MHz}$, DSA = 3dB, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-147.1		dBFS/Hz
		$f_{\text{IN}} = 30\text{ MHz}$, DSA = 3dB, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-150.7		dBFS/Hz
		$f_{\text{IN}} = 410\text{ MHz}$, DSA = 3dB, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		-155.4		dBFS/Hz
		$f_{\text{IN}} = 830\text{ MHz}$, DSA = 3dB		-156.2		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA = 3dB		-156.0		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA = 3dB		-155.4		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA = 3dB		-155.1		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA = 3dB		-155.1		dBFS/Hz
		$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48, $3 \leq \text{Atten} \leq 22$		-147.8		dBFS/Hz
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24, $3 \leq \text{Atten} \leq 22$		-151.5		dBFS/Hz
		$f_{\text{IN}} = 410\text{ MHz}$, $3 \leq \text{Atten} \leq 22$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		-156.6		dBFS/Hz
		$f_{\text{IN}} = 830\text{ MHz}$, $3 \leq \text{Atten} \leq 22$		-156.0		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$, $3 \leq \text{Atten} \leq 25$		-155.8		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$, $3 \leq \text{Atten} \leq 25$		-155.7		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$, $3 \leq \text{Atten} \leq 25$		-155.4		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$, $3 \leq \text{Atten} \leq 25$		-155.8		dBFS/Hz
NF _{min}	Noise Figure min DSA Atten=0 - 3dB	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		29.4		dB
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		24.5		dB
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		19.3		dB
		$f_{\text{IN}} = 830\text{ MHz}$		19.1		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		19.0		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		20.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		22.8		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		22.4		dB

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$ below 6GHz and $f_{\text{ADC}} = 3000\text{MSPS}$ above 6GHz; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 3dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure ⁽⁴⁾ DSA Atten=4dB	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		30.6		dB
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		25.1		dB
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		20.1		dB
		$f_{\text{IN}} = 830\text{ MHz}$		20.0		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		20.6		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		21.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		23.5		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		22.3		dB
NF _{max}	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		45.9		dB
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		40.2		dB
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		35.0		dB
		$f_{\text{IN}} = 830\text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		37.6		dB
IMD3	3 rd order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 30 \pm 1\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-82		dBc
		$f_{\text{IN}} = 400\text{MHz}$ and 405MHz , $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		-75		dBc
		$f_{\text{IN}} = 840\text{ MHz}$		-82		dBc
		$f_{\text{IN}} = 1770\text{ MHz}$		-84		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-74		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-77		dBc
		$f_{\text{IN}} = 4920\text{ MHz}$		-76		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		78		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		100		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		94		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		81		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		79		dBFS

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$ below 6GHz and $f_{\text{ADC}} = 3000\text{MSPS}$ above 6GHz; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 3dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}^{(2)}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-84		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, Bypass Mode (TI only test mode)		-91		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, Bypass Mode (TI only test mode)		-90		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-84		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-78		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, Bypass Mode (TI only test mode)		-96		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, Bypass Mode (TI only test mode)		-94		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-80		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-85		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-75		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-94		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-94		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		-94		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-81		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dBFS
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		101		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		105		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		95		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		89		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		89		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		87		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		90		dBFS

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$ below 6GHz and $f_{\text{ADC}} = 3000\text{MSPS}$ above 6GHz; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 3dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion ⁽²⁾ $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-104		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, Bypass Mode (TI only test mode)		-91		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, Bypass Mode (TI only test mode)		-104		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$, with board trim		-79		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$, with board trim		-102		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$, with board trim		-100		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$, with board trim		-101		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$, with board trim		-99		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-103		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, Bypass Mode (TI only test mode)		-84		dBFS
		$f_{\text{IN}} = 381\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, Bypass Mode (TI only test mode)		-91		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-94		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13\text{ dBFS}$	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-104		dBFS
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-105		dBFS
		$f_{\text{IN}} = 410\text{ MHz}$, $f_{\text{ADC}} = 3000\text{MSPS}$, $f_{\text{NCO}} = 400\text{MHz}$, Decimate by 24		-95		dBFS
		$f_{\text{IN}} = 830\text{ MHz}$		-89		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-89		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-90		dBFS
RX-RX/FB Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN 1FBIN to 1RXIN 2FBIN to 3RXIN	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-98		dB
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-98		dB
		$f_{\text{IN}} = 400\text{ MHz}$		-88		dB
		$f_{\text{IN}} = 830\text{ MHz}$		-77		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		-71		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		-74		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		-77		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		-65		dB

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, $f_{\text{ADC}} = 2949.12\text{MSPS}$ below 6GHz and $f_{\text{ADC}} = 3000\text{MSPS}$ above 6GHz; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 3dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX-FB Isolation	Near Channel: 1TXOUT to 1FBIN 3TXOUT to 2FBIN	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-92		dB
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-93		dB
		$f_{\text{IN}} = 400\text{ MHz}$		-92		dB
		$f_{\text{IN}} = 830\text{ MHz}$		-84		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		-88		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		-86		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		-82		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		-81		dB
TX-RX Isolation	Far Channel: 1TXOUT to 1RXIN 3TXOUT to 2RXIN	$f_{\text{IN}} = 5\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 17\text{MHz}$, Decimate by 48		-105		dB
		$f_{\text{IN}} = 30\text{ MHz}$, $f_{\text{ADC}} = 1500\text{MSPS}$, $f_{\text{NCO}} = 30\text{MHz}$, Decimate by 24		-101		dB
		$f_{\text{IN}} = 400\text{ MHz}$		-99		dB
		$f_{\text{IN}} = 830\text{ MHz}$		-86		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		-87		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		-84		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		-82		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dB

- (1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) After HD2 trim on specific printed circuit board.
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB

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7.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f _{VCO2}	VCO2 min frequency				8.848	GHz
	VCO2 max frequency		9.216			GHz
f _{VCO3}	VCO3 min frequency				9.8304	GHz
	VCO3 max frequency		10.24			GHz
f _{VCO4}	VCO4 min frequency				11.7965	GHz
	VCO4 max frequency		12.288			GHz
DIV _{DAC}	DAC sample rate divider		1, 2 or 3			
DIV _{FBADC}	ADC sample rate divider from DAC sample rate		1, 2, 3, 4, 6 or 8			
DIV _{RXADC}	ADC sample rate divider		1, 2, 3, 4, 6 or 8			
PN _{VCO}	Closed Loop Phase Noise F _{PLL} = 11.79848 GHz F _{REF} =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise F _{PLL} =8.84736 GHz F _{REF} =491.52MHz	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise F _{PLL} = 9.8403 GHz F _{REF} =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise F _{PLL} = 7.86432GHz F _{REF} =491.52MHz	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F _{rms}	Clock PLL integrated phase error ⁽¹⁾	f _{PLL} =11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f _{PLL} =8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f _{PLL} =9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f _{PFD}	PFD frequency		100		500	MHz
PN _{pll_flat}	Normalized PLL flat Noise	f _{VCO} = 11796.48MHz		-226.5		dBc/Hz
F _{REF}	Input Clock frequency		0.1		12	GHz
V _{SS}	Input Clock level		0.6		1.8	Vppdiff

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance ⁽²⁾	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution

(2) Refer to S11 data available from TI for impedance vs frequency

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7.8 Digital Electrical CharacteristicsTypical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V _{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V _{SRCOM}	SerDes Input Common Mode			400		mV
Z _{SRdiff}	SerDes Internal Differential Termination ⁽¹⁾			100		Ω
F _{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance ⁽²⁾	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V _{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V _{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z _{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V _{IH}	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V _{IL}	Low-Level Input Voltage			0.4×VDD1 P8GPIO		V
I _{IH}	High-Level Input Current		-250		250	mA
I _{IL}	Low-Level Input Current		-250		250	mA
C _L	CMOS input capacitance			2		pF
V _{OH}	High-Level Input Voltage		VDD1P8G PIO-0.2			V
V _{OL}	Low-Level Input Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
F _{SYSREFMAX}	SYSREF Input Frequency Maximum			40		MHz
V _{SWINGSRMAX}	SYSREF Input Swing Maximum			1.8		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} < 500MHz		0.3		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} > 500MHz		0.6		Vppdiff ⁽³⁾
V _{COMSRMAX}	SYSREF Input Common Mode Voltage Maximum			0.8		V
V _{COMSRMIN}	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z _T	Input termination	differential		100 ⁽¹⁾		Ω
C _L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V _{ICOM}	Input Common Voltage			1.2		V
V _{ID}	Differential Input Voltage swing			450		Vppdiff ⁽³⁾
Z _T	Input termination	differential		100		Ω
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V _{OCOM}	Output Common Voltage			1.2		V
V _{OD}	Differential Output Voltage swing			500		Vppdiff ⁽³⁾

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z _T	Internal Termination			100		Ω

- (1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
- (2) Loss tolerance is bump to bump from STX to SRX
- (3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

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7.9 Power Supply Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 737.28MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T2F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec $f_{\text{DAC}} = 5898.24\text{ SPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 1.85\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1	948.2			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8		533.7			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		77.3			mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX		299.4			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		804.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		49.1			mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9		2041.3			mA
P_{diss}	Power Dissipation		6027.1			mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 8847.36\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{OUT}} = f_{\text{IN}} = 1.9, 2.6\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	820.4			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8		735.2			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		74.4			mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX		289.0			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		822.0			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		45.6			mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9		2263.8			mA
P_{diss}	Power Dissipation		6359.2			mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	1668.6			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8		965.1			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		77.6			mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX		893.4			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		879.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		50.7			mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9		3826.9			mA
P_{diss}	Power Dissipation		10513.0			mW

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 737.28MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 7372.8\text{ MSPS}$ $f_{\text{ADC}} = 2457.6\text{ MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1	1611.5			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8		694.5			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		72.8			mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX		768.5			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		940.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		45.5			mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9		3000.5			mA
P_{diss}	Power Dissipation		9087.4			mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 3.5\text{ GHz}$ $f_{\text{RX}} = 3.5\text{ GHz}$ 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1	821.8			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8		808.5			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		77.4			mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX		289.5			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		682.0			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		49.0			mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9		2123.3			mA
P_{diss}	Power Dissipation		6209.3			mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 8: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.	20.3			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8		292.8			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		12.6			mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX		4.6			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		54.3			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		15.3			mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9		313.1			mA
P_{diss}	Power Dissipation		956.8			mW

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 737.28MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 9: 4T4R2F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msp/s RX Rate 122.88 Msp/s $f_{\text{DAC}} = 5898.24\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 0.85\text{ GHz}$ $f_{\text{RX}} = 0.8\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-8-8-1		1593.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			840.6		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			77.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			905.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			817.7		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			52.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2405.2		mA
P_{diss}	Power Dissipation			8814.3		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msp/s RX Rate 245.76 Msp/s $f_{\text{DAC}} = 8847.36\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85\text{ GHz}$ $f_{\text{RX}} = 1.75\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1		1626.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			976.4		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			902.7		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1111.9		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			48.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3578.9		mA
P_{diss}	Power Dissipation			10515.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msp/s $f_{\text{DAC}} = 11796.48\text{ MSPS}$, interleave mode, $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 3.7\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		797		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			817		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73.2		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			179		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			906		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			70.5		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2483		mA
P_{diss}	Power Dissipation			6754		mW

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 737.28MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 3.7\text{GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		726		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			876		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			72.8		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			583		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			270		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			71.6		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2130		mA
P_{diss}	Power Dissipation			6124		mW

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Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 737.28MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11c: TDD 4T4R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps f_{DAC} = 11796.48 MSPS, interleave mode, f_{ADC} = 2949.12 MSPS $f_{\text{TX}} = f_{\text{RX}} = 3.7\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		779		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			832		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73.1		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			280		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			747		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			70.8		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2395		mA
P_{diss}	Power Dissipation			6596		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11d: FDD 4T4R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps f_{DAC} = 11796.48 MSPS, interleave mode, f_{ADC} = 2949.12 MSPS $f_{\text{TX}} = f_{\text{RX}} = 3.7\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		1236		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			915		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73.2		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			583		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			923		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			72		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3097		mA
P_{diss}	Power Dissipation			8798		mW

7.10 Timing Requirements

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{\text{s}}(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{\text{h}}(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{\text{s}}(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK ⁽¹⁾		$5 + t_{\text{sCLK}}$		ns
$t_{\text{s}}(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{\text{(SCLK_W)}}$	Minimum SCLK period: registers write		25		ns
$t_{\text{(SCLK_R)}}$	Minimum SCLK period: registers read		50		ns
$t_{\text{d}}(\text{data_out})$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge

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7.11 Switching Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

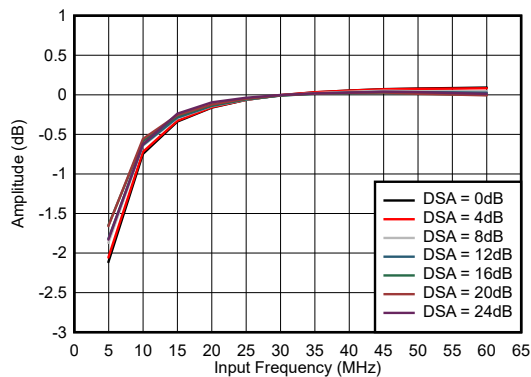
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
t _{JESD TX}	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles ⁽¹⁾
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t _{JESD RX}	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles ⁽¹⁾
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
FB Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t _{JESD FB}	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles ⁽¹⁾
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

7.12 Typical Characteristics

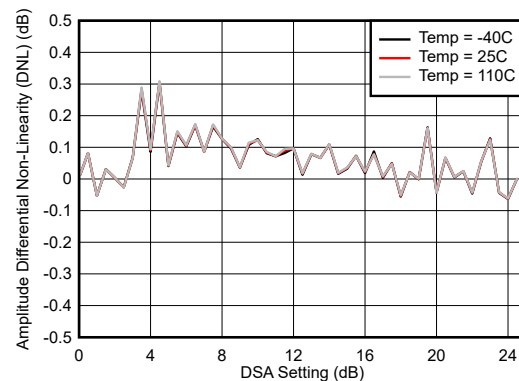
7.12.1 RX Typical Characteristics 30 MHz and 400 MHz

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.



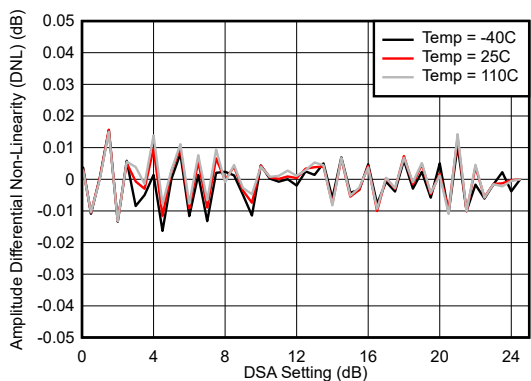
Normalized to 30 MHz

Figure 7-1. RX In-Band Gain Flatness, $f_{\text{IN}} = 30\text{ MHz}$



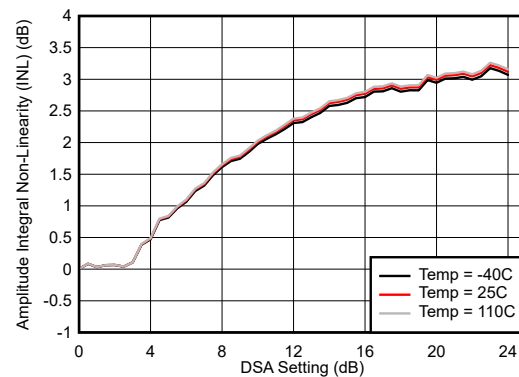
Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30 MHz



Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

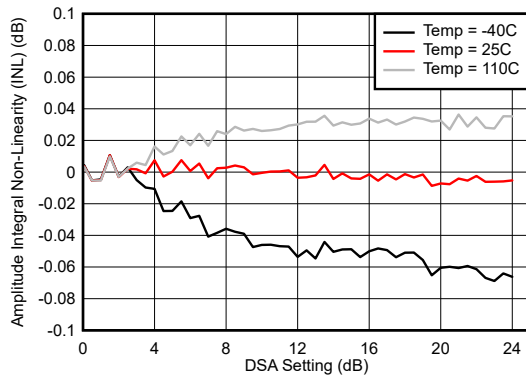
Figure 7-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30 MHz

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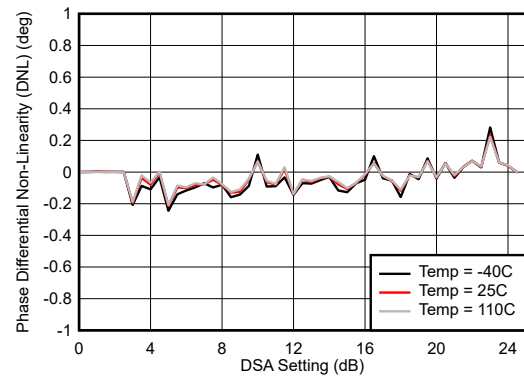
7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.



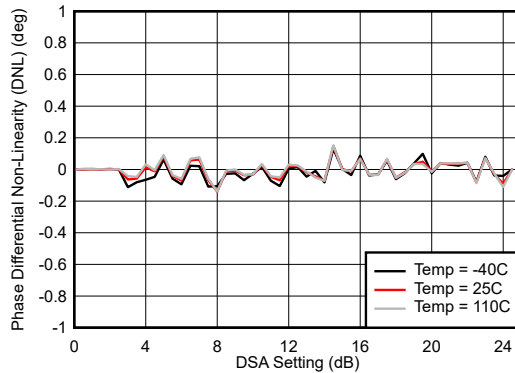
$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

Figure 7-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30 MHz



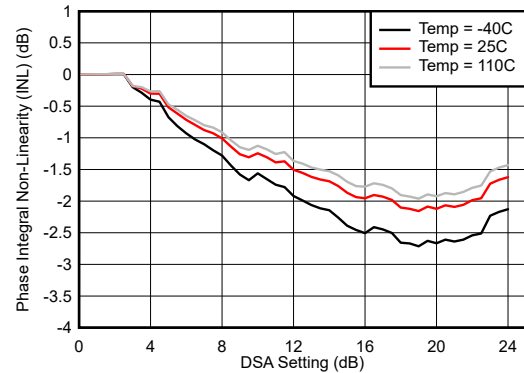
$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

Figure 7-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30 MHz



$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

Figure 7-7. RX Calibrated Differential Phase Error vs DSA Setting at 30 MHz

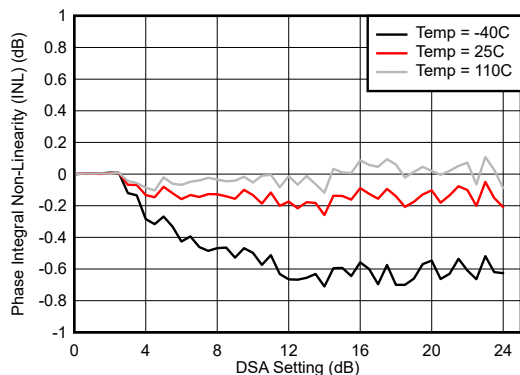


$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

Figure 7-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30 MHz

7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

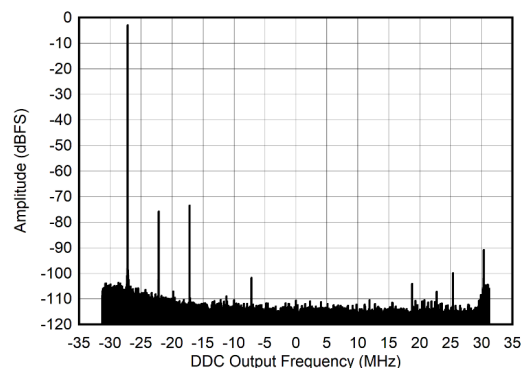
Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.



With 0.8 GHz matching

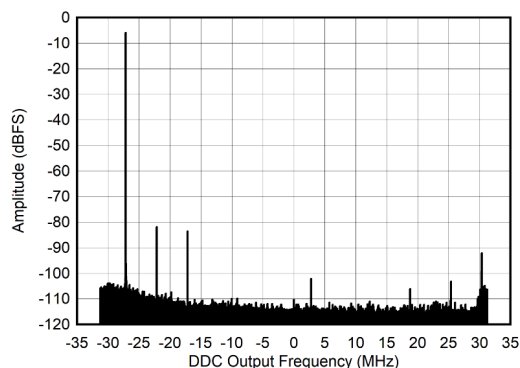
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30 MHz



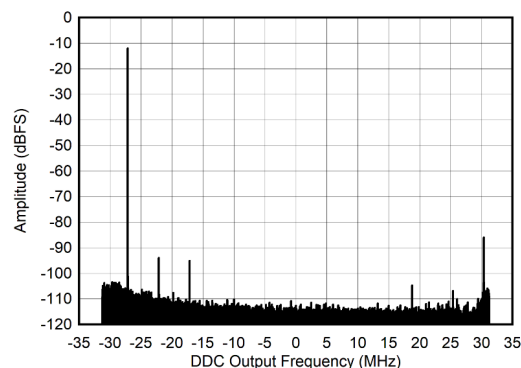
$A_{\text{IN}} = -3\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-10. RX Output FFT at 5 MHz



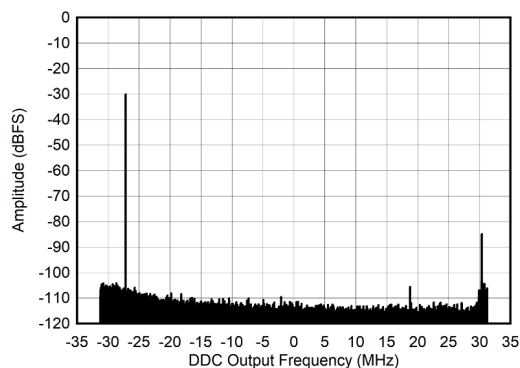
$A_{\text{IN}} = -6\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-11. RX Output FFT at 5 MHz



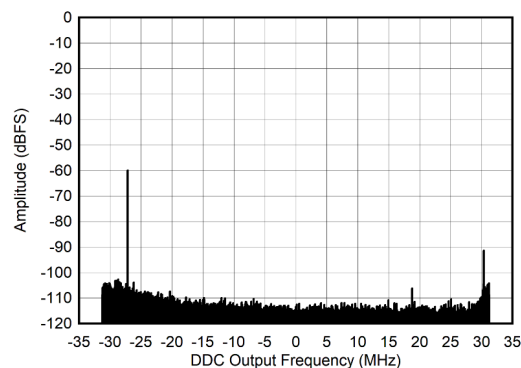
$A_{\text{IN}} = -12\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-12. RX Output FFT at 5 MHz



$A_{\text{IN}} = -30\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-13. RX Output FFT at 5 MHz



$A_{\text{IN}} = -60\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

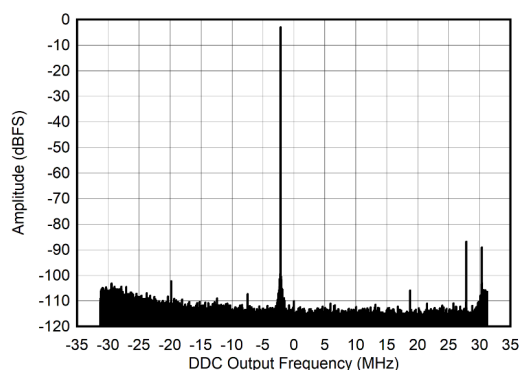
Figure 7-14. RX Output FFT at 5 MHz

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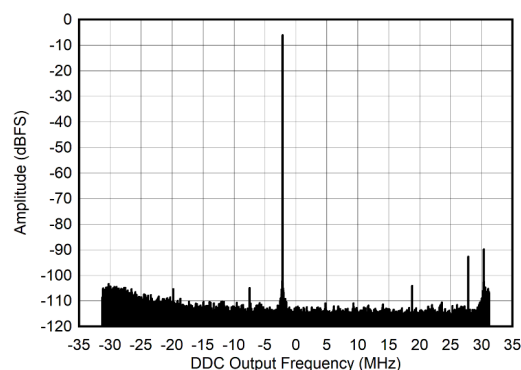
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7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

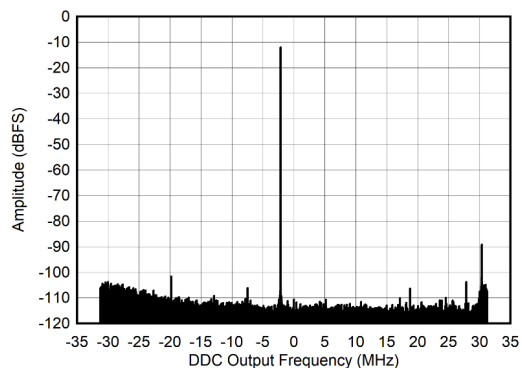
Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.



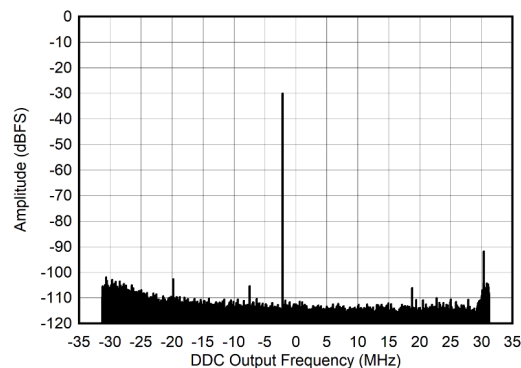
$A_{\text{IN}} = -3\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-15. RX Output FFT at 30 MHz

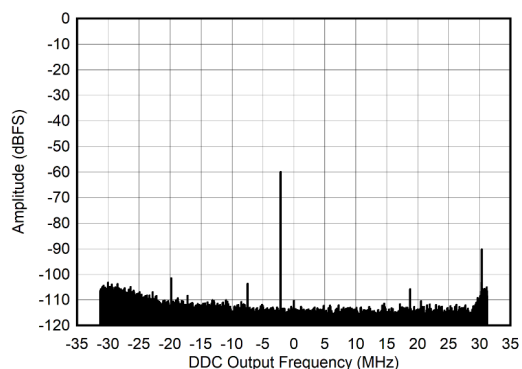
$A_{\text{IN}} = -6\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-16. RX Output FFT at 30 MHz

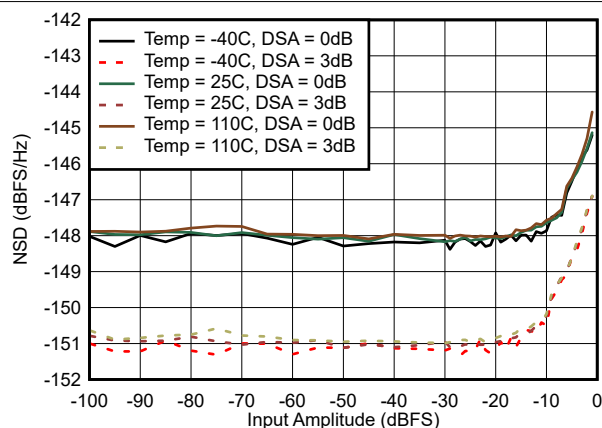
$A_{\text{IN}} = -12\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-17. RX Output FFT at 30 MHz

$A_{\text{IN}} = -30\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

Figure 7-18. RX Output FFT at 30 MHz

$A_{\text{IN}} = -60\text{ dBFS}$, $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$,
Decimate by 24x

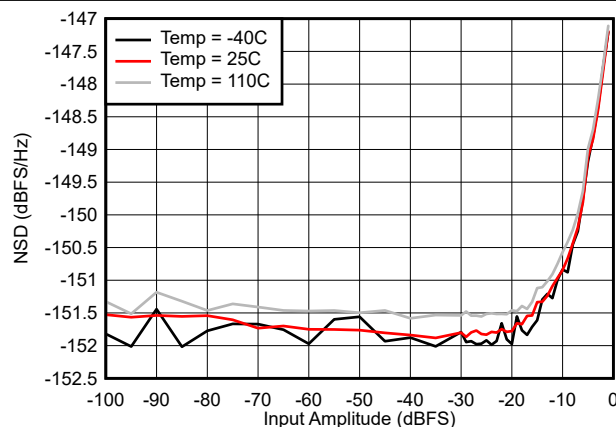
Figure 7-19. RX Output FFT at 30 MHz

$f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x

Figure 7-20. NSD vs Input Amplitude at 30 MHz with DSA = 0 and 3dB

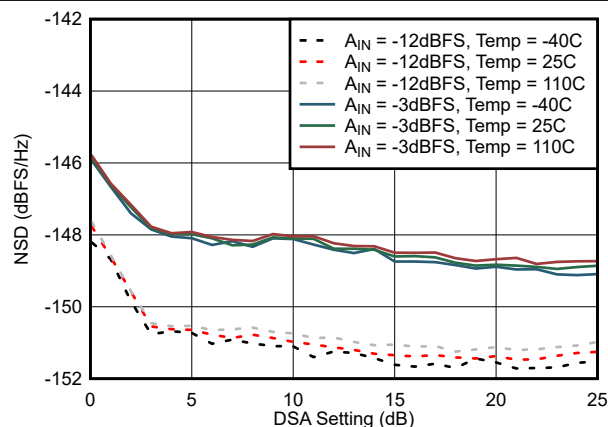
7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.



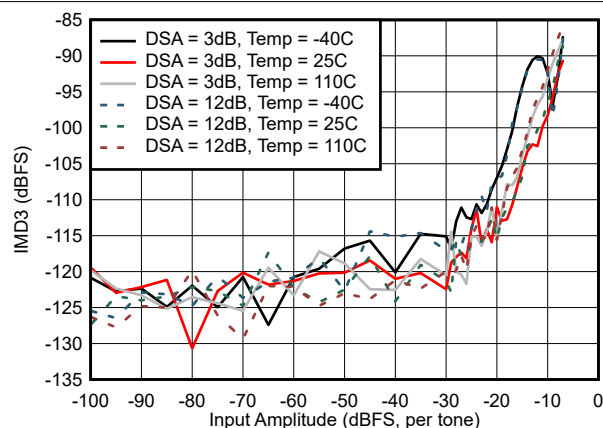
$f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x

Figure 7-21. NSD vs Input Amplitude at 30 MHz with DSA = 12



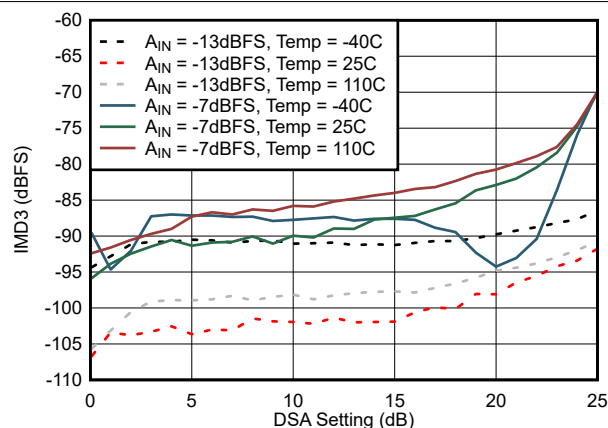
$f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x

Figure 7-22. NSD vs DSA Attenuation at 30 MHz



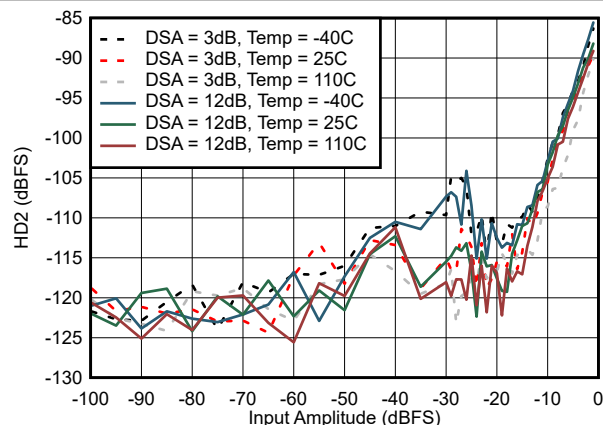
$f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x

Figure 7-23. IMD3 vs Input Amplitude at 30 MHz



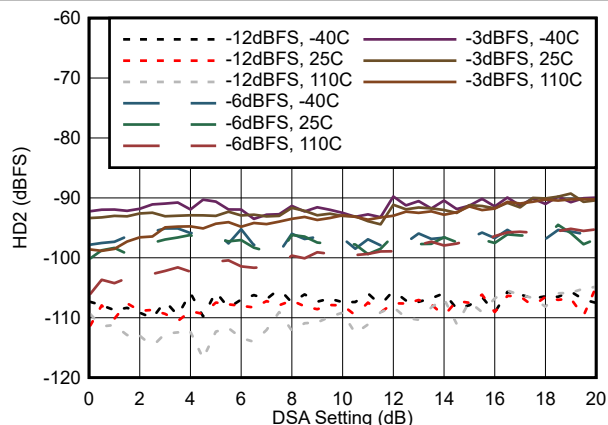
$f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x

Figure 7-24. IMD3 vs DSA Setting at 30 MHz



$f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x

Figure 7-25. HD2 vs Input Amplitude at 30 MHz



$f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.$, Decimate by 24x

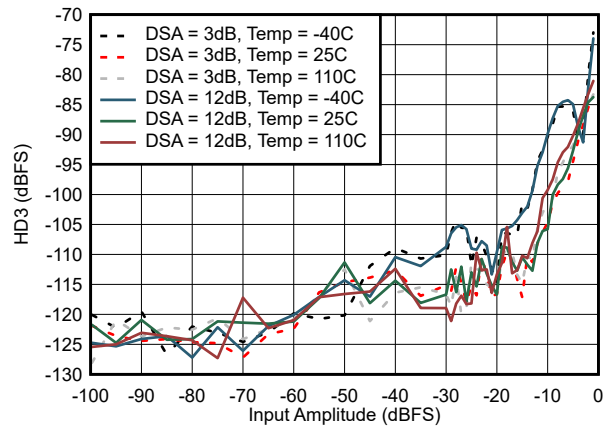
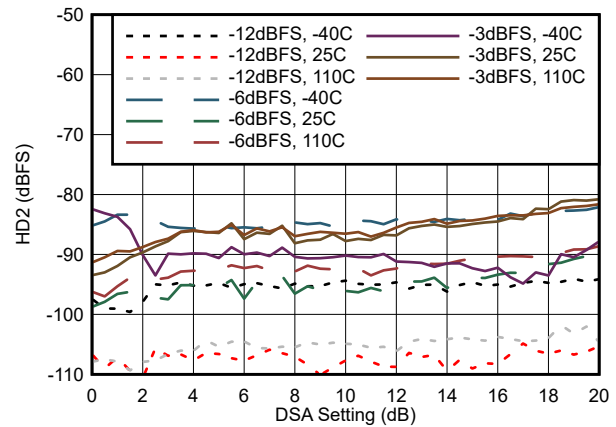
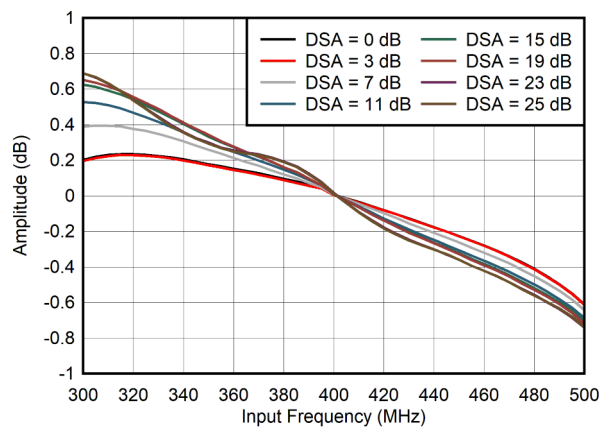
Figure 7-26. HD2 vs DSA Setting at 30 MHz

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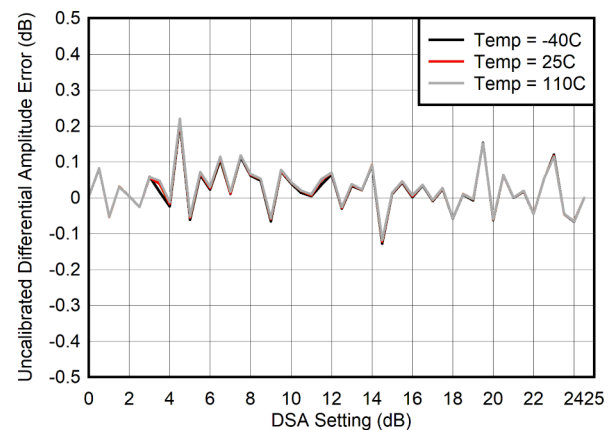
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7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.

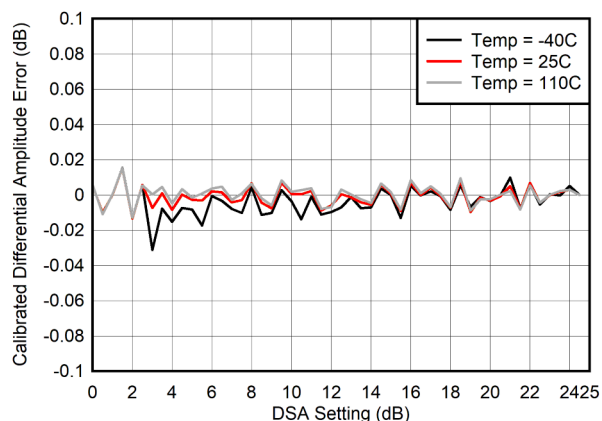

 $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x
Figure 7-27. HD3 vs Input Amplitude at 30 MHz
 $f_{\text{ADC}} = 1500\text{ MSPS}$, $f_{\text{NCO}} = 32.13\text{ MHz}$, Decimate by 24x
Figure 7-28. HD3 vs DSA Setting at 30 MHz

Normalized to 4000 MHz

Figure 7-29. RX In-Band Gain Flatness, $f_{\text{IN}} = 400\text{ MHz}$ 
 $\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$
Figure 7-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz

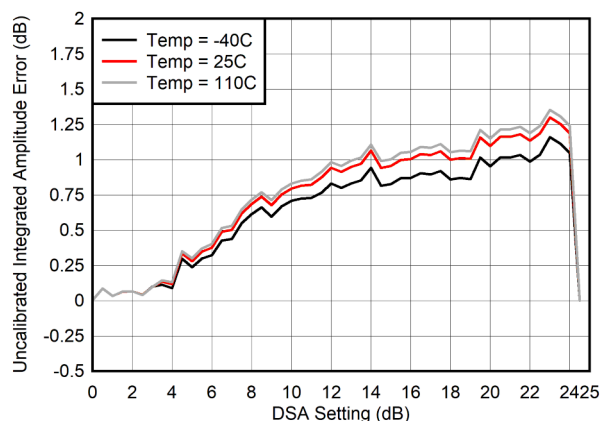
7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.



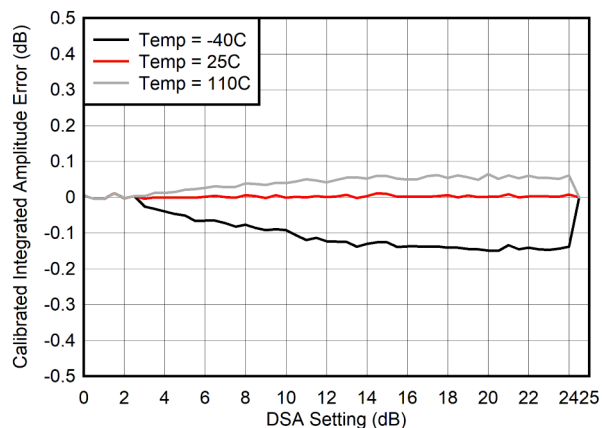
$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

Figure 7-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400 MHz



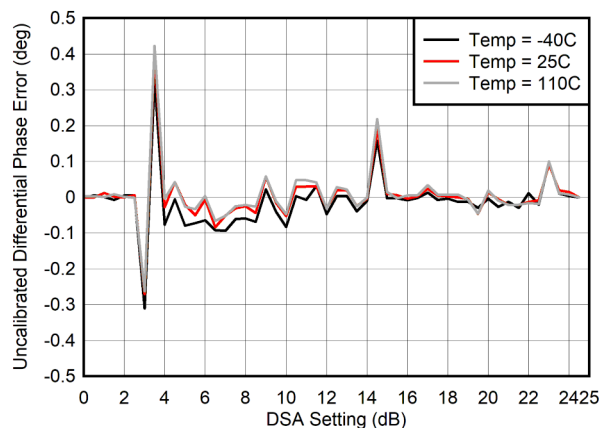
$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

Figure 7-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400 MHz



$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

Figure 7-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400 MHz



$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

Figure 7-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400 MHz

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7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.

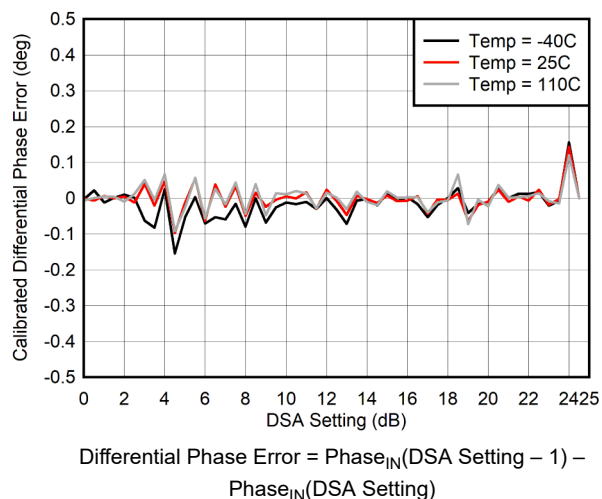


Figure 7-35. RX Calibrated Differential Phase Error vs DSA Setting at 400 MHz

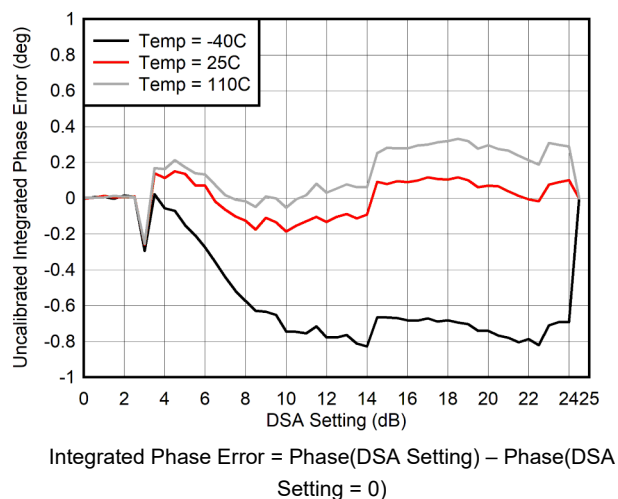


Figure 7-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400 MHz

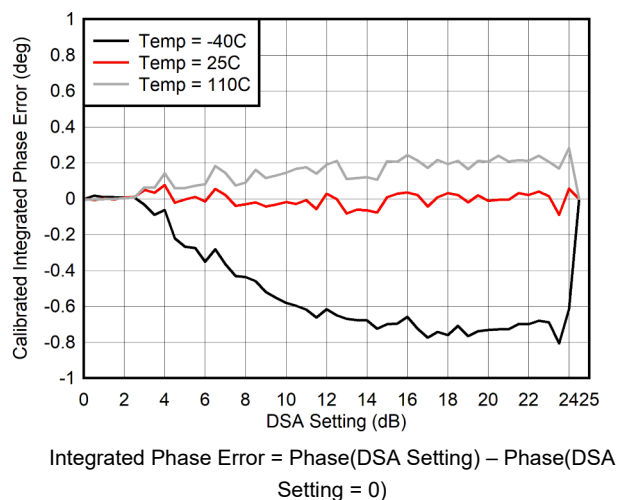


Figure 7-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400 MHz

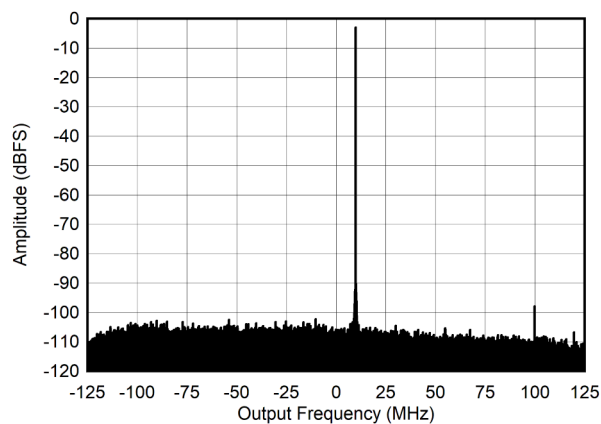
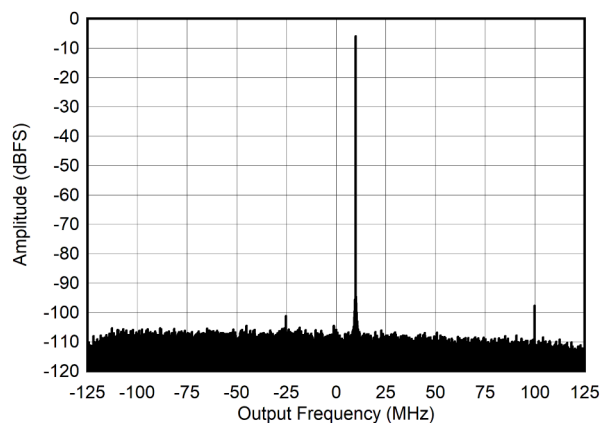


Figure 7-38. RX Output FFT at 405 MHz and -3dBFS

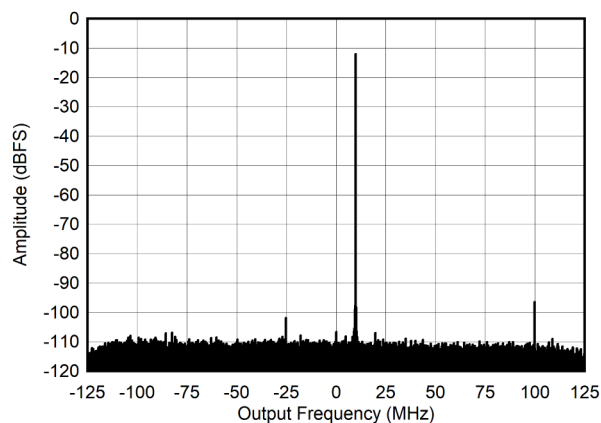
7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.



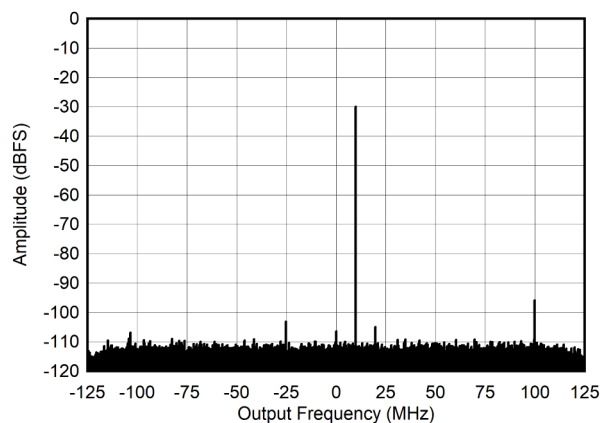
$f_{\text{NCO}} = 400\text{MHz}$

Figure 7-39. RX Output FFT at 405 MHz and -6dBFS



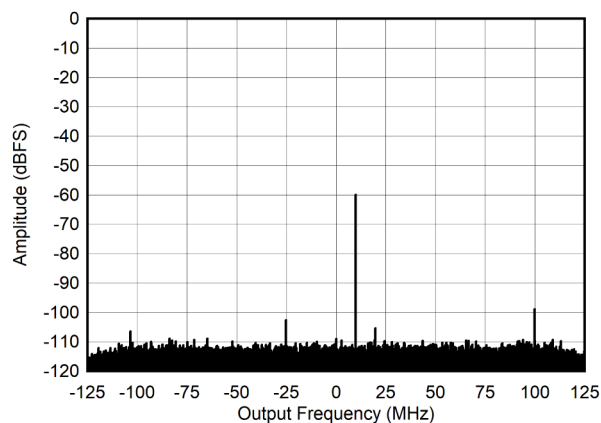
$f_{\text{NCO}} = 400\text{MHz}$

Figure 7-40. RX Output FFT at 405 MHz and -12dBFS



$f_{\text{NCO}} = 400\text{MHz}$

Figure 7-41. RX Output FFT at 405 MHz and -30dBFS



$f_{\text{NCO}} = 400\text{MHz}$

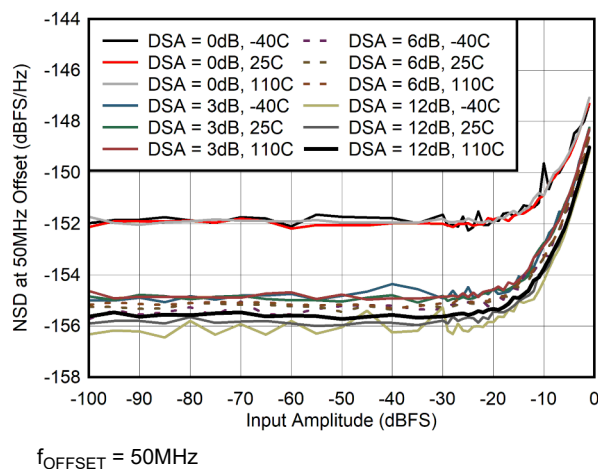
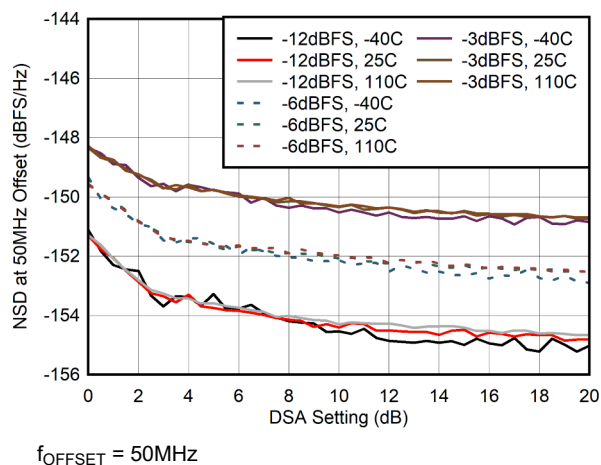
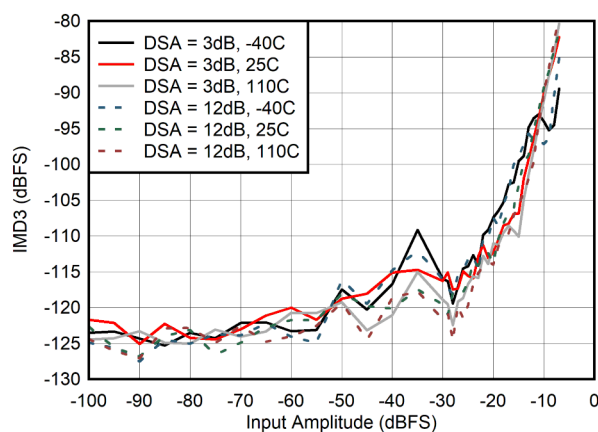
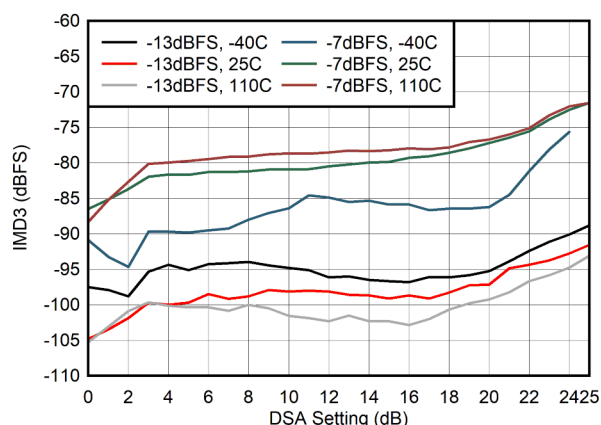
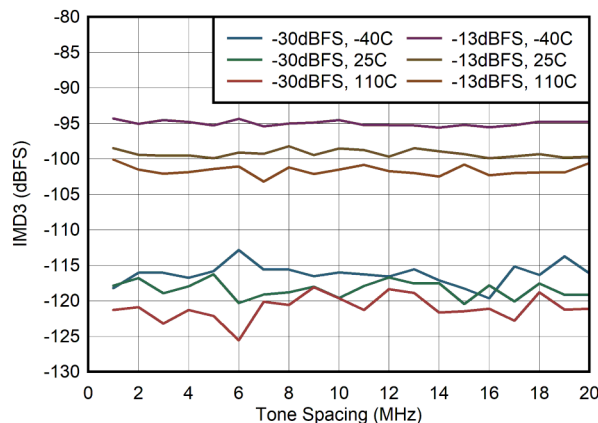
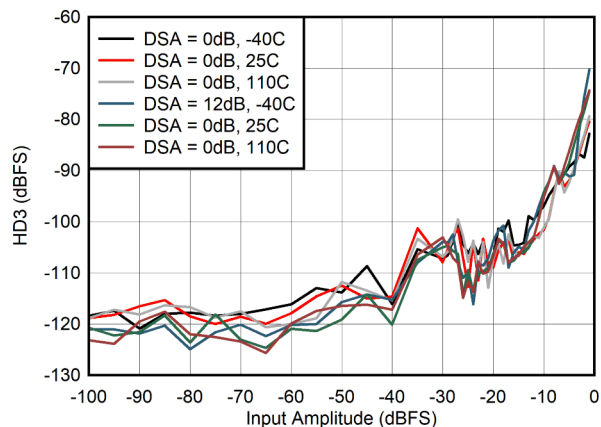
Figure 7-42. RX Output FFT at 405 MHz and -60dBFS

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7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB.

**Figure 7-43. NSD vs Input Amplitude at 400MHz****Figure 7-44. NSD vs DSA Setting at 400MHz****Figure 7-45. IMD3 vs Input Amplitude at 400MHz****Figure 7-46. IMD3 vs DSA Setting at 400MHz****Figure 7-47. IMD3 vs Tone Spacing at 400MHz****Figure 7-48. HD3 vs Input Amplitude at 400MHz**

7.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with $f_{\text{REF}} = 500$ MHz, $A_{\text{IN}} = -3$ dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with $f_{\text{REF}} = 500$ MHz, $A_{\text{IN}} = -3$ dBFS, DSA setting = 3 dB.

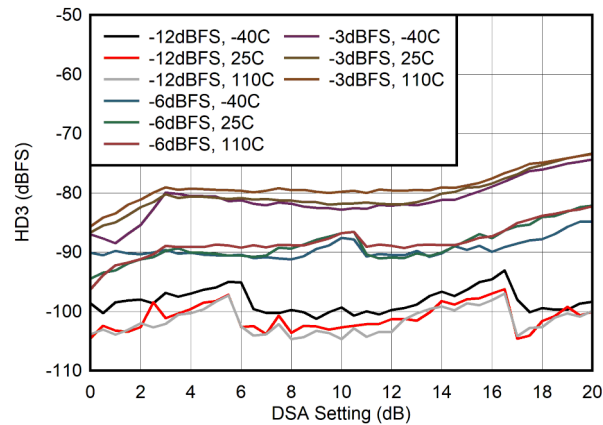


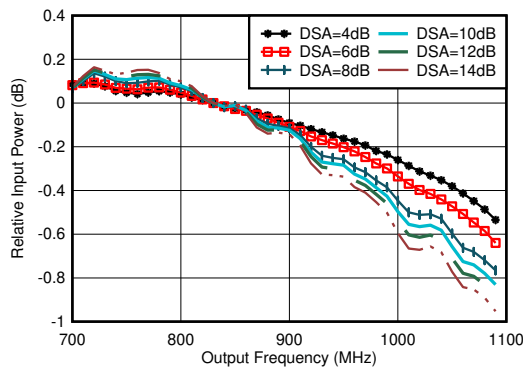
Figure 7-49. HD3 vs DSA Setting at 400MHz

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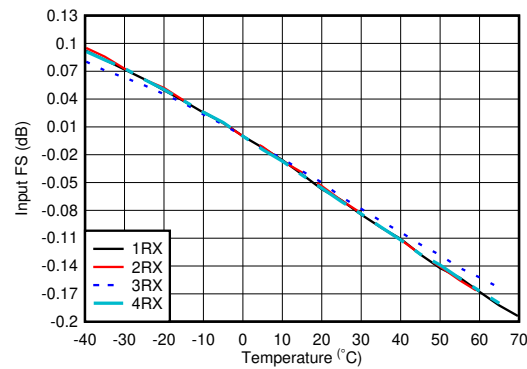
7.12.2 RX Typical Characteristics at 800MHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



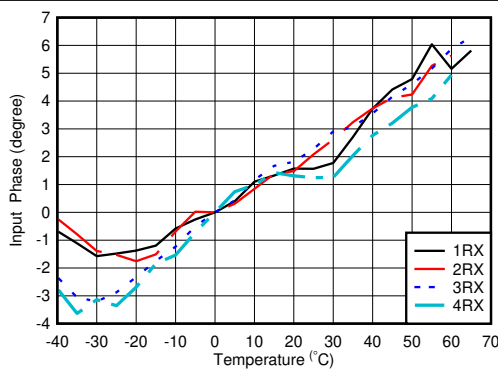
With 0.8 GHz matching, normalized to 830 MHz

Figure 7-50. RX In-Band Gain Flatness for Channel 1RX, $f_{\text{IN}} = 830\text{ MHz}$



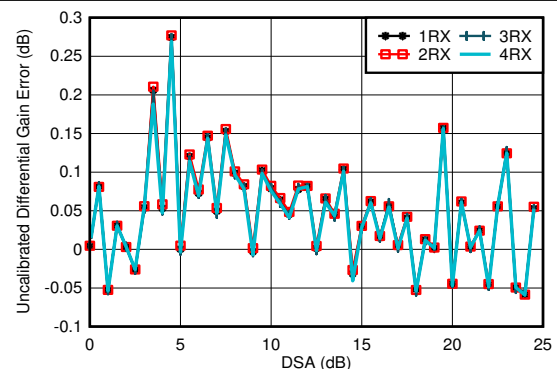
With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 7-51. RX Input Fullscale vs Temperature and Channel at 800MHz



With 0.8 GHz matching, normalized to phase at 25°C

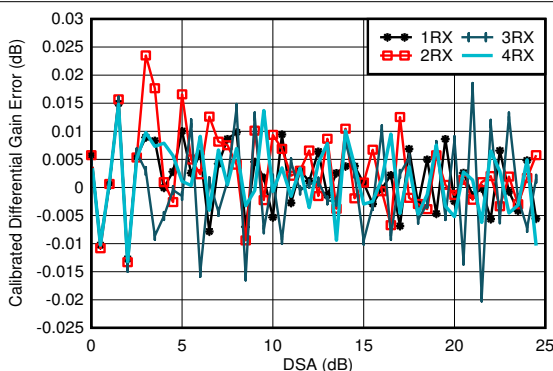
Figure 7-52. RX Input Phase vs Temperature and DSA at $f_{\text{OUT}} = 0.8\text{ GHz}$



With 0.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

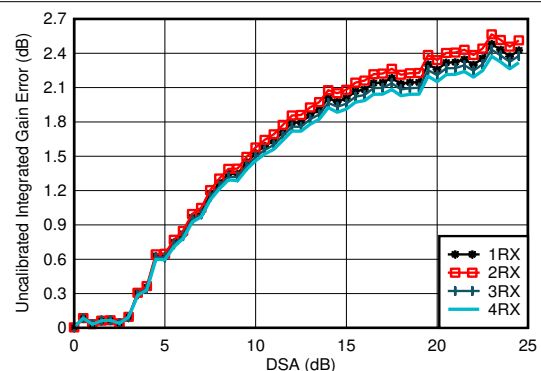
Figure 7-53. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-54. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



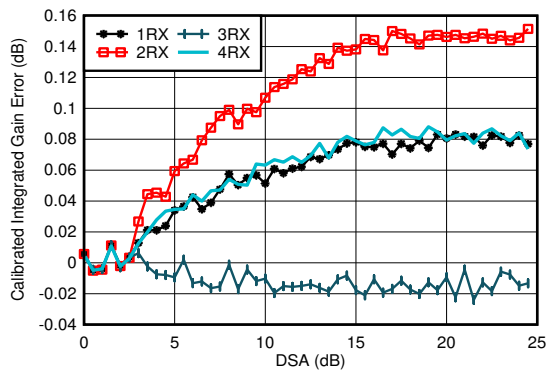
With 0.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-55. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz

7.12.2 RX Typical Characteristics at 800MHz (continued)

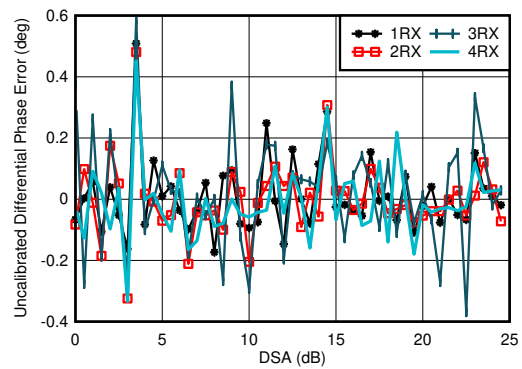
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

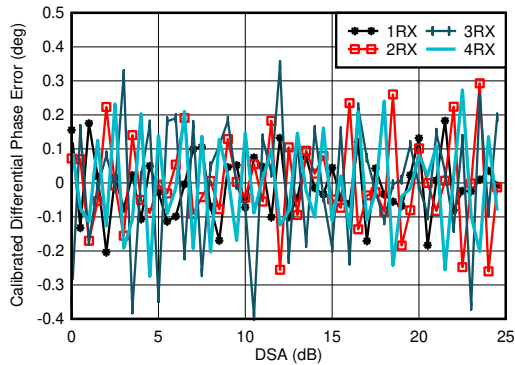
Figure 7-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 0.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

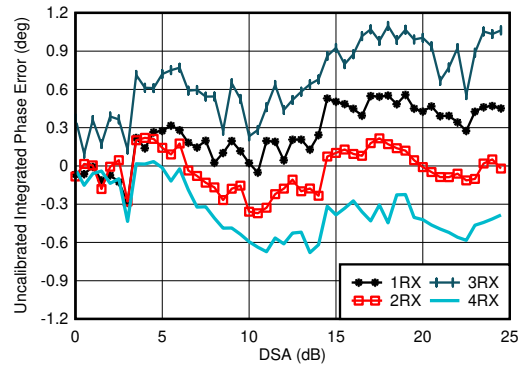
Figure 7-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

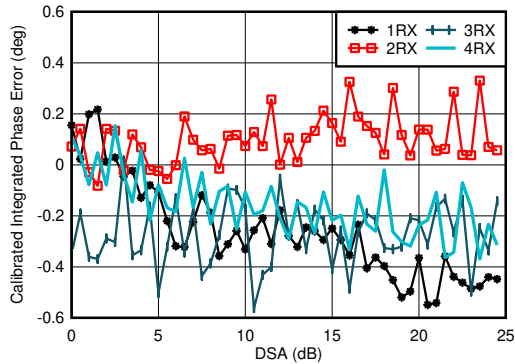
Figure 7-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

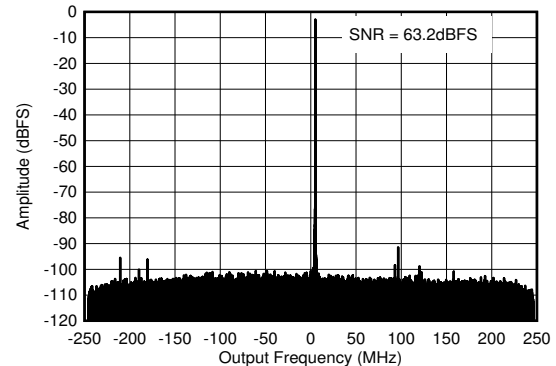
Figure 7-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-60. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching, $f_{\text{IN}} = 840\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$

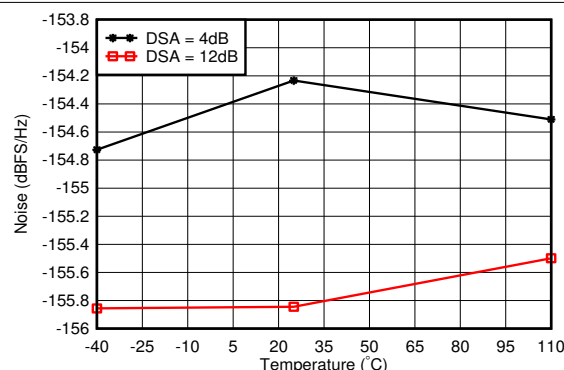
Figure 7-61. RX Output FFT at 0.8 GHz

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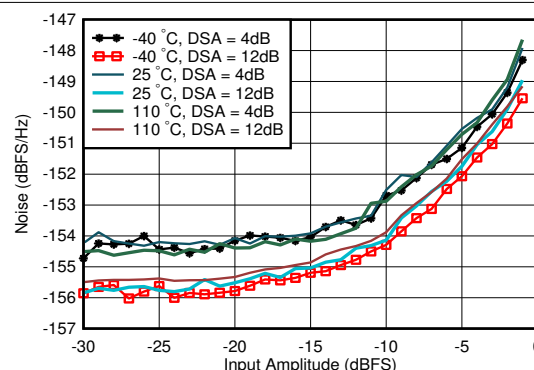
7.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



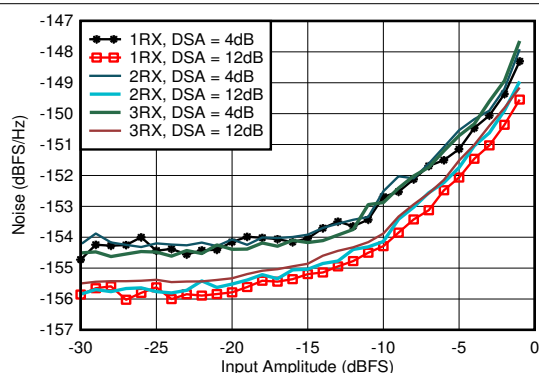
With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 7-62. RX Noise Spectral Density vs Temperature at 0.8 GHz



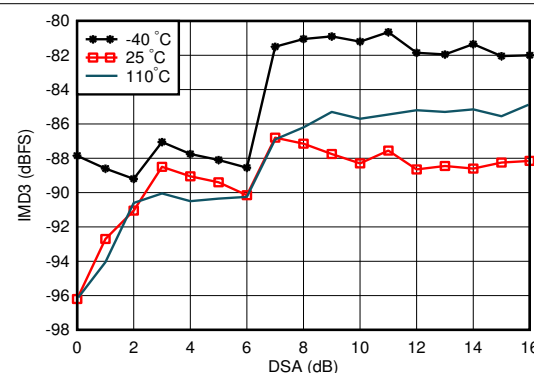
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 7-63. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



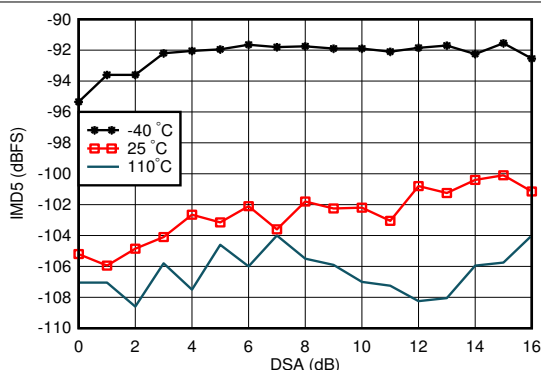
With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 7-64. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



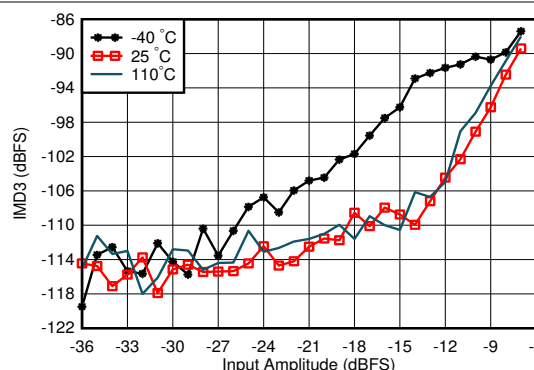
A. With 0.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-65. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-66. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz

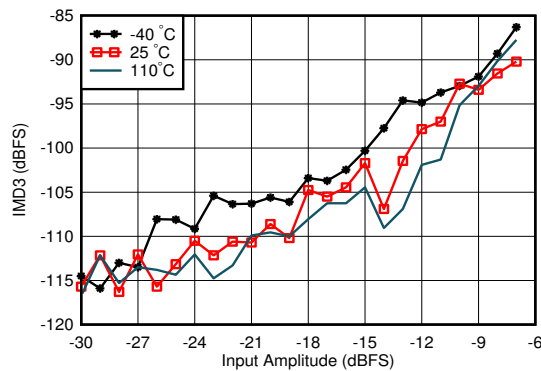


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-67. RX IMD3 vs Input Level and Temperature at 0.8 GHz

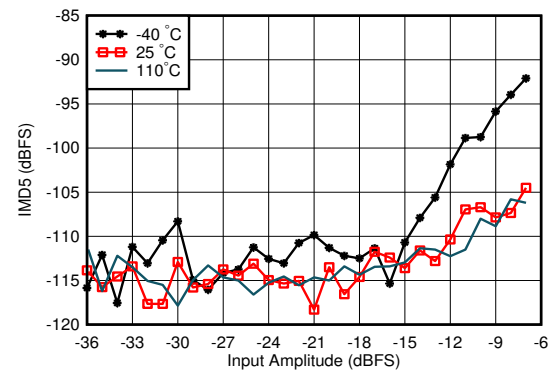
7.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



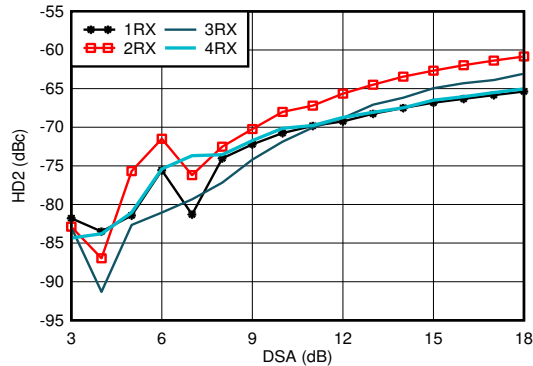
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-68. RX IMD3 vs Input Level and Temperature at 0.8 GHz



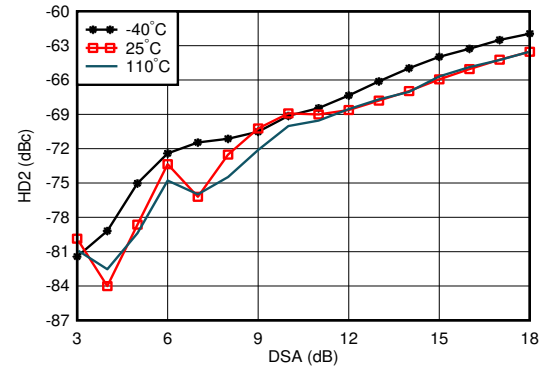
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-69. RX IMD5 vs Input Level and Temperature at 0.8 GHz



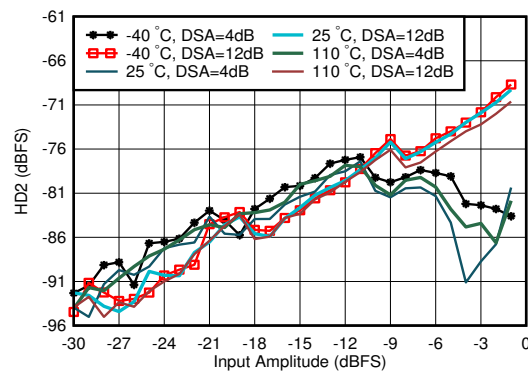
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-70. RX HD2 vs DSA Setting and Channel at 0.8 GHz



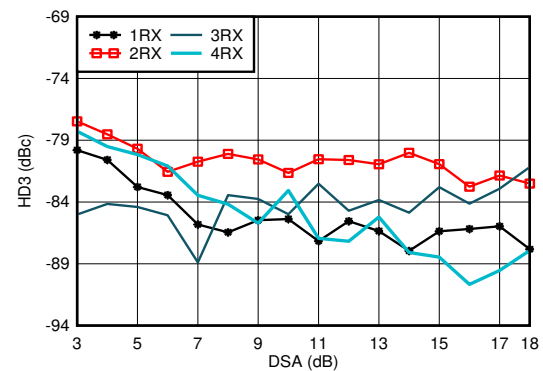
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-71. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-72. RX HD2 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

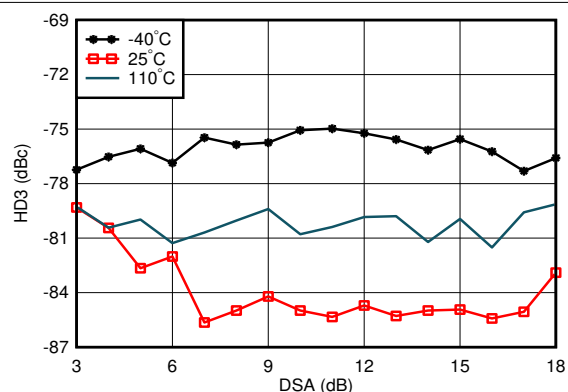
Figure 7-73. RX HD3 vs DSA Setting and Channel at 0.8 GHz

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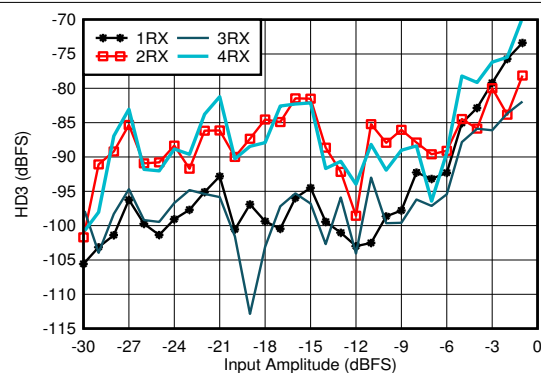
7.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



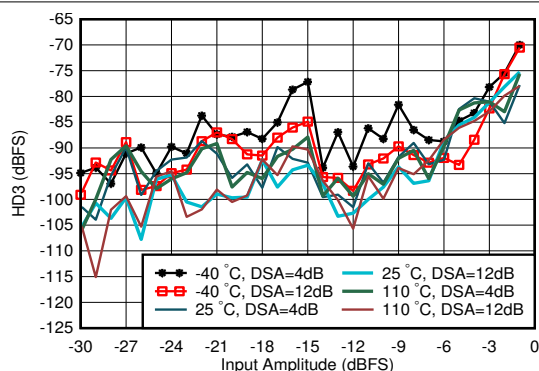
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-74. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



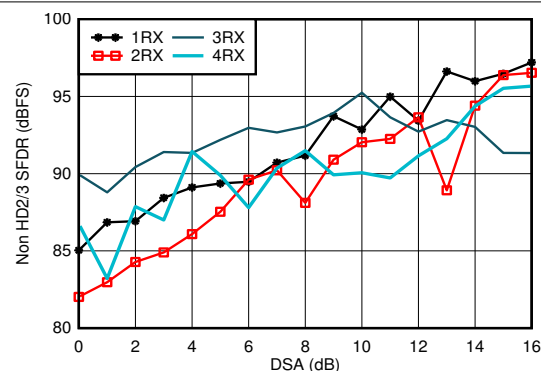
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-75. RX HD3 vs Input Level and Channel at 0.8 GHz



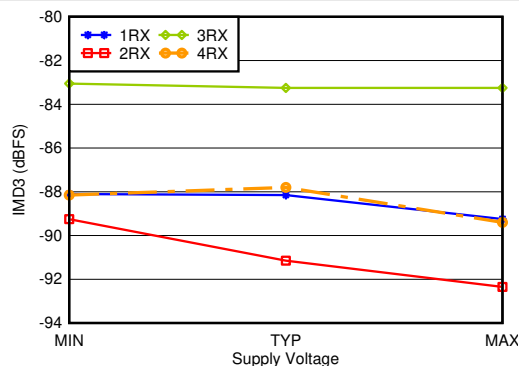
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-76. RX HD3 vs Input Level and Temperature at 0.8 GHz



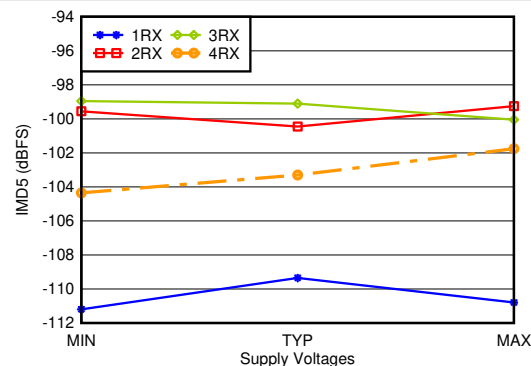
With 0.8 GHz matching

Figure 7-77. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-78. RX IMD3 vs Supply and Channel at 0.8 GHz

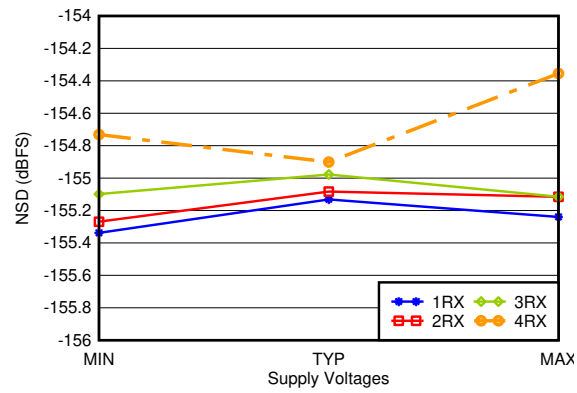


With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-79. RX IMD5 vs Supply and Channel at 0.8 GHz

7.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

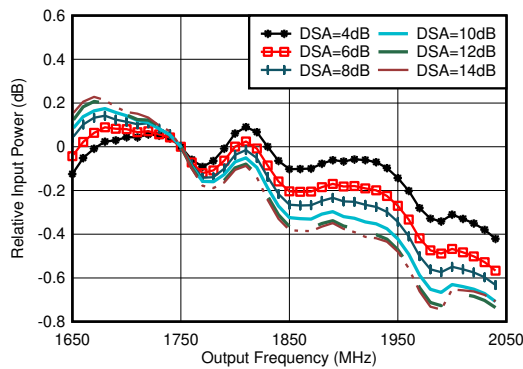
Figure 7-80. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

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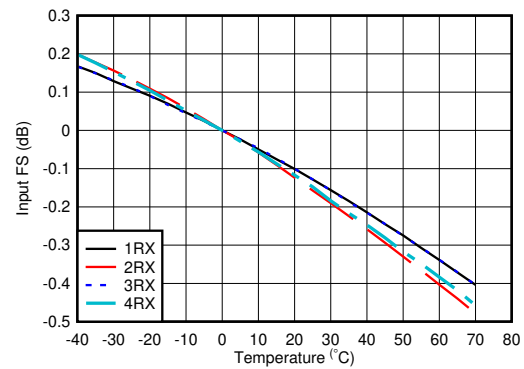
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7.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz

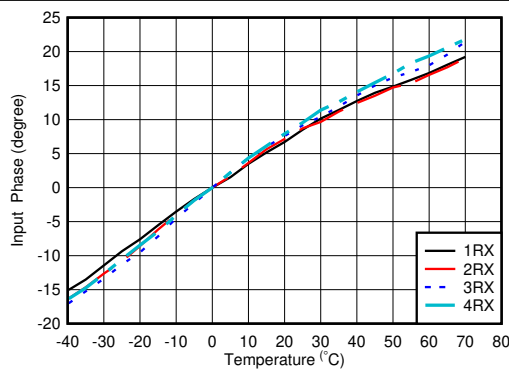
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



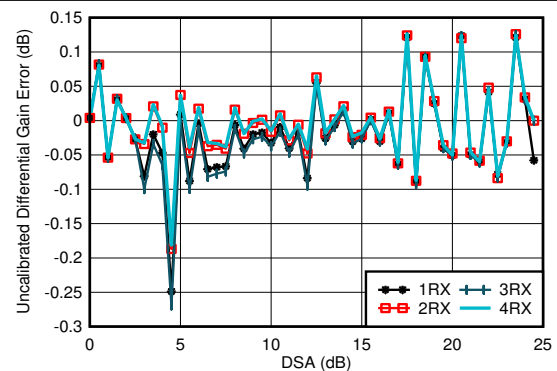
With 1.8 GHz matching, normalized to 1.75 GHz

Figure 7-81. RX In-Band Gain Flatness, $f_{\text{IN}} = 1750\text{ MHz}$ 

With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

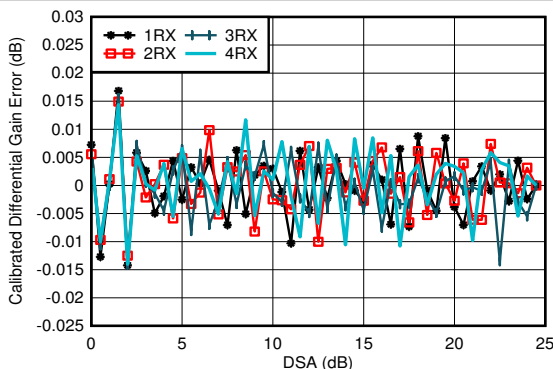
Figure 7-82. RX Input Fullscale vs Temperature and Channel at 1.75 GHz

With 2.6 GHz matching, normalized to phase at 25°C

Figure 7-83. RX Input Phase vs Temperature and DSA at $f_{\text{IN}} = 1.75\text{ GHz}$ 

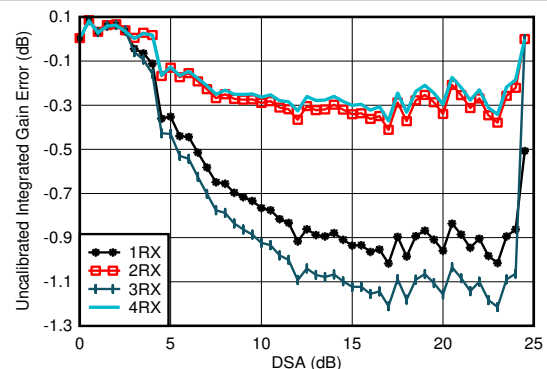
With 1.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz

With 1.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz

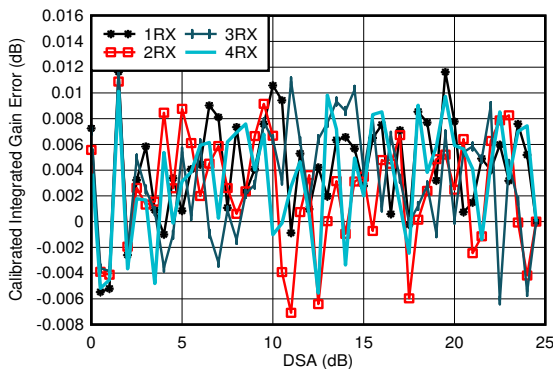
With 1.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

7.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

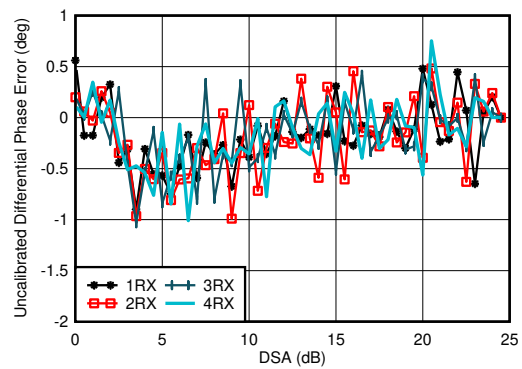
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{dBFS}$, DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

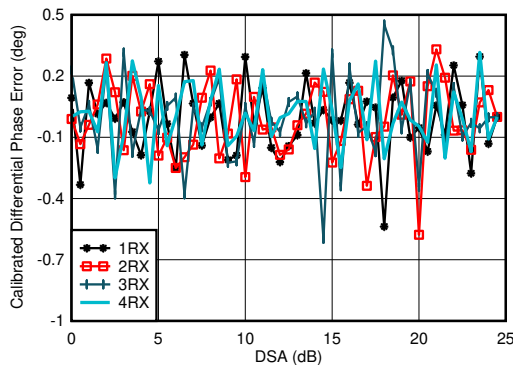
Figure 7-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

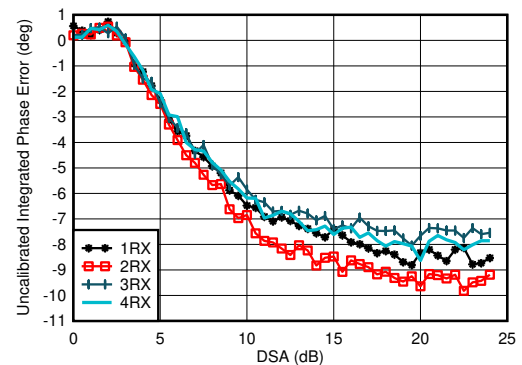
Figure 7-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

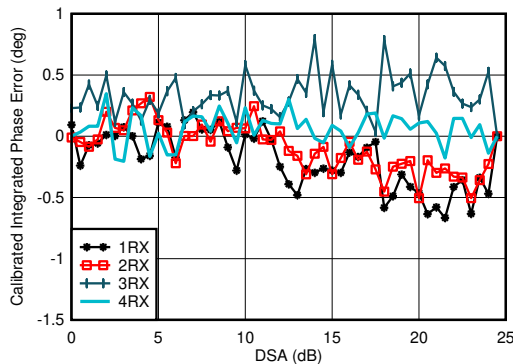
Figure 7-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

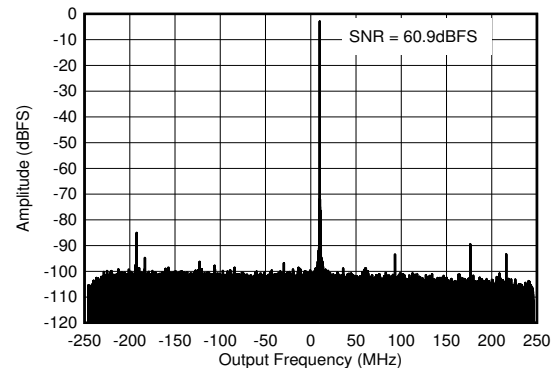
Figure 7-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-91. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

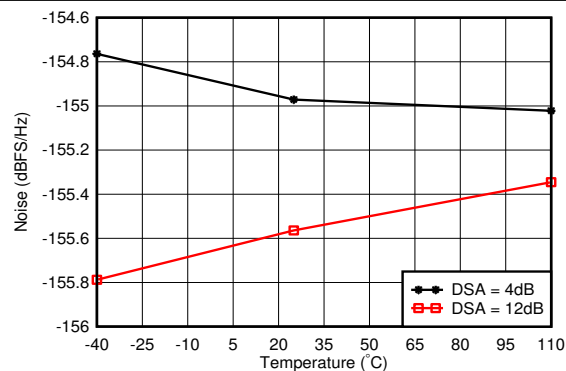


With 1.8 GHz matching, $f_{\text{IN}} = 2610\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$

Figure 7-92. RX Output FFT at 1.75 GHz

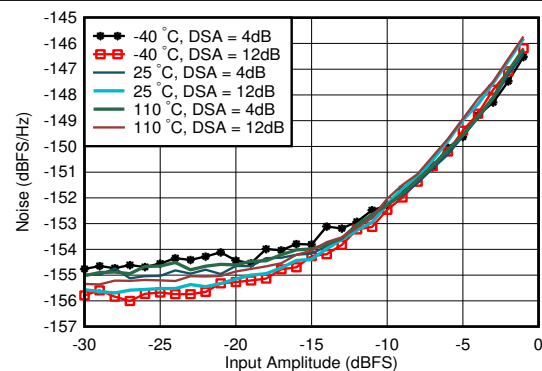
7.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



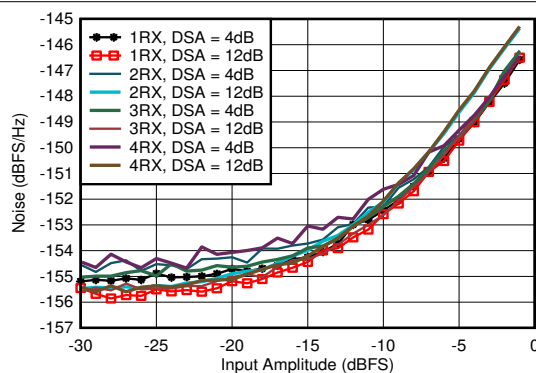
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 7-93. RX Noise Spectral Density vs Temperature at 1.75 GHz



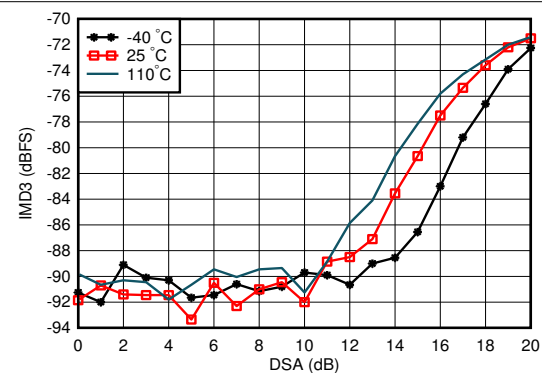
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 7-94. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



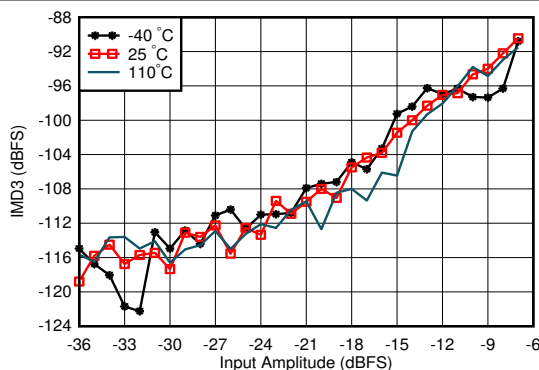
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 7-95. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



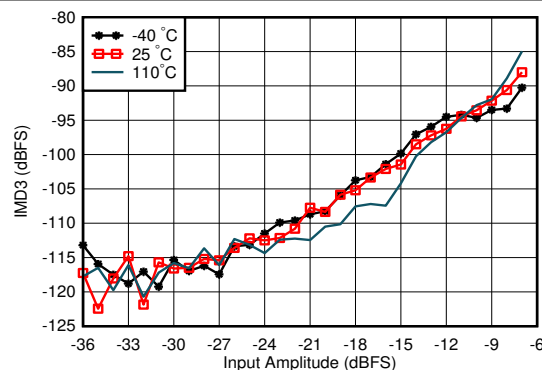
With 1.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-96. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-97. RX IMD3 vs Input Level and Temperature at 1.75 GHz

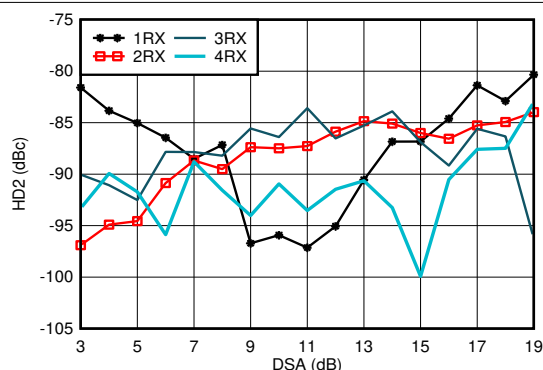


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-98. RX IMD3 vs Input Level and Temperature at 1.75 GHz

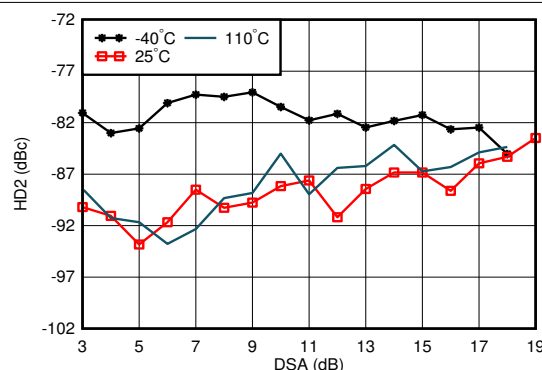
7.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



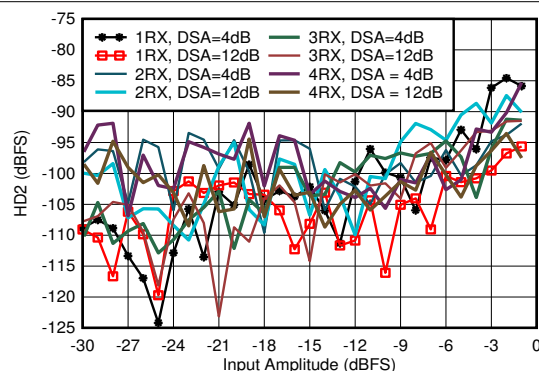
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-99. RX HD2 vs DSA Setting and Channel at 1.9 GHz



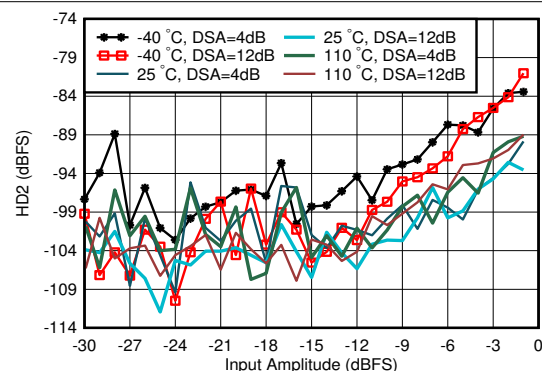
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-100. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



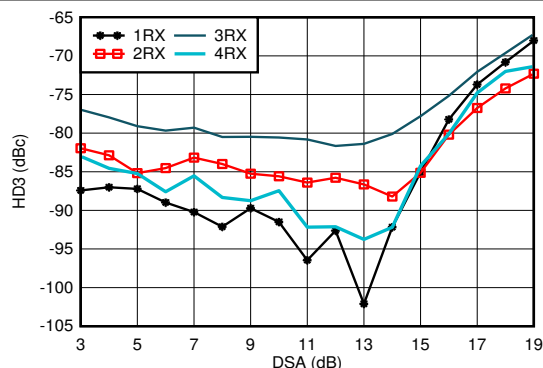
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-101. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



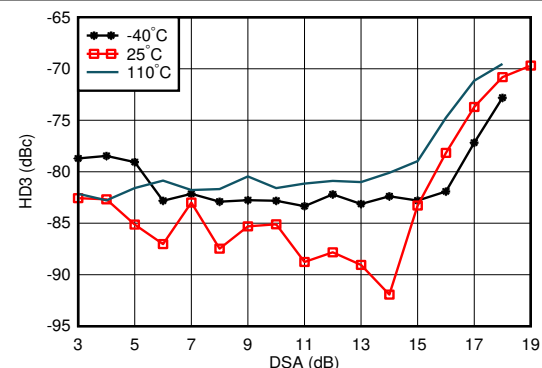
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-102. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz



With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, DDC bypass mode (TI only mode for characterization)

Figure 7-103. RX HD3 vs DSA Setting and Channel at 1.9 GHz



With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, DDC bypass mode (TI only mode for characterization)

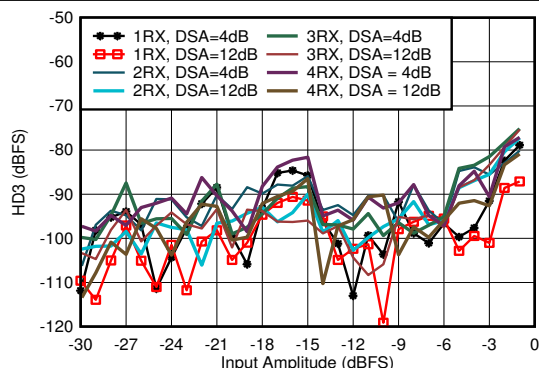
Figure 7-104. RX HD3 vs DSA Setting and Temperature at 1.9 GHz

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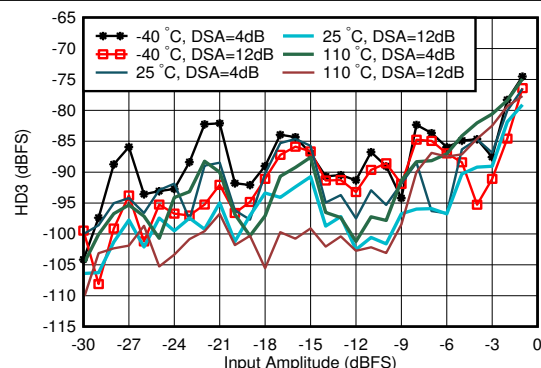
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7.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

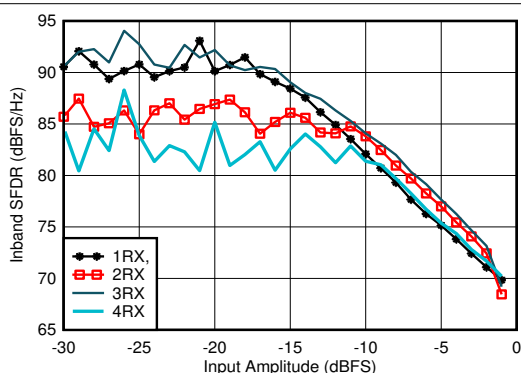
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



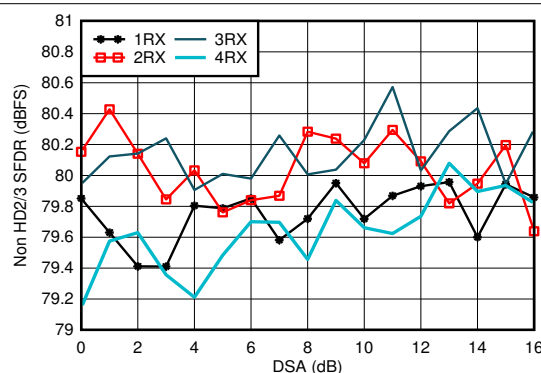
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, DDC bypass mode (TI only mode for characterization)

Figure 7-105. RX HD3 vs Input Level and Channel at 1.9 GHz

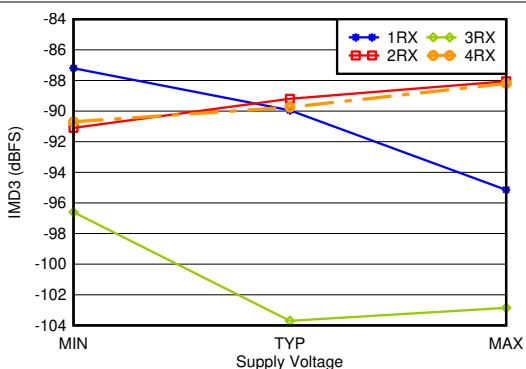
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{MHz}$, DDC bypass mode (TI only mode for characterization)

Figure 7-106. RX HD3 vs Input Level and Temperature at 1.9 GHz

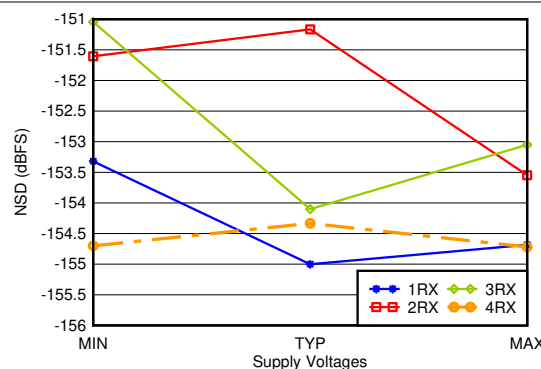
With 1.8 GHz matching, decimated by 3

Figure 7-107. RX In-Band SFDR ($\pm 400\text{ MHz}$) vs Input Amplitude at 1.75 GHz

With 1.8 GHz matching

Figure 7-108. RX Non-HD2/3 vs DSA Setting at 1.75 GHz

With 1.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

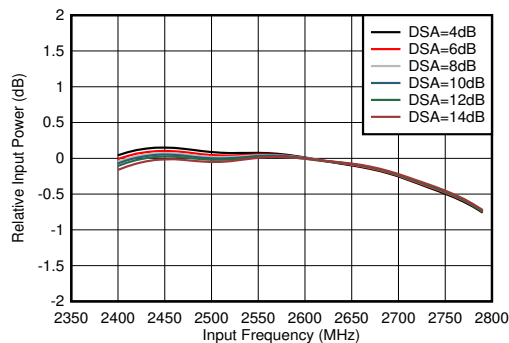
Figure 7-109. RX IMD3 vs Supply and Channel at 1.75 GHz

With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-110. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

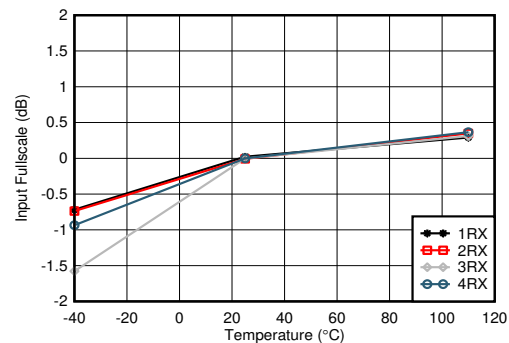
7.12.4 RX Typical Characteristics 2.6GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



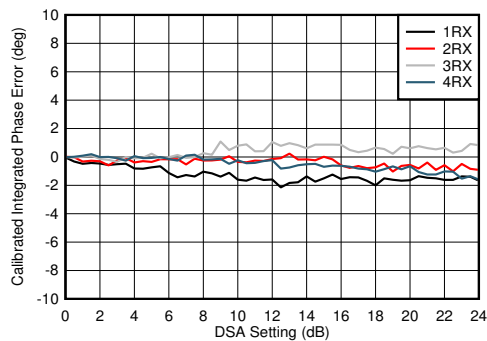
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 7-111. RX Inband Gain Flatness, $f_{\text{IN}} = 2600\text{ MHz}$



With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

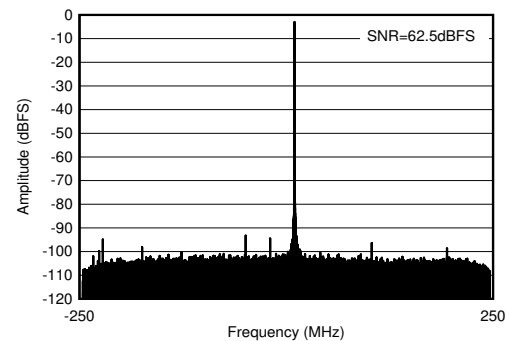
Figure 7-112. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



With 2.6 GHz matching

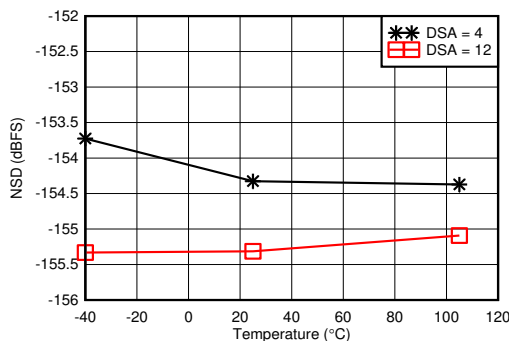
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



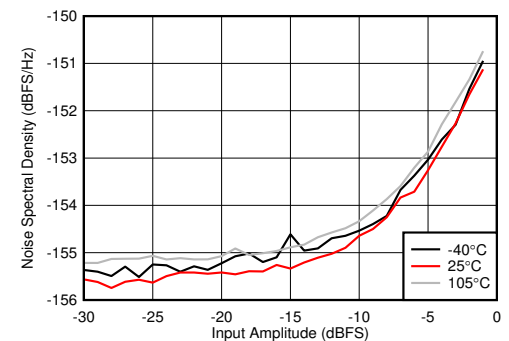
With 2.6 GHz matching, $f_{\text{IN}} = 2610\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$

Figure 7-114. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 7-115. RX Noise Spectral Density vs Temperature at 2.6 GHz



With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

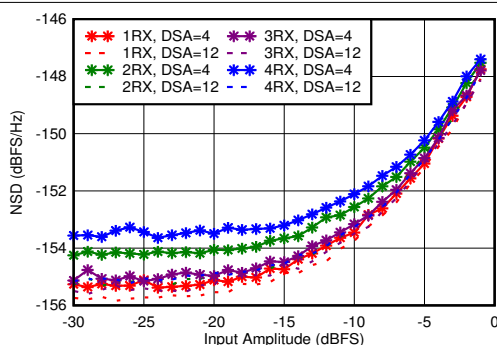
Figure 7-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

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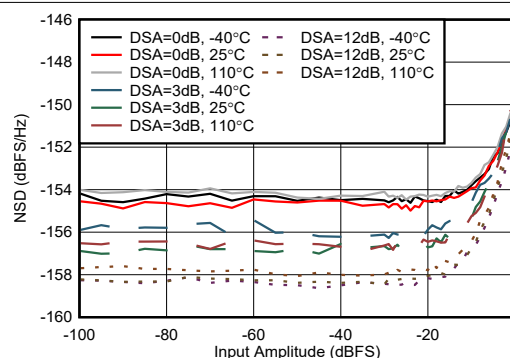
7.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



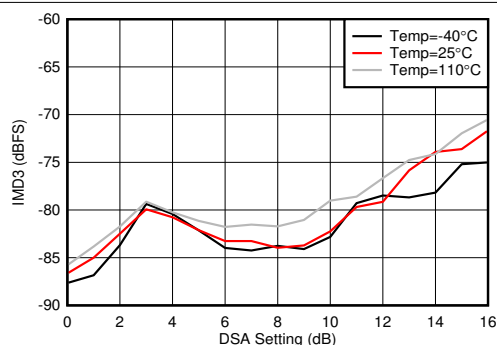
With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 7-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



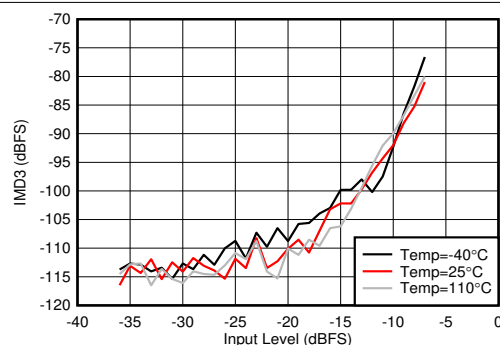
50-MHz offset from tone, external clock mode

Figure 7-118. RX Noise Spectral Density vs Input Amplitude at 2.61 GHz (Ext. Clock)



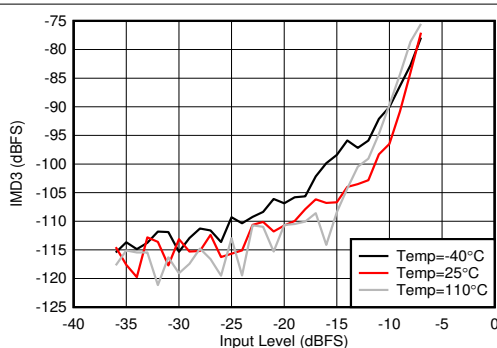
With 2.6 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-119. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



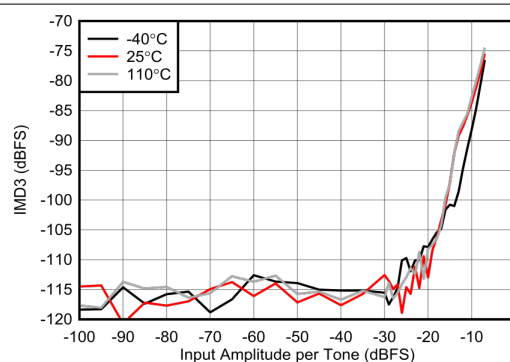
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-120. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-121. RX IMD3 vs Input Level and Temperature at 2.6 GHz

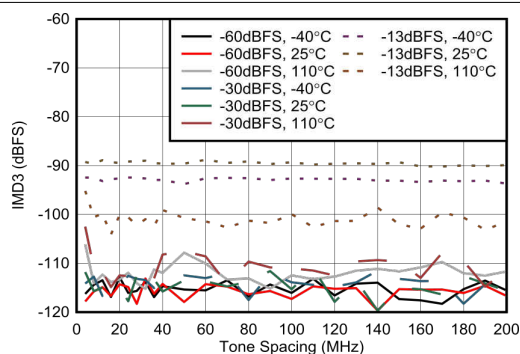


Tone spacing = 50 MHz, External clock mode

Figure 7-122. RX IMD3 vs Input Level at 2.6 GHz (Ext. Clock)

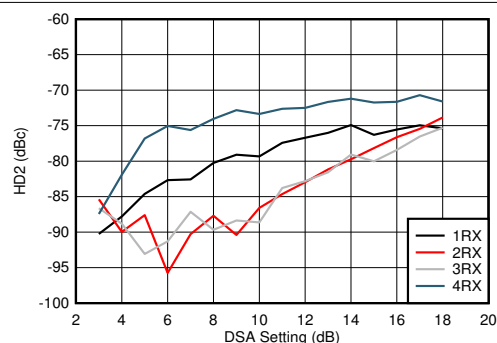
7.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



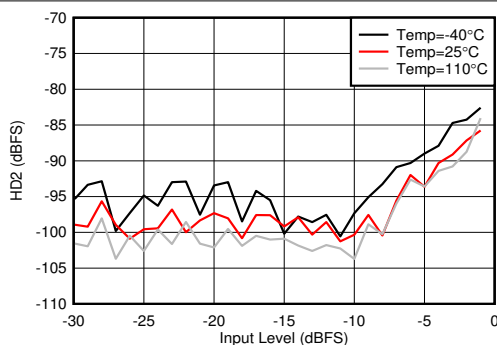
External clock mode

Figure 7-123. RX IMD3 vs Tone Spacing at 2.6 GHz (Ext. Clock)



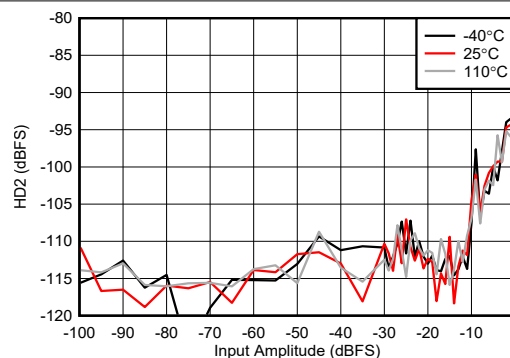
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-124. RX HD2 vs DSA Setting and Channel at 2.6 GHz



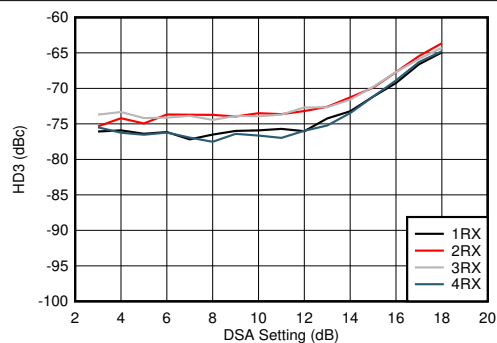
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-125. RX HD2 vs Input Level and Temperature at 2.6 GHz



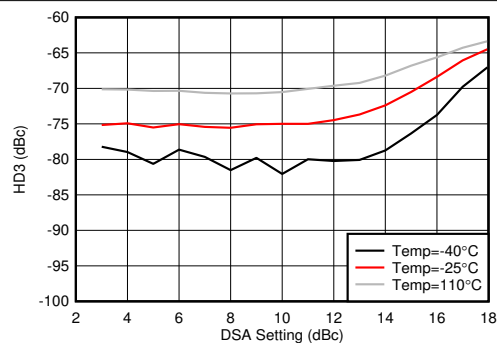
External clock mode

Figure 7-126. RX HD2 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-127. RX HD3 vs DSA Setting and Channel at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

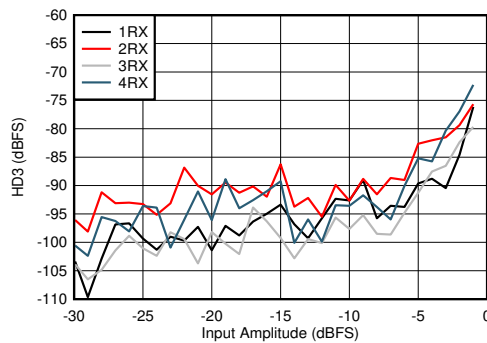
Figure 7-128. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

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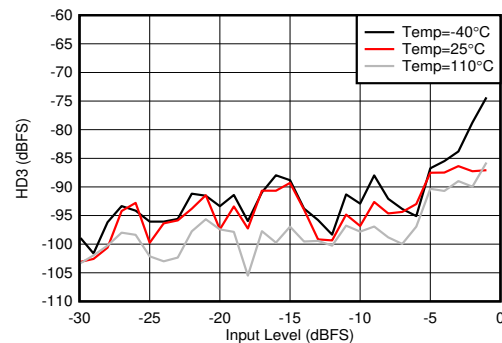
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7.12.4 RX Typical Characteristics 2.6GHz (continued)

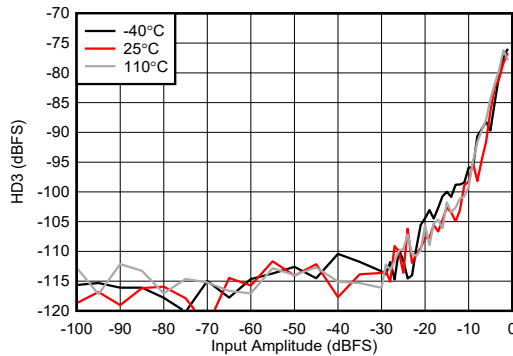
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



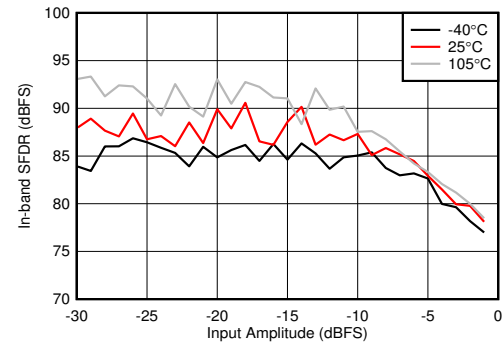
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-129. RX HD3 vs Input Level and Channel at 2.6 GHz

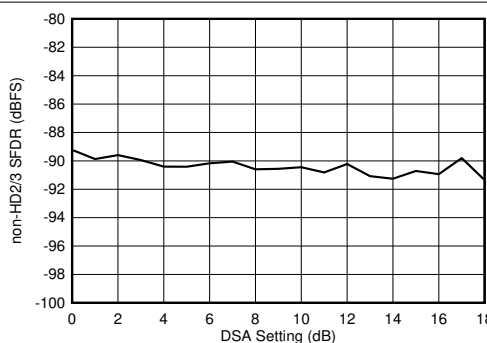
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-130. RX HD3 vs Input Level and Temperature at 2.6 GHz

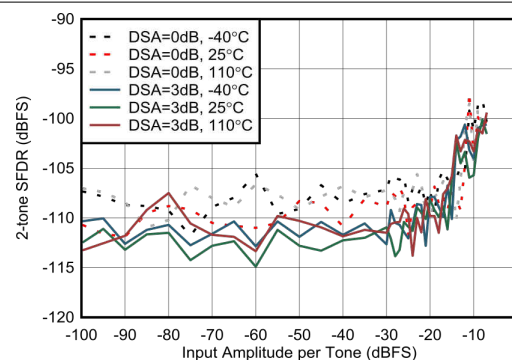
External clock mode

Figure 7-131. RX HD3 vs Input Level and Temperature at 2.6 GHz

With 2.6 GHz matching, decimate by 4

Figure 7-132. RX In-Band SFDR ($\pm 300\text{ MHz}$) vs Input Amplitude and Temperature at 2.6 GHz

With 2.6 GHz matching

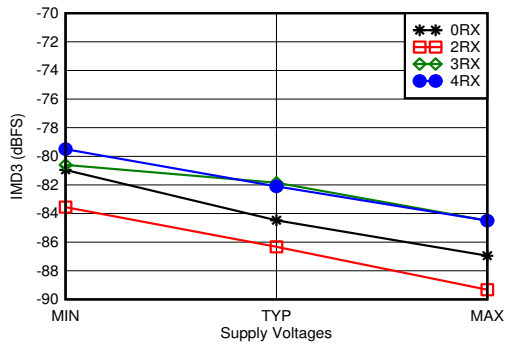
Figure 7-133. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

External clock mode, 50MHz tone spacing, excluding 3rd order distortion

Figure 7-134. RX 2-tone SFDR vs Input Amplitude at 2.6 GHz

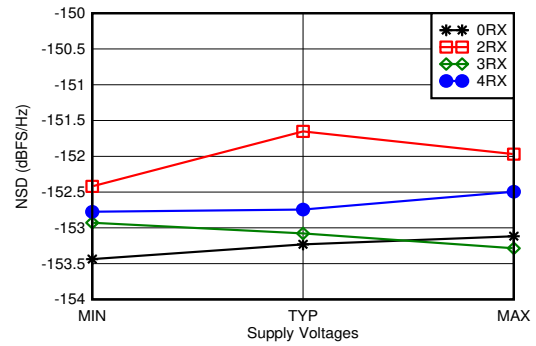
7.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 2.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-135. RX IMD3 vs Supply and Channel at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

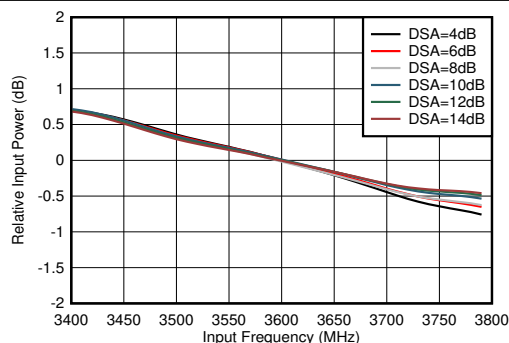
Figure 7-136. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

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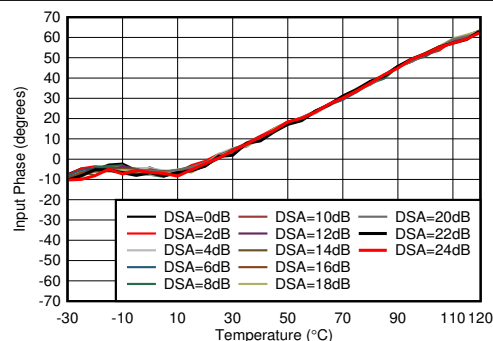
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7.12.5 RX Typical Characteristics 3.5GHz

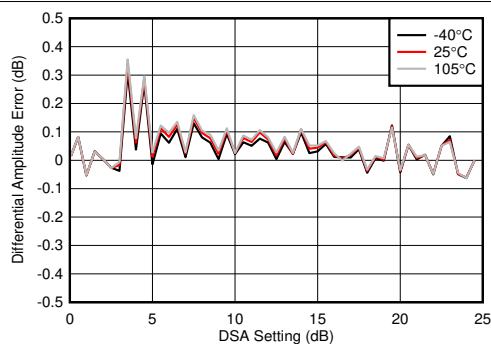
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 3.6 GHz matching, normalized to 3.6 GHz

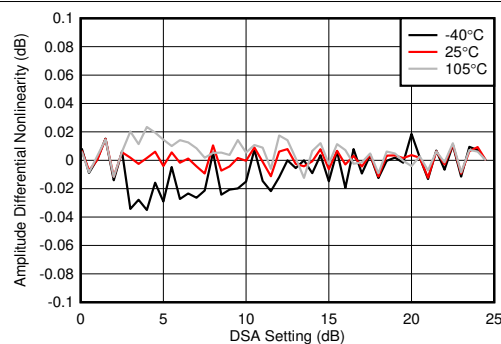
Figure 7-137. RX In-Band Gain Flatness, $f_{\text{IN}} = 3600\text{ MHz}$ 

With 3.6 GHz matching, normalized to phase at 25°C

Figure 7-138. RX Input Phase vs Temperature at 3.6 GHz

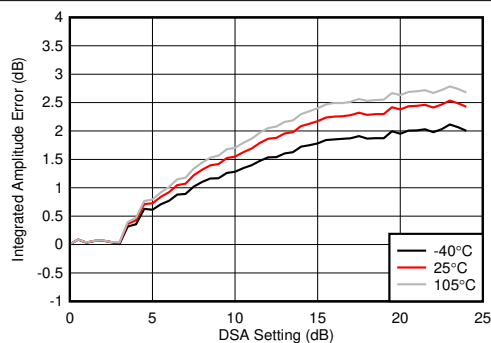
With 3.6 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-139. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz

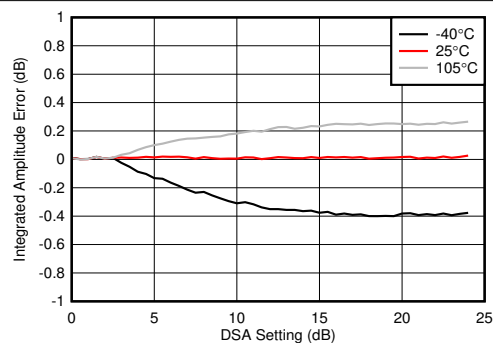
With 3.6 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-140. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz

With 3.6 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-141. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

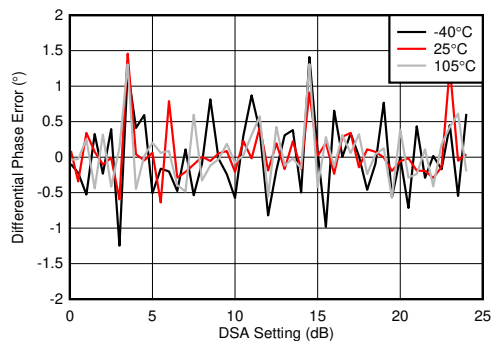
With 3.6 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-142. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

7.12.5 RX Typical Characteristics 3.5GHz (continued)

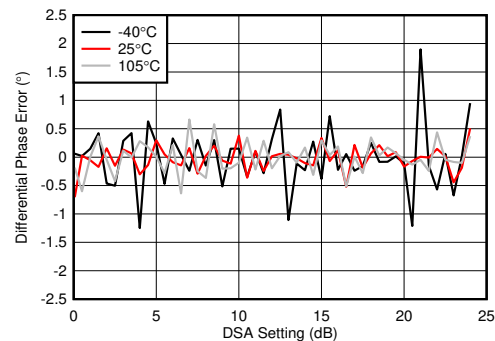
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

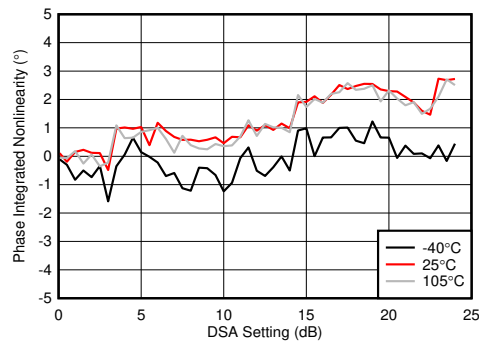
Figure 7-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

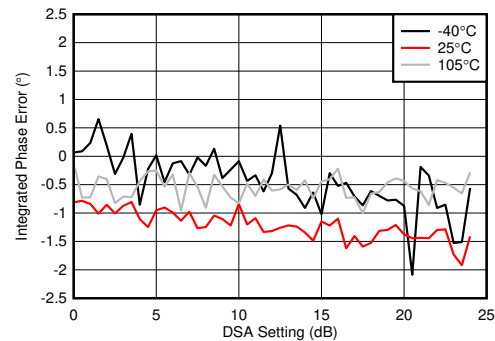
Figure 7-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

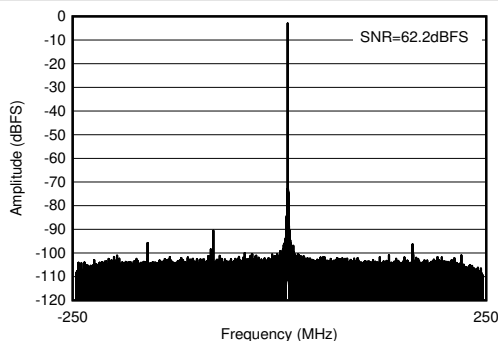
Figure 7-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

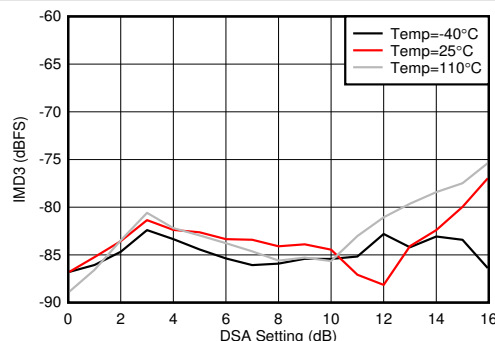
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

Figure 7-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching, $f_{\text{IN}} = 3610\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$

Figure 7-147. RX Output FFT at 3.6 GHz



With 3.5 GHz matching, each tone at -7 dBFS , 20-MHz tone spacing

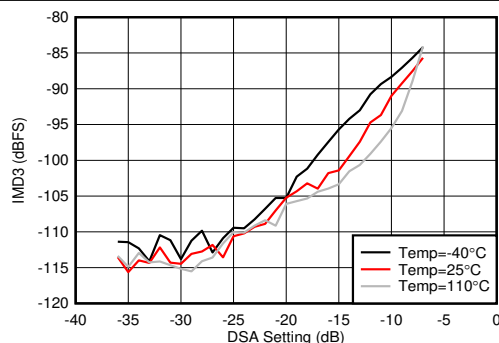
Figure 7-148. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

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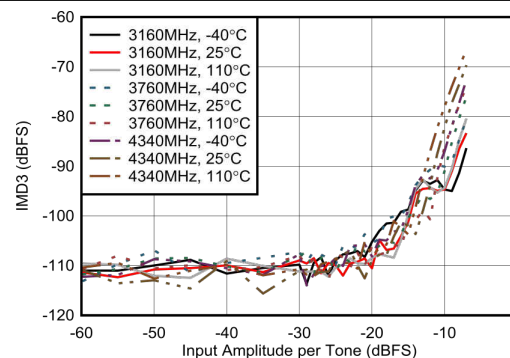
7.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



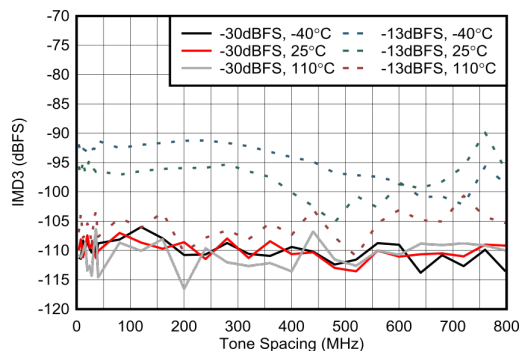
With 3.5 GHz matching, 20-MHz tone spacing

Figure 7-149. RX IMD3 vs Input Level and Temperature at 3.6 GHz



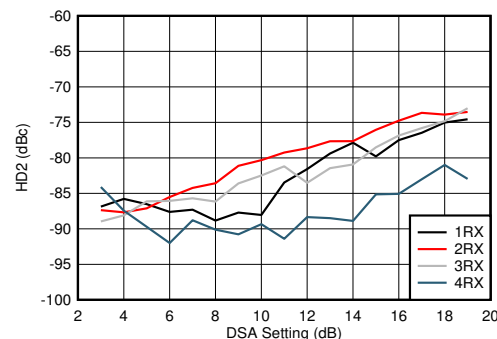
External clock mode, 20-MHz tone spacing, 2x Decimation

Figure 7-150. RX IMD3 vs Input Level



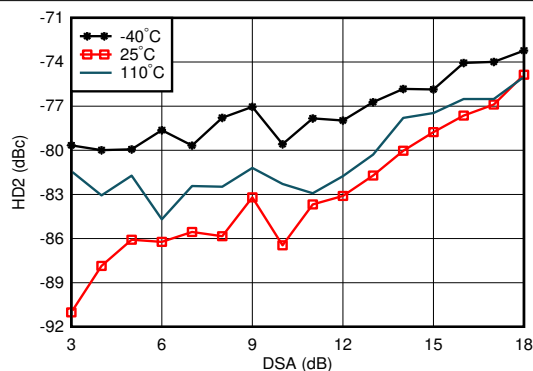
External clock mode, 2x Decimation

Figure 7-151. RX IMD3 vs Tone Spacing at 3.76GHz



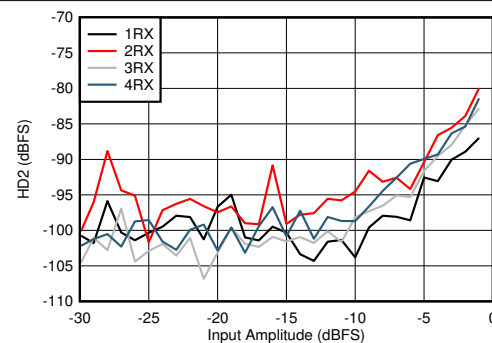
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-152. RX HD2 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-153. RX HD2 vs DSA Setting and Temperature at 3.6 GHz

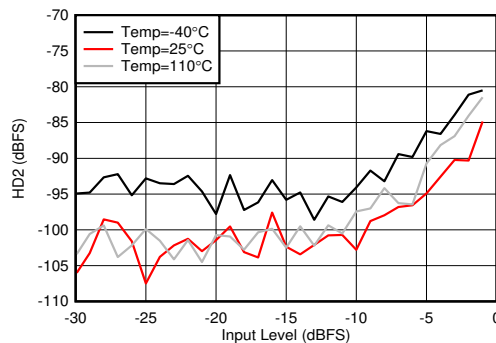


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-154. RX HD2 vs Input Level and Channel at 3.6 GHz

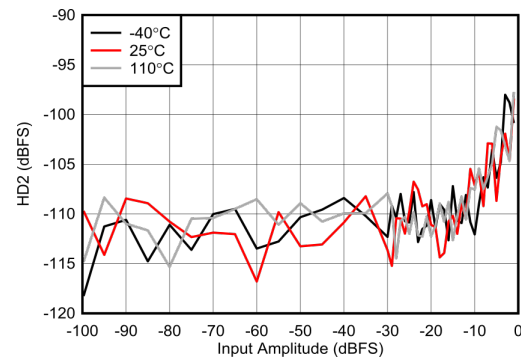
7.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



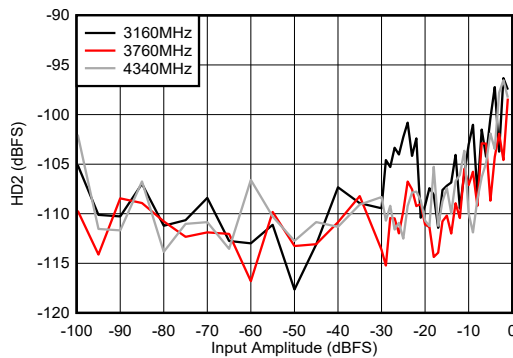
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-155. RX HD2 vs Input Level and Temperature at 3.6 GHz



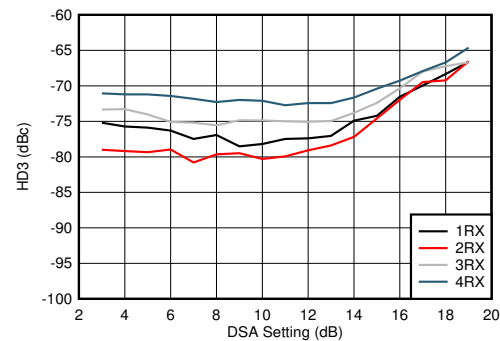
External clock mode, 2x Decimation

Figure 7-156. RX HD2 vs Input Level at 3.76 GHz



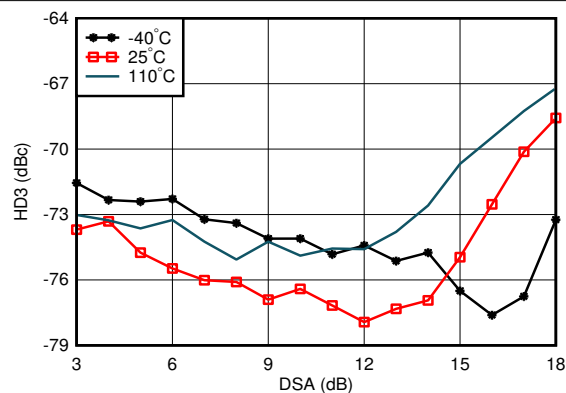
External clock mode, 25°C, 2x Decimation

Figure 7-157. RX HD2 vs Input Level



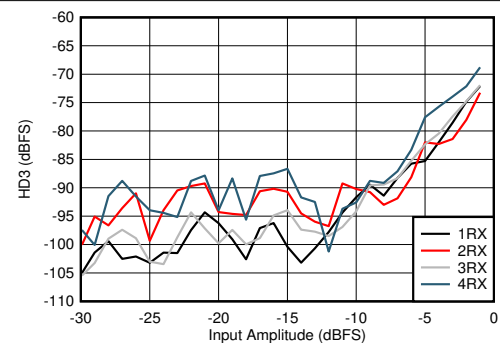
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-158. RX HD3 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-159. RX HD3 vs DSA Setting and Temperature at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

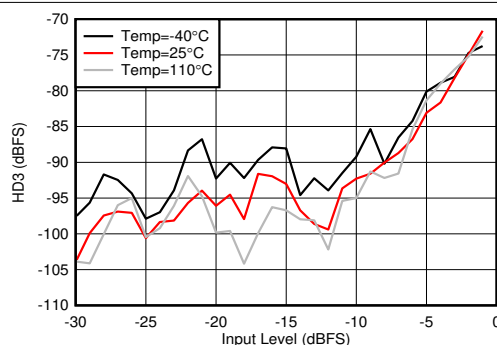
Figure 7-160. RX HD3 vs Input Level and Channel at 3.6 GHz

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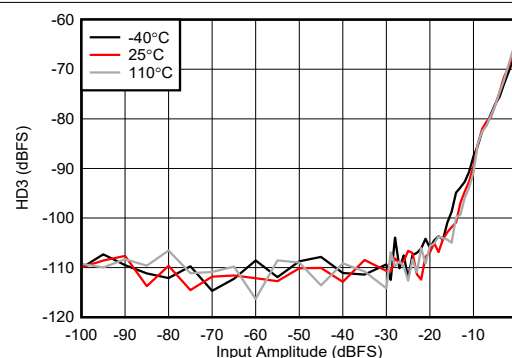
7.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



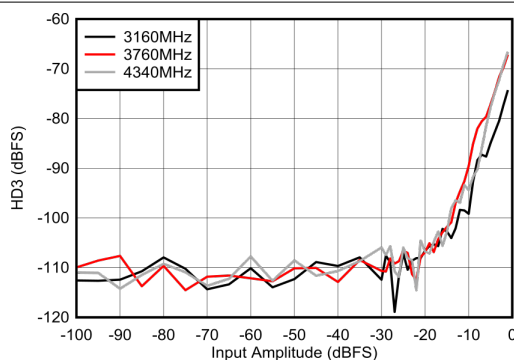
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-161. RX HD3 vs Input Level and Temperature at 3.6 GHz



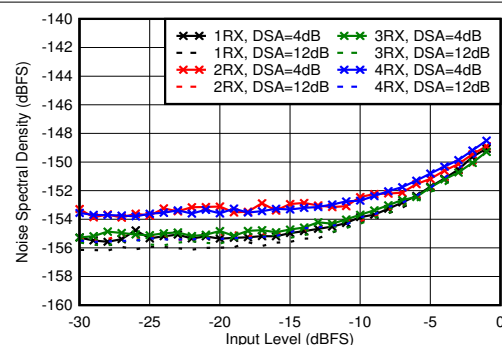
External clock mode, 2x Decimation

Figure 7-162. RX HD3 vs Input Level at 3.76GHz



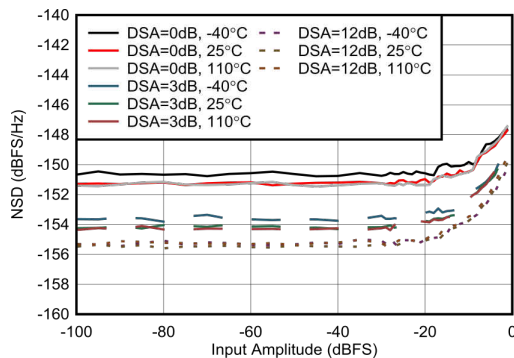
External clock mode, 25°C, 2x Decimation

Figure 7-163. RX HD3 vs Input Level



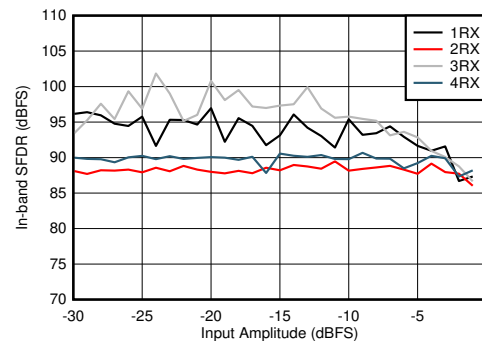
With 3.5 GHz matching, 12.5-MHz offset from tone

Figure 7-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



External clock mode, 25°C, 2x Decimation

Figure 7-165. RX Noise Spectral Density vs Input Level at 3.76GHz

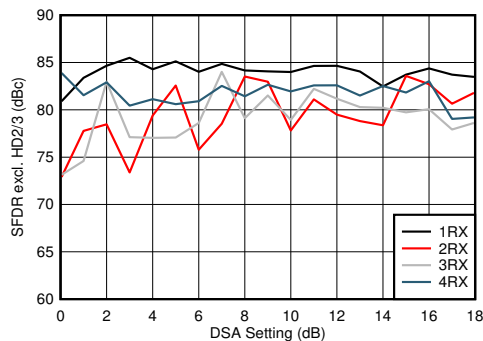


With 3.5 GHz matching

Figure 7-166. RX In-Band SFDR ($\pm 200\text{ MHz}$) vs Input Level and Channel at 3.6 GHz

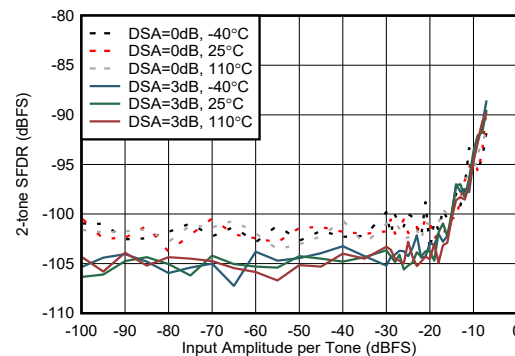
7.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



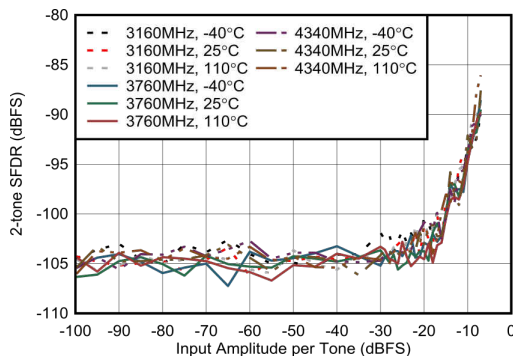
With 3.5 GHz matching

Figure 7-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz



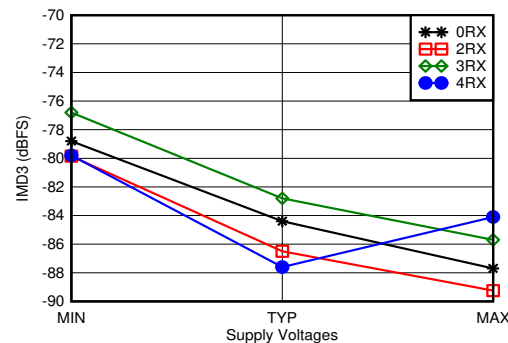
External clock mode, 20MHz tone spacing, excluding 3rd order distortion

Figure 7-168. RX 2-tone SFDR vs Input Amplitude and DSA Setting at 3.7 GHz



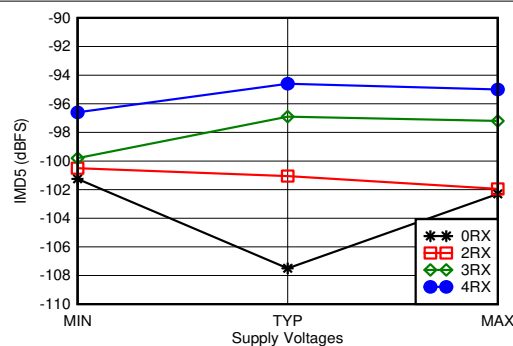
External clock mode, 20MHz tone spacing, excluding 3rd order distortion

Figure 7-169. RX 2-tone SFDR vs Input Amplitude and Frequency at 3.7 GHz



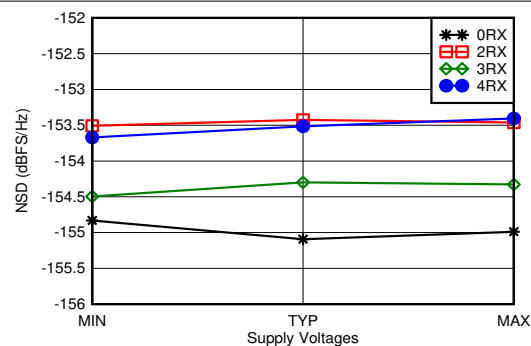
With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-170. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-171. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, tone at -20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

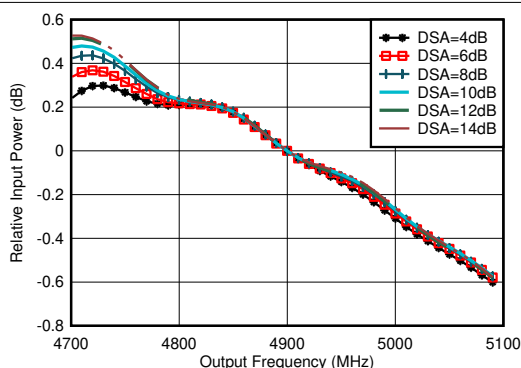
Figure 7-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

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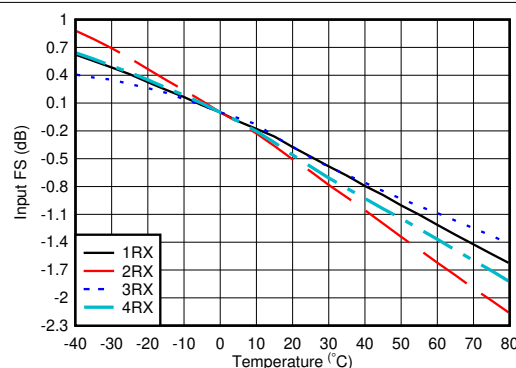
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7.12.6 RX Typical Characteristics 4.9GHz

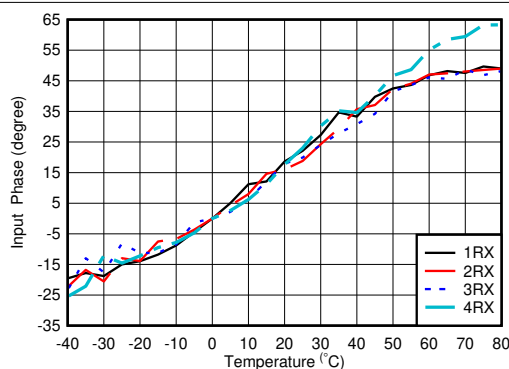
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



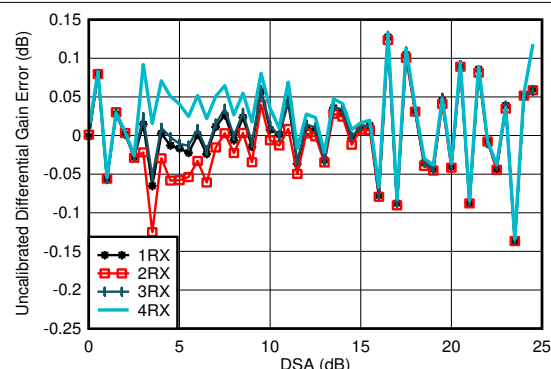
With matching, normalized to power at 4.9GHz for each DSA setting

Figure 7-173. RX Inband Gain Flatness, $f_{\text{IN}} = 4900\text{ MHz}$ 

With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

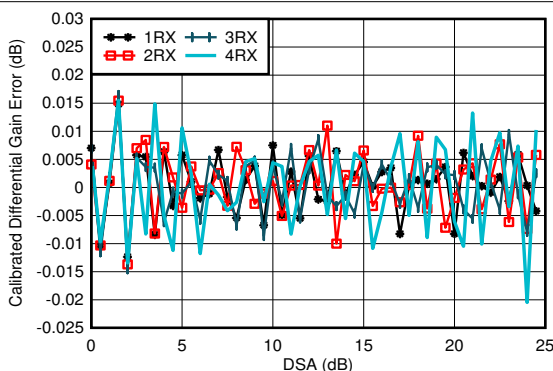
Figure 7-174. RX Input Fullscale vs Temperature and Channel at 4.9 GHz

With 4.9 GHz matching, normalized to phase at 25°C

Figure 7-175. RX Input Phase vs Temperature and DSA at $f_{\text{OUT}} = 4.9\text{ GHz}$ 

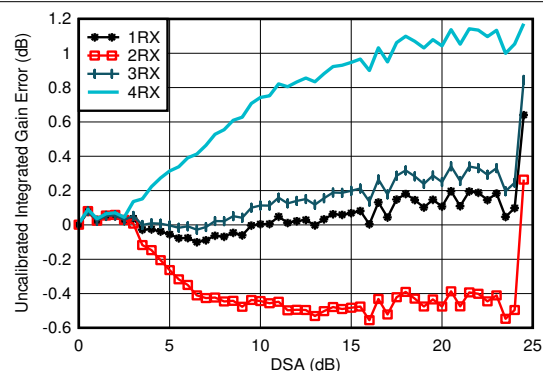
With 4.9 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz

With 4.9 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz

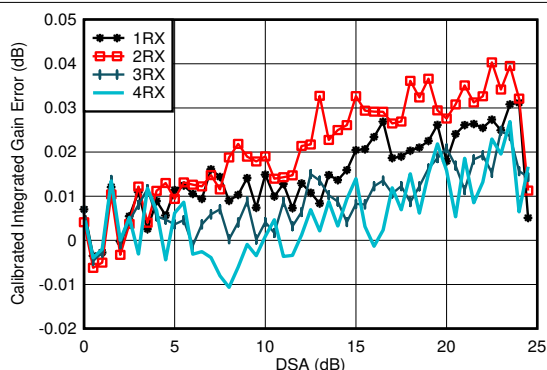
With 4.9 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

7.12.6 RX Typical Characteristics 4.9GHz (continued)

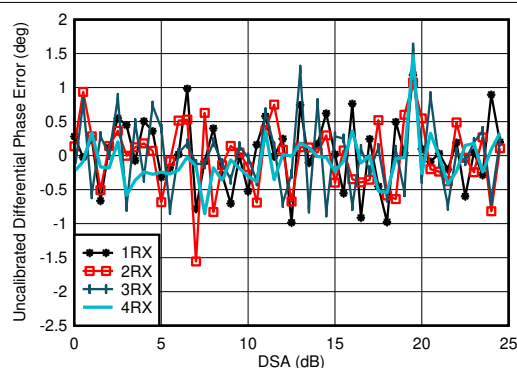
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{dBFS}$, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

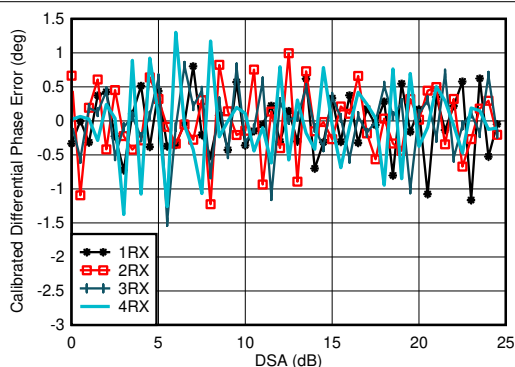
Figure 7-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

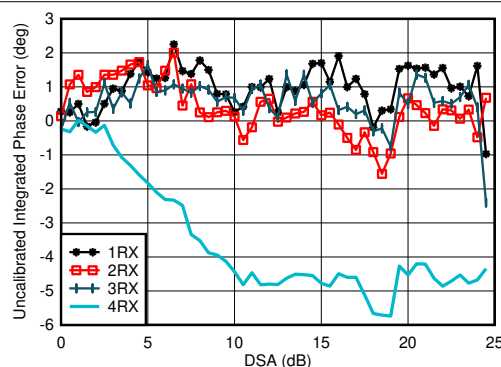
Figure 7-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

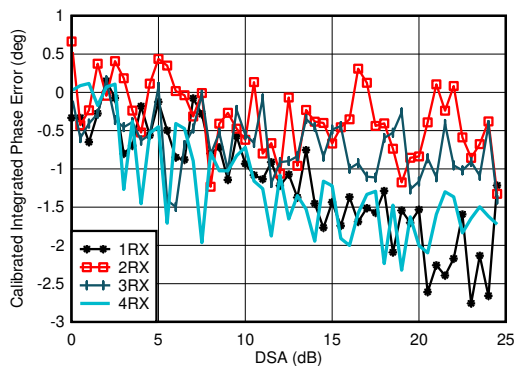
Figure 7-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

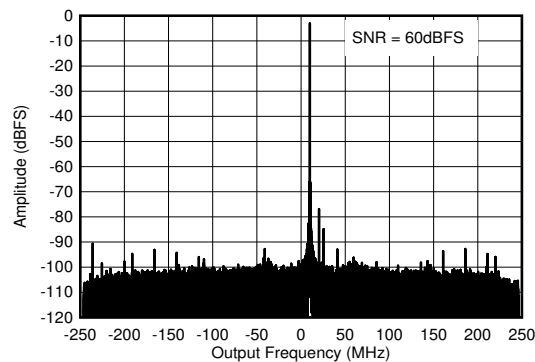
Figure 7-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-183. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching, $f_{\text{IN}} = 4910\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$

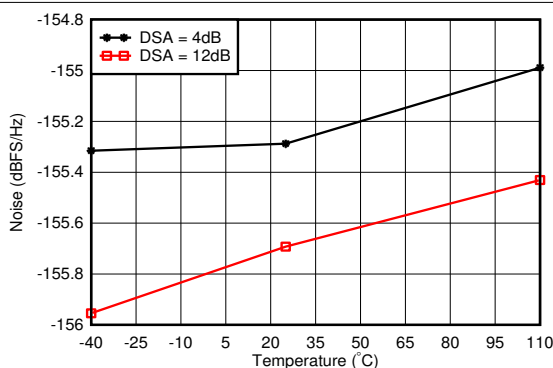
Figure 7-184. RX Output FFT at 4.9 GHz

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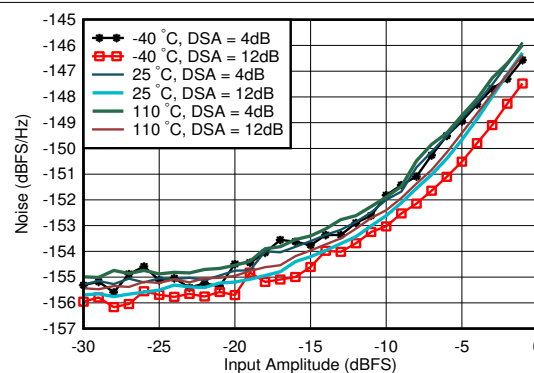
7.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



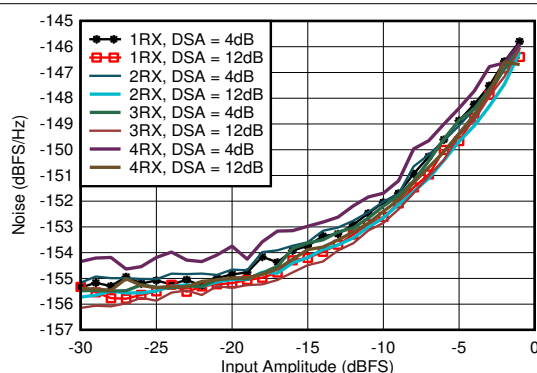
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 7-185. RX Noise Spectral Density vs Temperature at 4.9 GHz



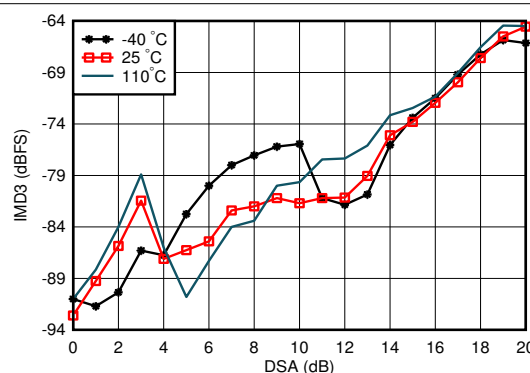
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 7-186. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



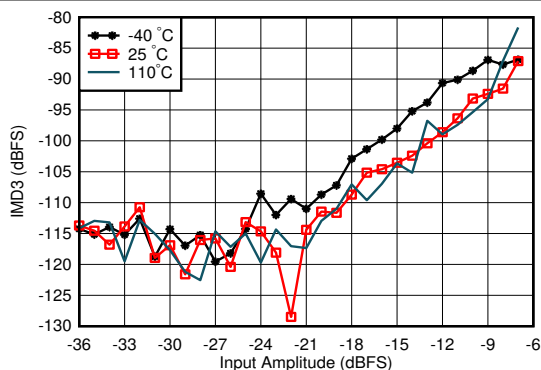
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 7-187. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz



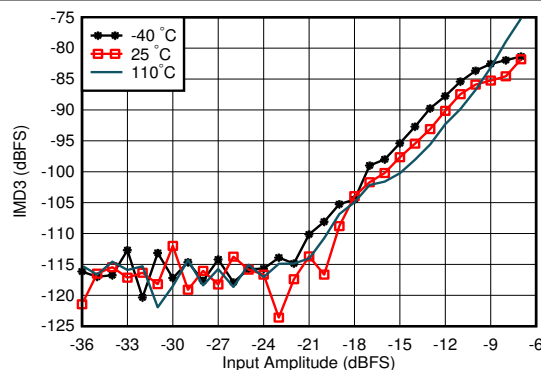
With 4.9 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-188. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-189. RX IMD3 vs Input Level and Temperature at 4.9 GHz

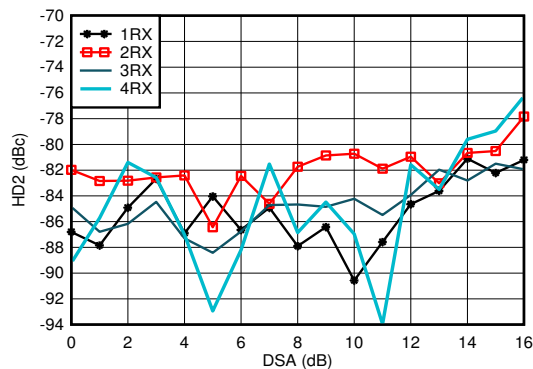


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-190. RX IMD3 vs Input Level and Temperature at 4.9 GHz

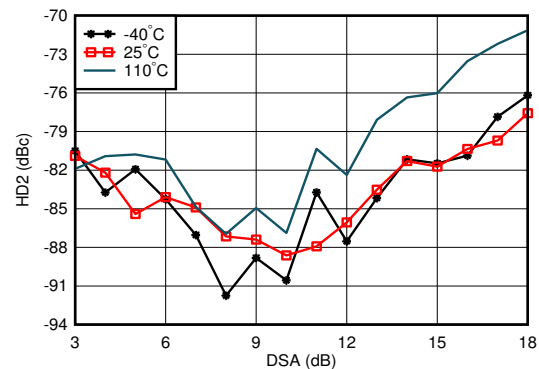
7.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



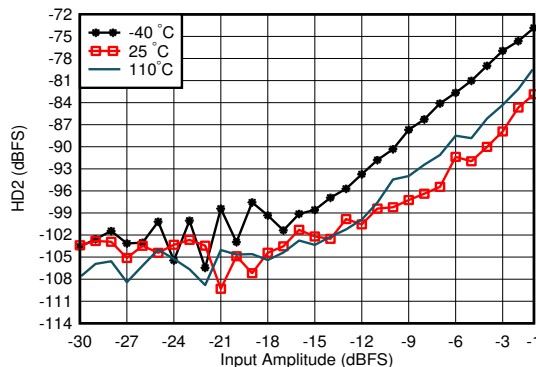
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-191. RX HD2 vs DSA Setting and Channel at 4.9 GHz



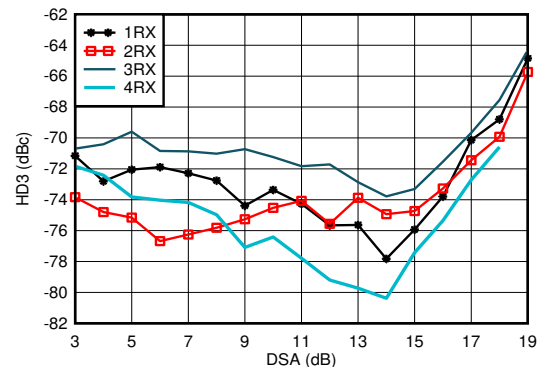
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-192. RX HD2 vs DSA and Temperature at 4.9 GHz



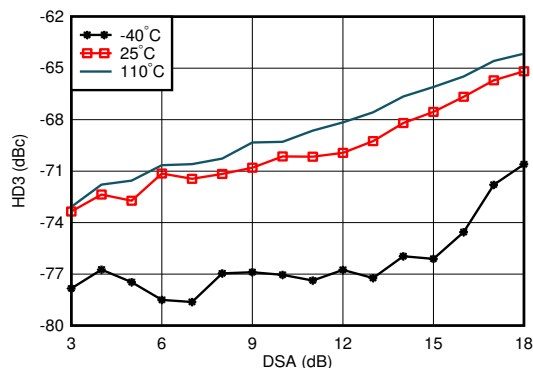
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-193. RX HD2 vs Input Level and Temperature at 4.9 GHz



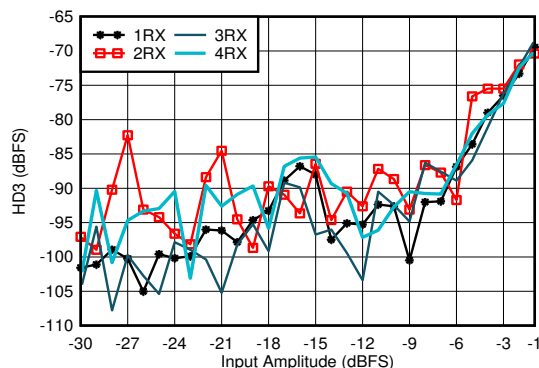
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-194. RX HD3 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-195. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

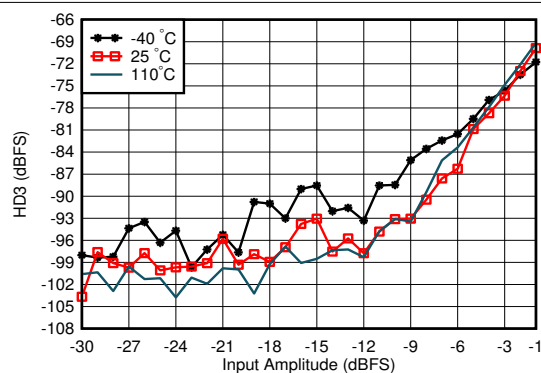
Figure 7-196. RX HD3 vs Input Level and Channel at 4.9 GHz

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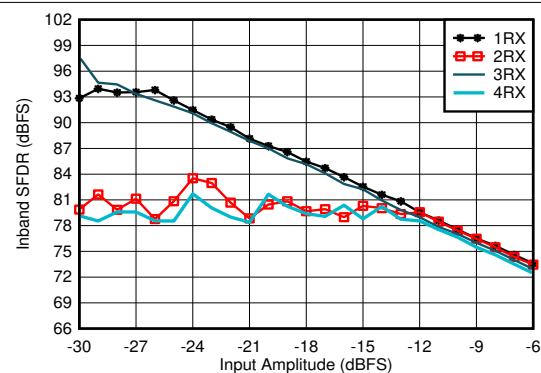
7.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



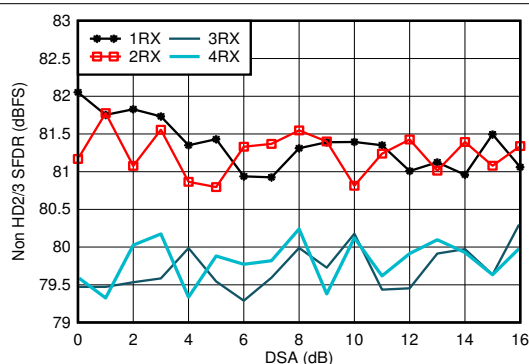
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-197. RX HD3 vs Input Level and Temperature at 4.9 GHz



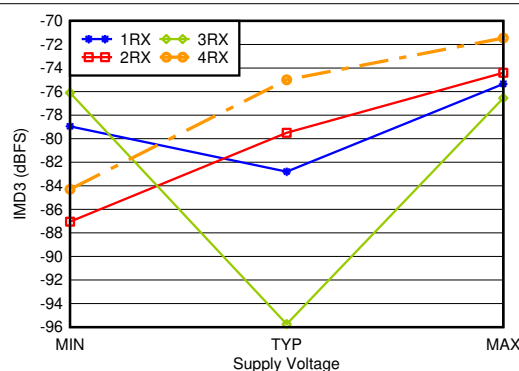
With 4.9 GHz matching, decimate by 3

Figure 7-198. RX In-Band SFDR ($\pm 400\text{ MHz}$) vs Input Amplitude and Channel at 4.9 GHz



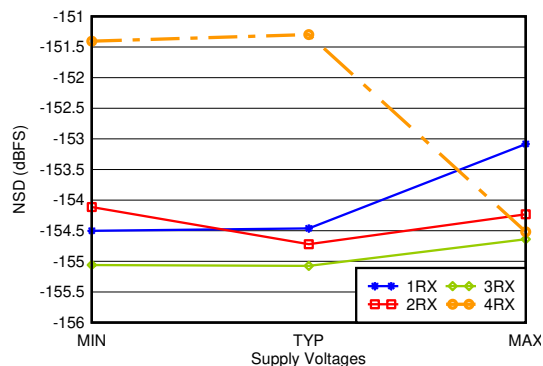
With 4.9 GHz matching

Figure 7-199. RX Non-HD2/3 vs DSA Setting at 4.9 GHz



With 4.9 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-200. RX IMD3 vs Supply and Channel at 4.9 GHz

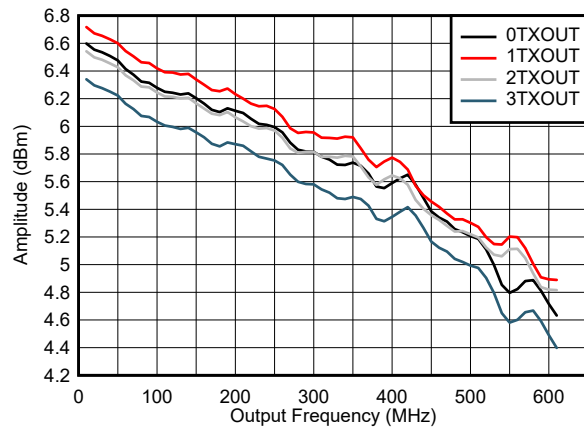


With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-201. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

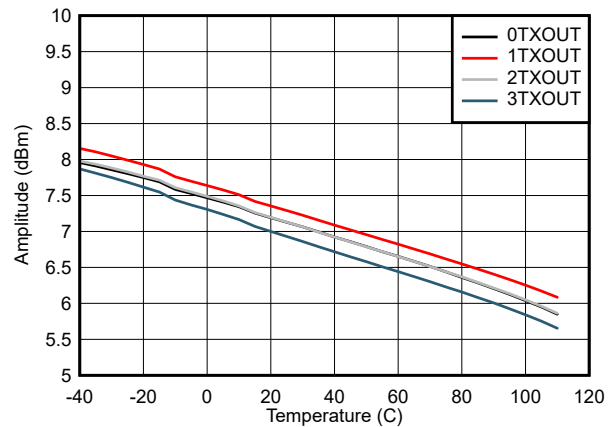
7.12.7 TX Typical Characteristics at 30MHz and 400MHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



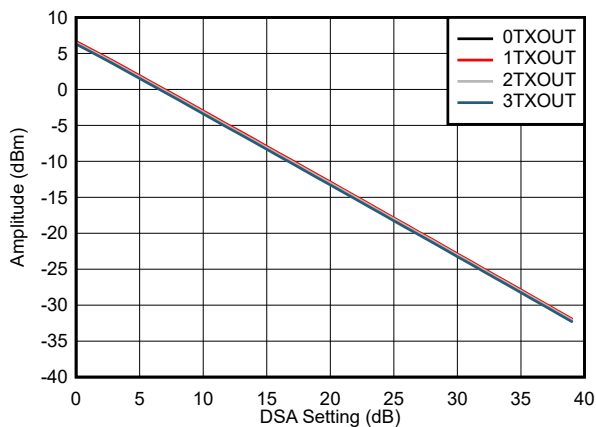
including PCB and cable losses

Figure 7-202. TX Output Fullscale vs Output Frequency: 5 MHz - 600 MHz



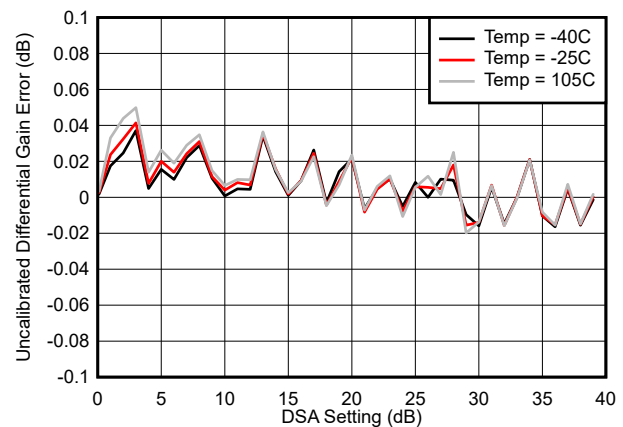
including PCB and cable losses

Figure 7-203. TX Output Fullscale vs Temperature at 30 MHz



including PCB and cable losses

Figure 7-204. TX Output Fullscale vs DSA Setting at 30 MHz



Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

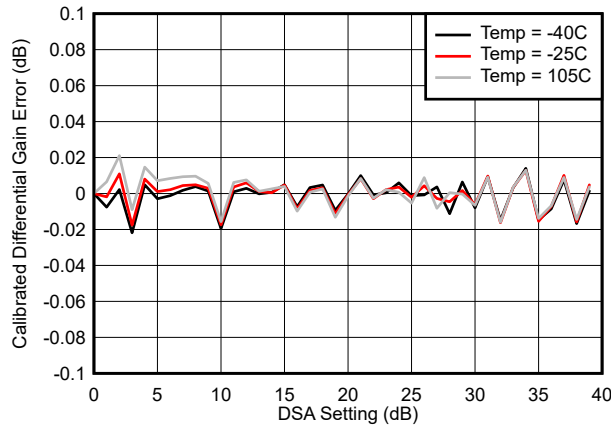
Figure 7-205. Uncalibrated TX Differential Gain Error (DNL) at 30 MHz

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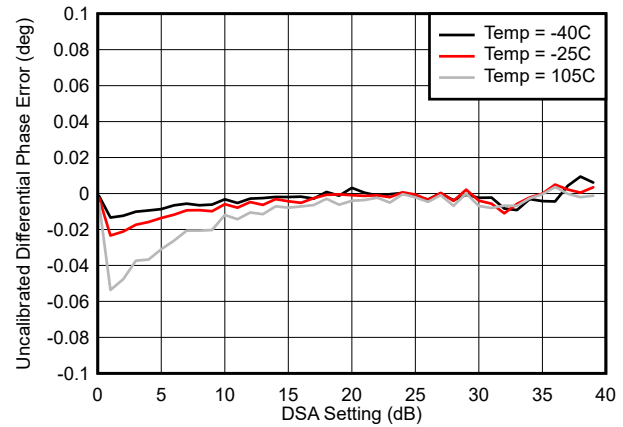
7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



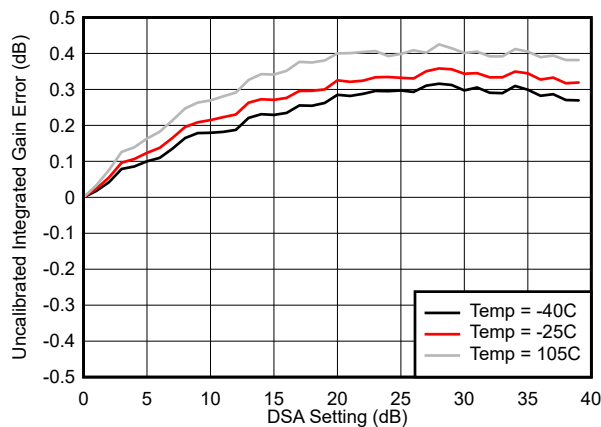
$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

Figure 7-206. Calibrated TX Differential Gain Error (DNL) at 30MHz



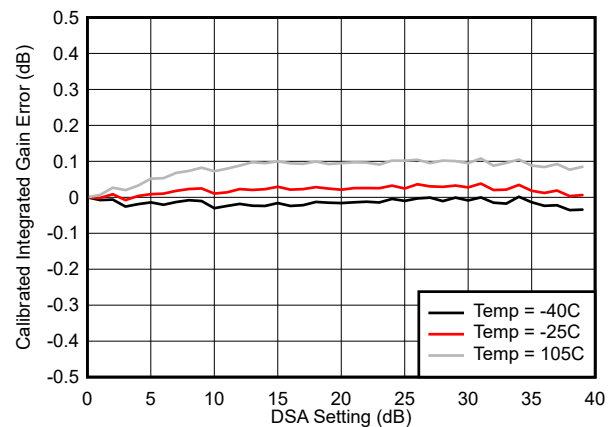
$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

Figure 7-207. Calibrated TX Differential Gain Error (DNL) at 30 MHz



$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

Figure 7-208. Uncalibrated TX Integrated Gain Error (INL) at 30 MHz

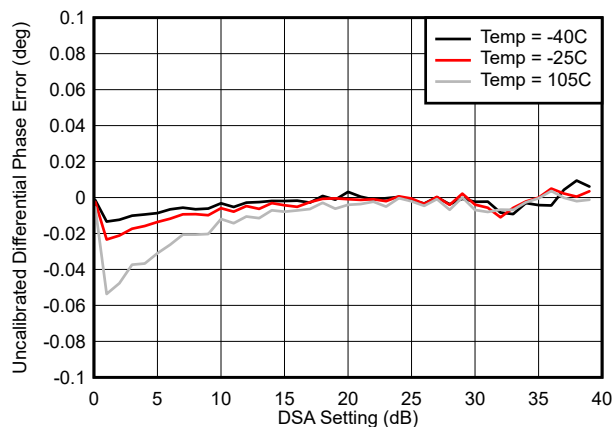


$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

Figure 7-209. Calibrated TX Integrated Gain Error (INL) at 30 MHz

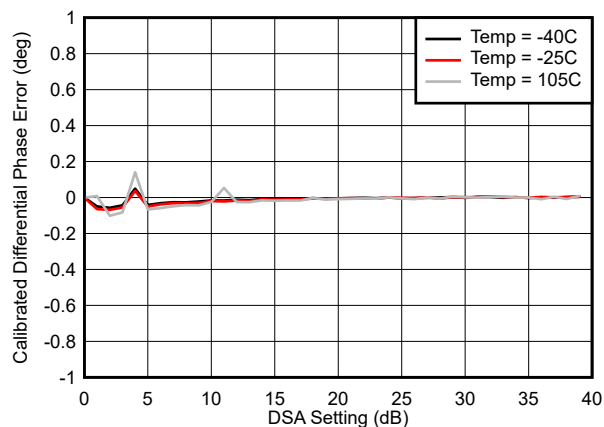
7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



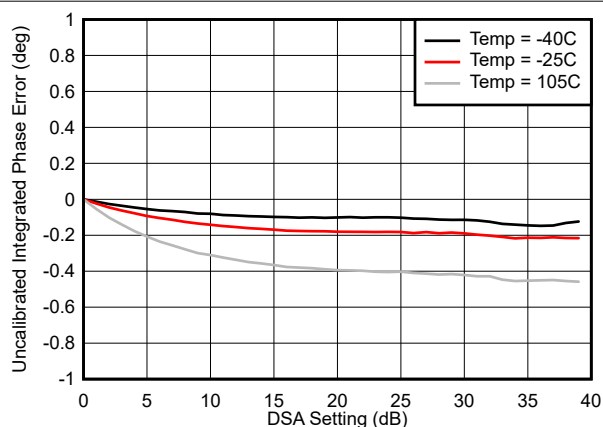
$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

Figure 7-210. Uncalibrated TX Differential Phase Error (DNL) at 30 MHz



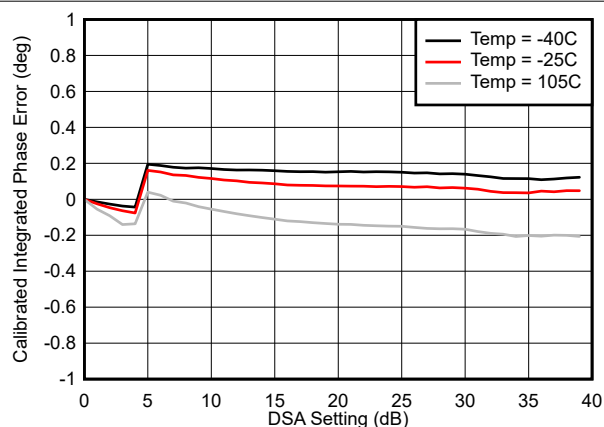
$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

Figure 7-211. Calibrated TX Differential Phase Error (DNL) at 30 MHz



$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

Figure 7-212. Uncalibrated TX Integrated Phase Error (INL) at 30 MHz



$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

Figure 7-213. Calibrated TX Integrated Phase Error (INL) at 30 MHz

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7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

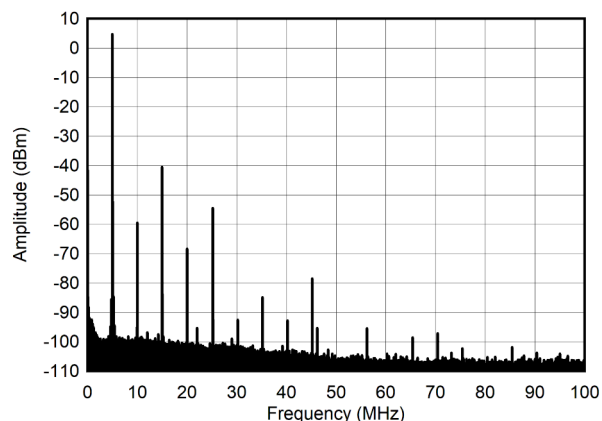


Figure 7-214. Single Tone Spectrum at 5 MHz and -1 dBFS (0 - 100 MHz)

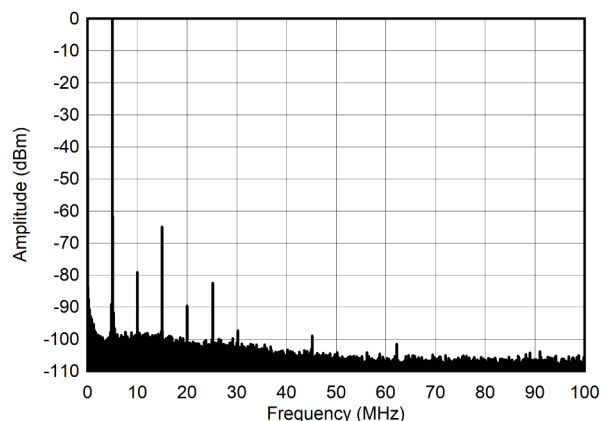


Figure 7-215. Single Tone Spectrum at 5 MHz and -6 dBFS (0 - 100 MHz)

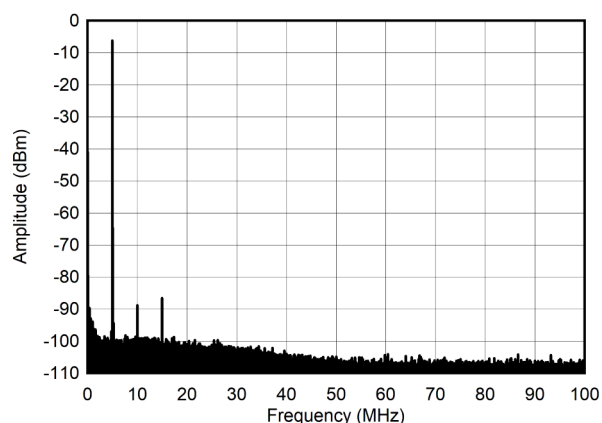


Figure 7-216. Single Tone Spectrum at 5 MHz and -12 dBFS (0 - 100 MHz)

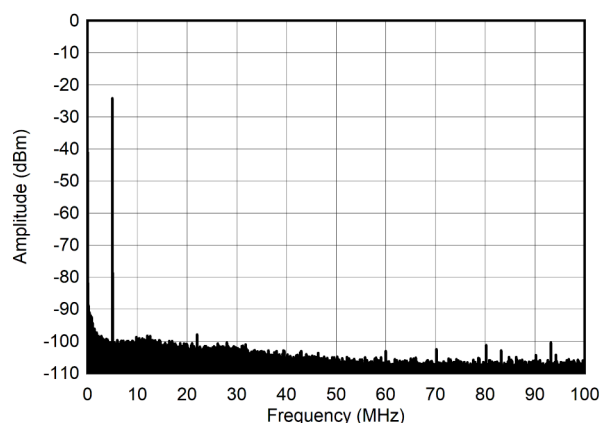


Figure 7-217. Single Tone Spectrum at 5 MHz and -30 dBFS (0 - 100 MHz)

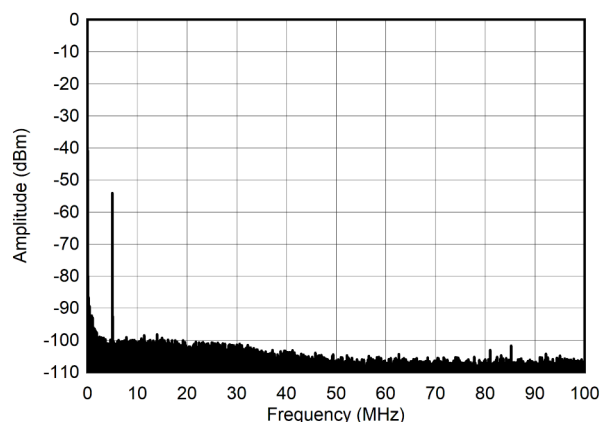


Figure 7-218. Single Tone Spectrum at 5 MHz and -60 dBFS (0 - 100 MHz)

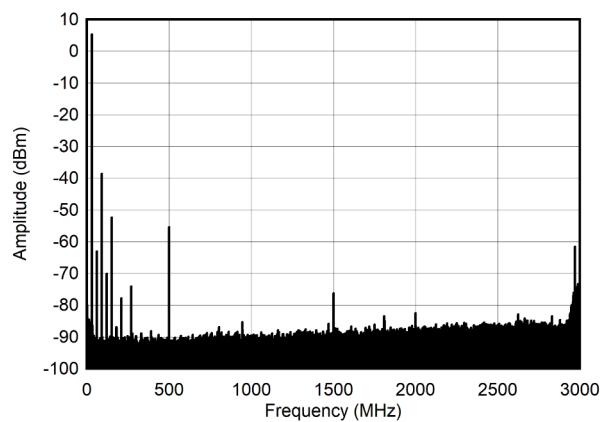


Figure 7-219. Single Tone Spectrum at 30 MHz and -1 dBFS (Nyquist)

7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

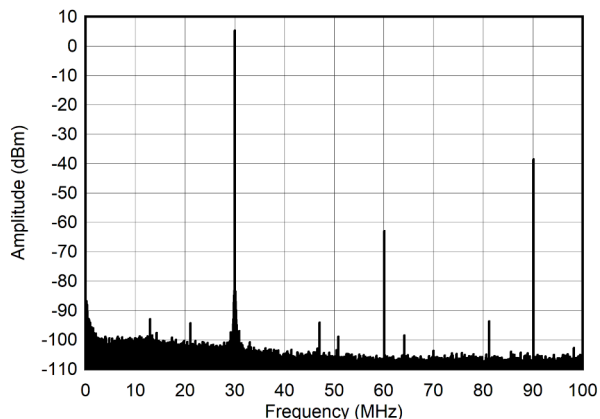


Figure 7-220. Single Tone Spectrum at 30 MHz and -1 dBFS (0 - 100 MHz)

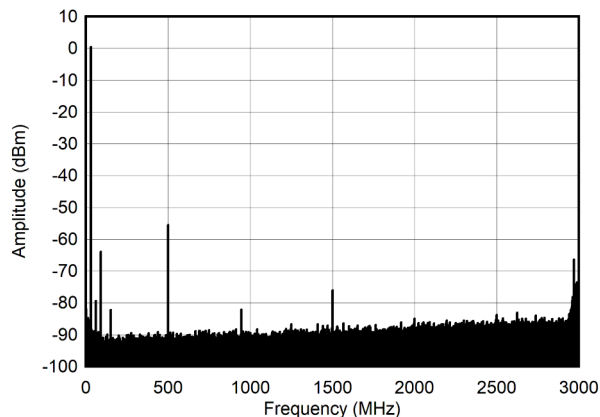


Figure 7-221. Single Tone Spectrum at 30 MHz and -6 dBFS (Nyquist)

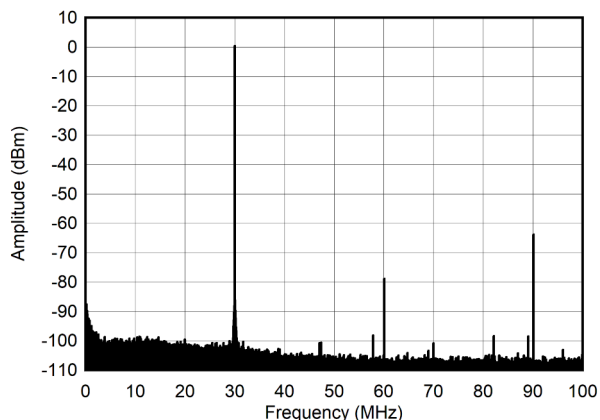


Figure 7-222. Single Tone Spectrum at 30 MHz and -6 dBFS (0 - 100 MHz)

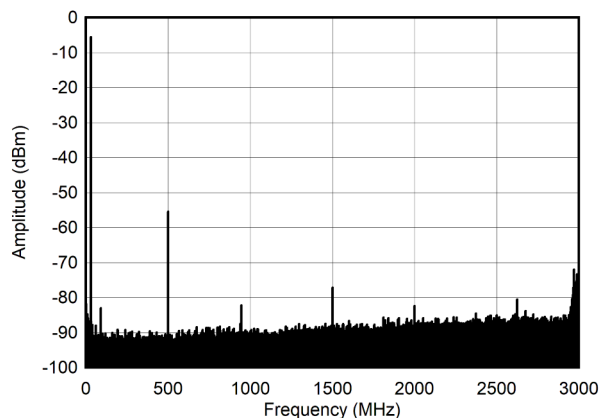


Figure 7-223. Single Tone Spectrum at 30 MHz and -12 dBFS (Nyquist)

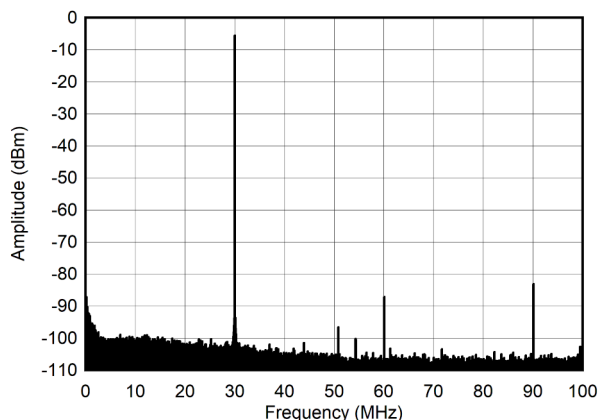


Figure 7-224. Single Tone Spectrum at 30 MHz and -12 dBFS (0 - 100 MHz)

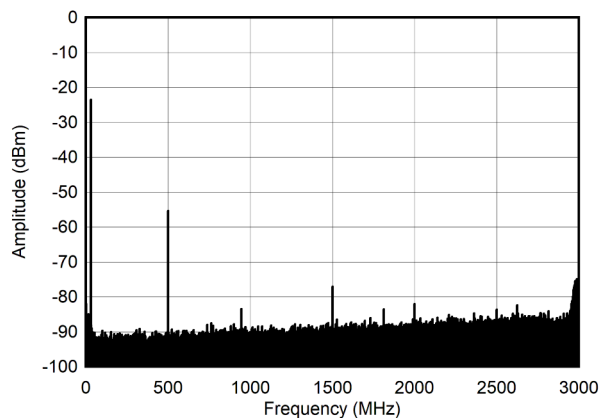


Figure 7-225. Single Tone Spectrum at 30 MHz and -30 dBFS (Nyquist)

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7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

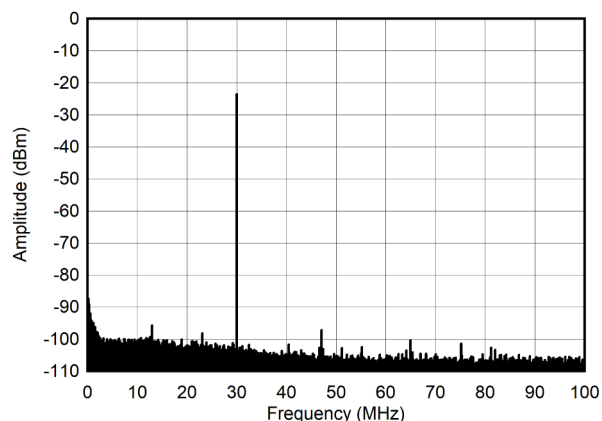


Figure 7-226. Single Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

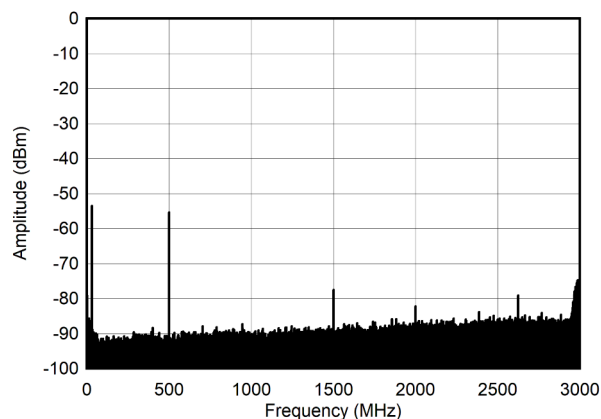


Figure 7-227. Single Tone Spectrum at 30 MHz and -60 dBFS (Nyquist)

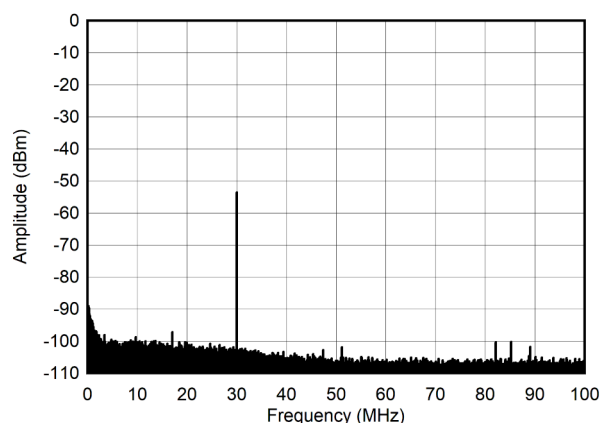


Figure 7-228. Single Tone Spectrum at 30 MHz and -60 dBFS (0 - 100 MHz)

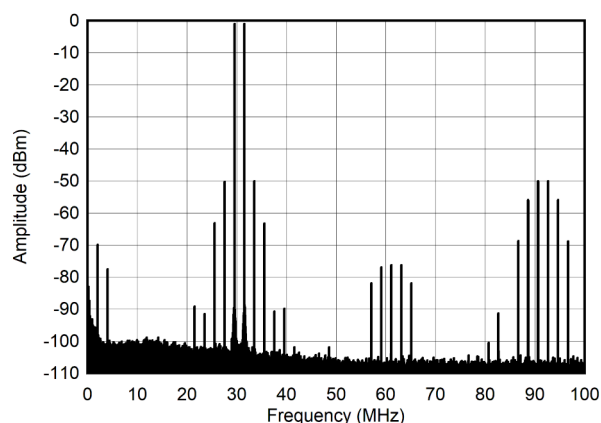


Figure 7-229. Dual Tone Spectrum at 30 MHz and -7 dBFS (0 - 100 MHz)

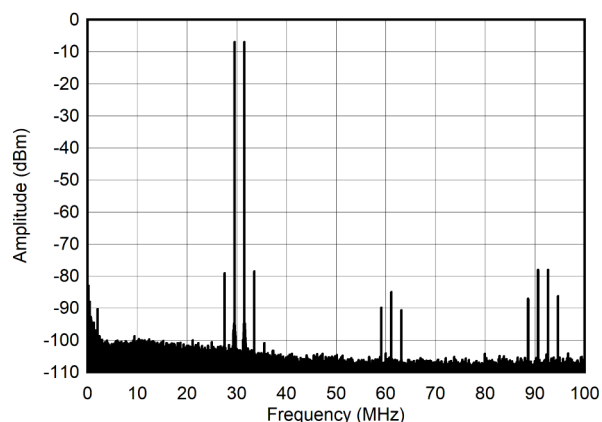


Figure 7-230. Dual Tone Spectrum at 30 MHz and -13 dBFS (0 - 100 MHz)

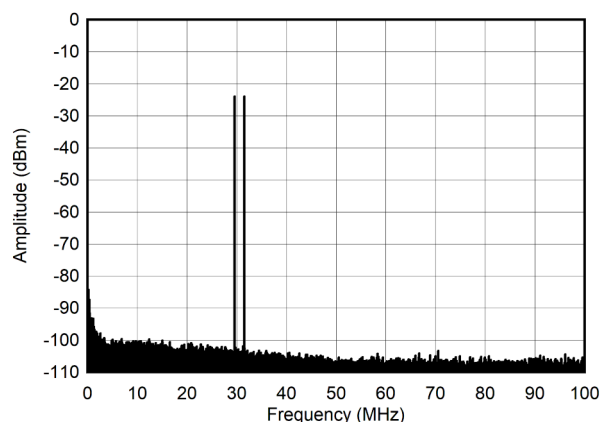


Figure 7-231. Dual Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

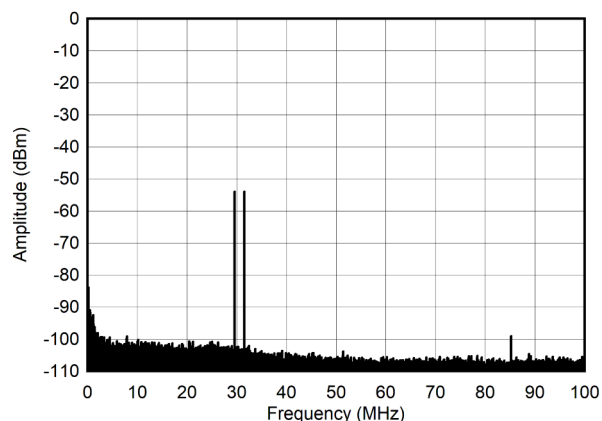
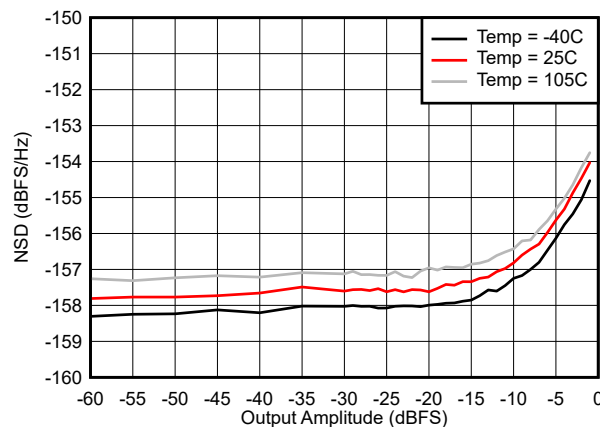
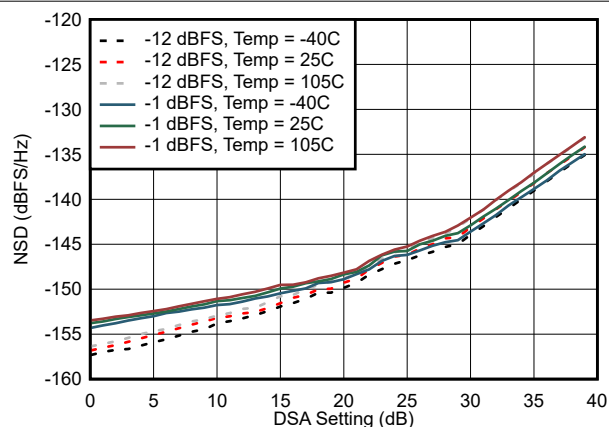


Figure 7-232. Dual Tone Spectrum at 30 MHz and -60d BFS (0 - 100 MHz)



measured at +50 MHz offset

Figure 7-233. Noise Spectral Density vs Digital Amplitude at 30 MHz



measured at +50 MHz offset

Figure 7-234. Noise Spectral Density vs DSA Setting at 30 MHz

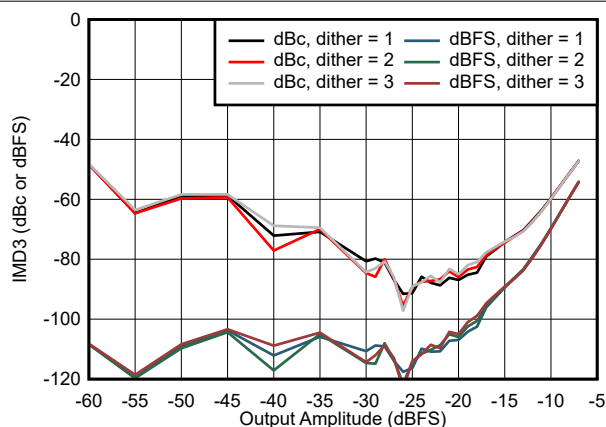


Figure 7-235. IMD3 vs Digital Amplitude at 30 MHz

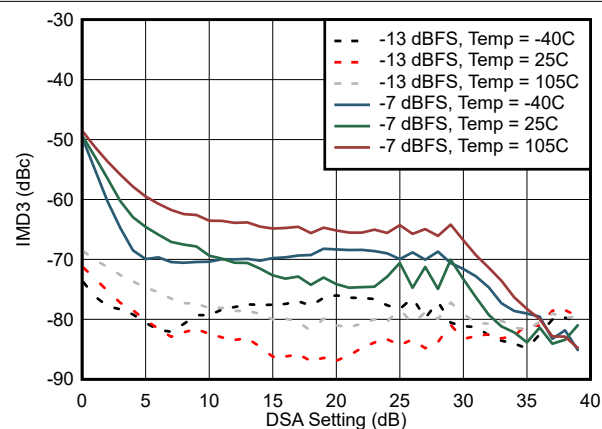


Figure 7-236. IMD3 vs DSA Setting at 30 MHz

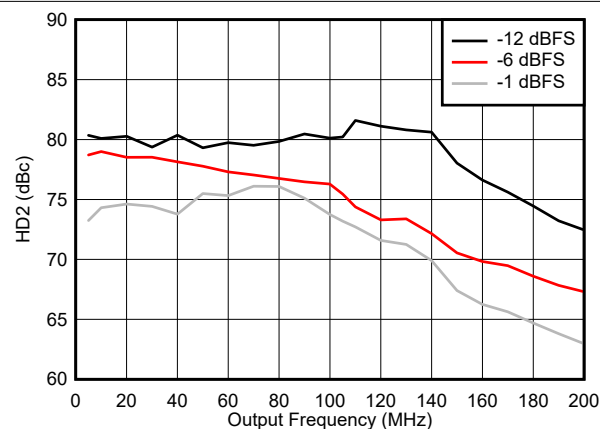


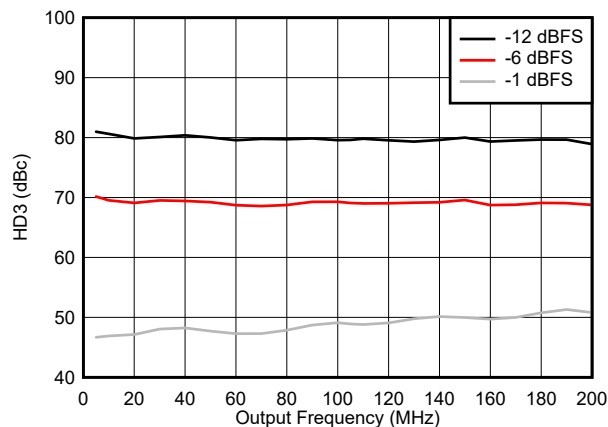
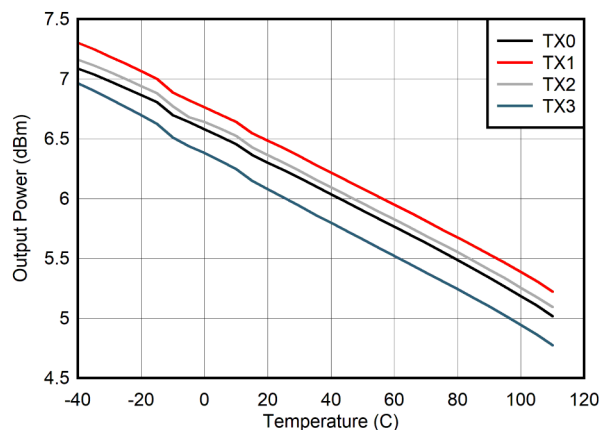
Figure 7-237. HD2 vs Frequency 0 - 200 MHz

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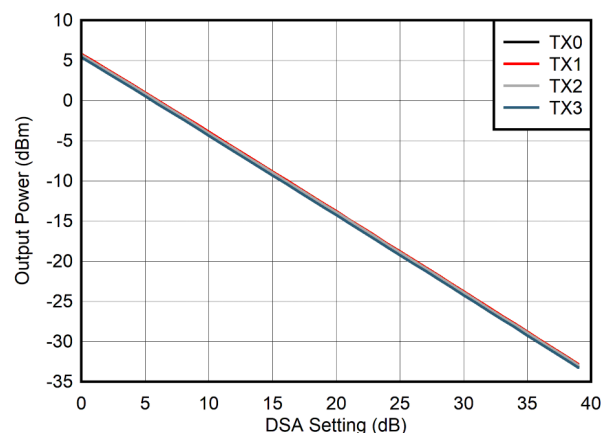
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7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

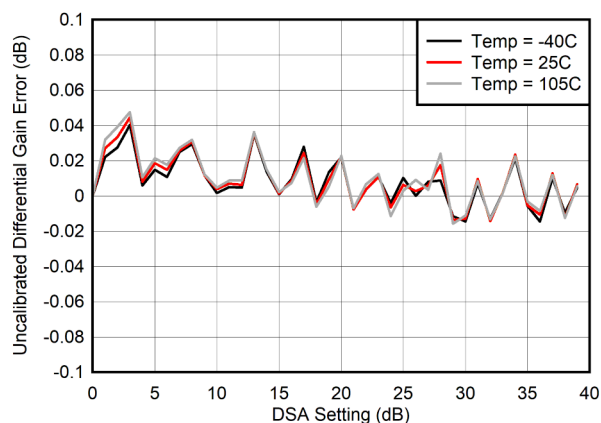
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

**Figure 7-238. HD3 vs Frequency 0 - 200 MHz**

including PCB and cable losses

Figure 7-239. TX Output Fullscale vs Temperature at 400 MHz

including PCB and cable losses

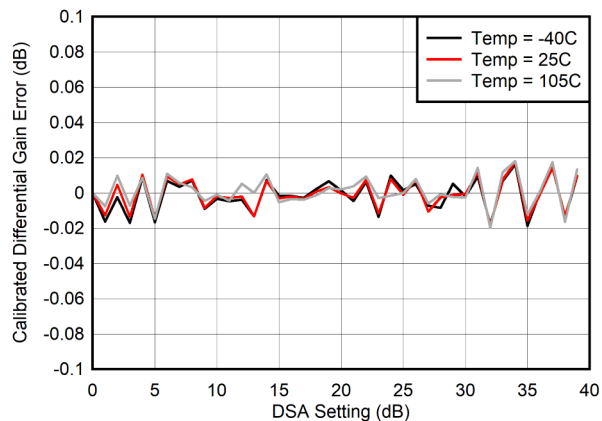
Figure 7-240. TX Output Fullscale vs DSA Setting at 400 MHz

Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-241. Uncalibrated TX Differential Gain Error (DNL) at 400 MHz

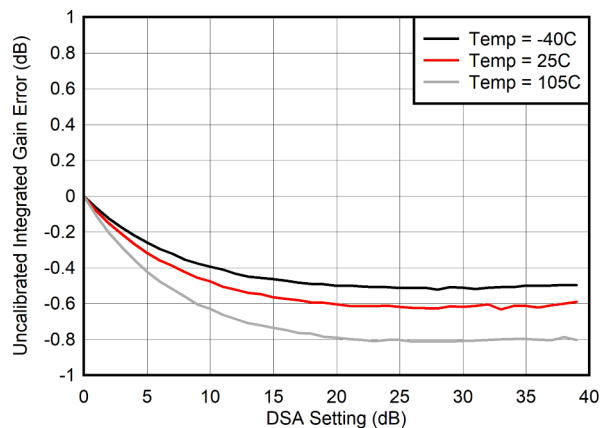
7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



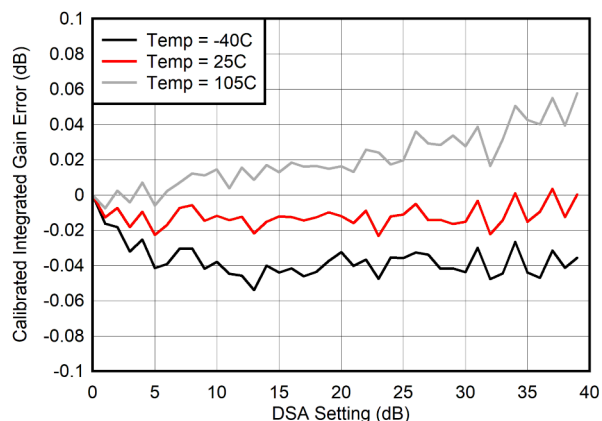
$$\text{Differential Gain Error} = P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$$

Figure 7-242. Calibrated TX Differential Gain Error (DNL) at 400 MHz



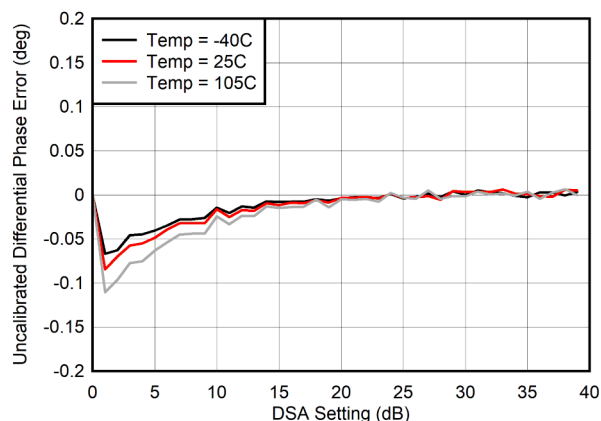
$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

Figure 7-243. Uncalibrated TX Integrated Gain Error (INL) at 400 MHz



$$\text{Integrated Gain Error} = P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSASetting} = 0) + (\text{DSA Setting})$$

Figure 7-244. Calibrated TX Integrated Gain Error (INL) at 400 MHz



$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

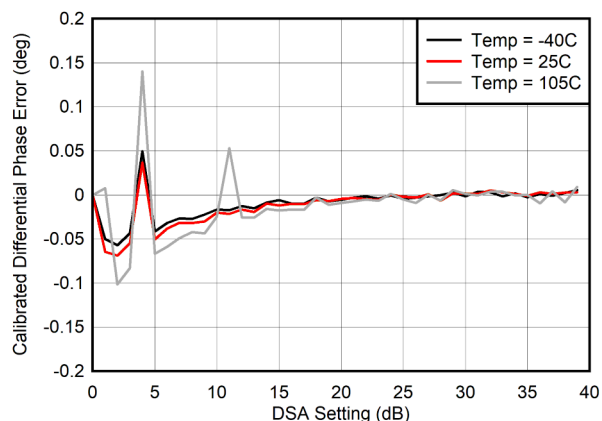
Figure 7-245. Uncalibrated TX Differential Phase Error (DNL) at 400 MHz

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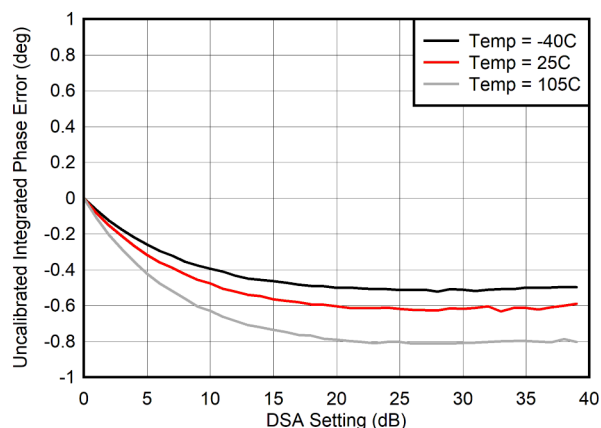
7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



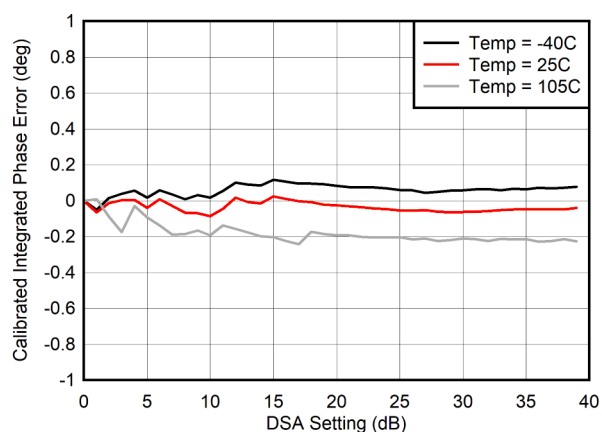
$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

Figure 7-246. Calibrated TX Differential Phase Error (DNL) at 400 MHz



$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

Figure 7-247. Uncalibrated TX Integrated Phase Error (INL) at 400 MHz



$$\text{Integrated Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSASetting} = 0)$$

Figure 7-248. Calibrated TX Integrated Phase Error (INL) at 400 MHz

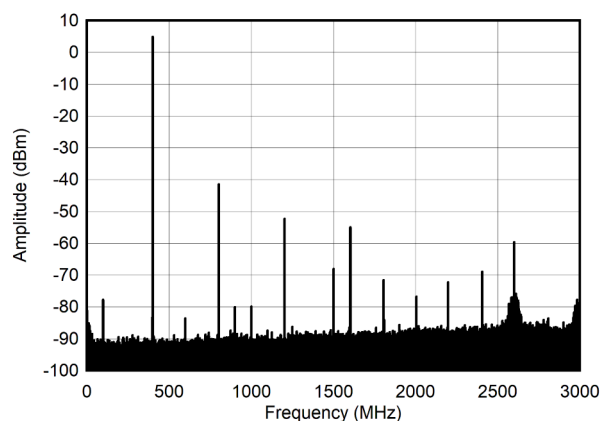


Figure 7-249. Single Tone Spectrum at 400 MHz and -1 dBFS (Nyquist)

7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

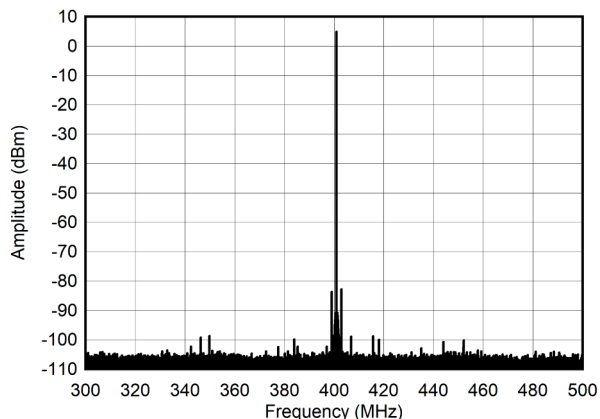


Figure 7-250. Single Tone Spectrum at 400 MHz and -1 dBFS ($\pm 100\text{MHz}$)

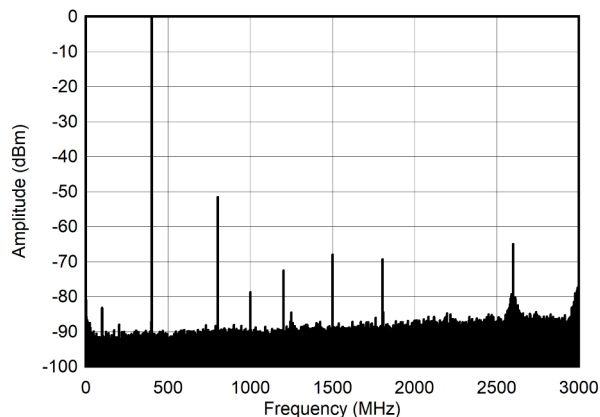


Figure 7-251. Single Tone Spectrum at 400 MHz and -6 dBFS (Nyquist)

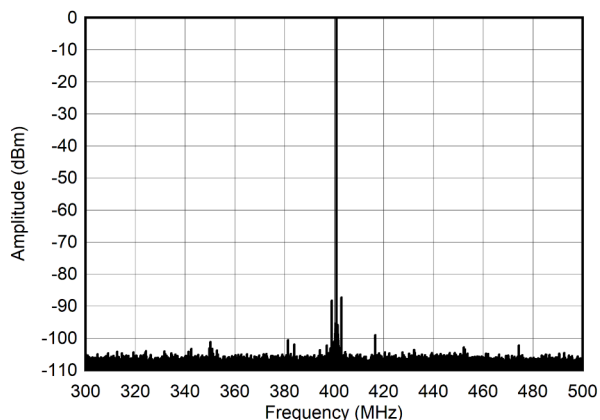


Figure 7-252. Single Tone Spectrum at 400 MHz and -6 dBFS ($\pm 100\text{MHz}$)

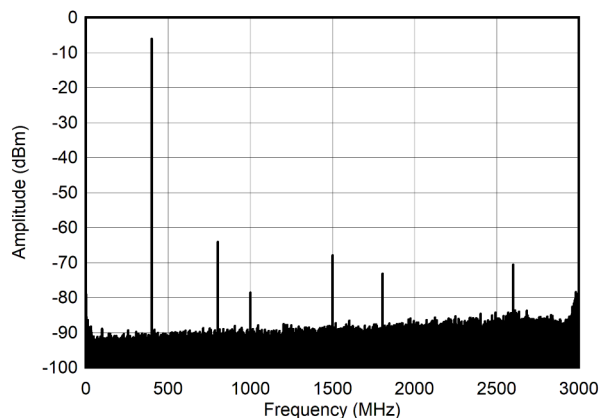


Figure 7-253. Single Tone Spectrum at 400 MHz and -12 dBFS (Nyquist)

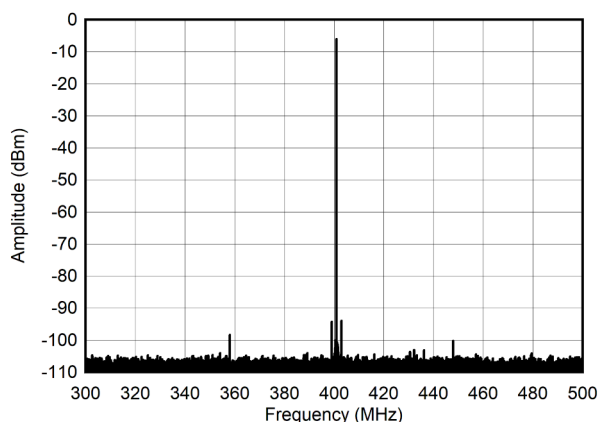


Figure 7-254. Single Tone Spectrum at 400 MHz and -12 dBFS ($\pm 100\text{MHz}$)

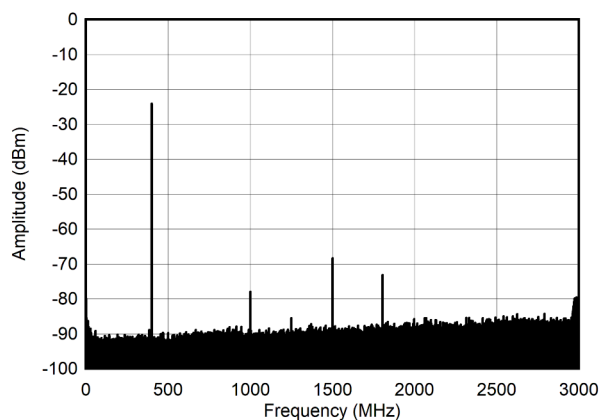


Figure 7-255. Single Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)

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7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

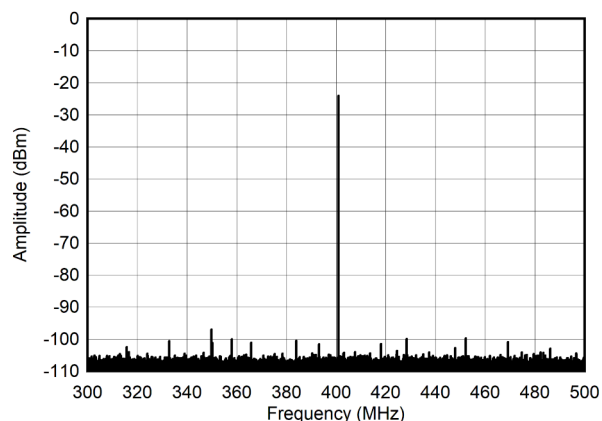


Figure 7-256. Single Tone Spectrum at 400 MHz and -30 dBFS ($\pm 100\text{MHz}$)

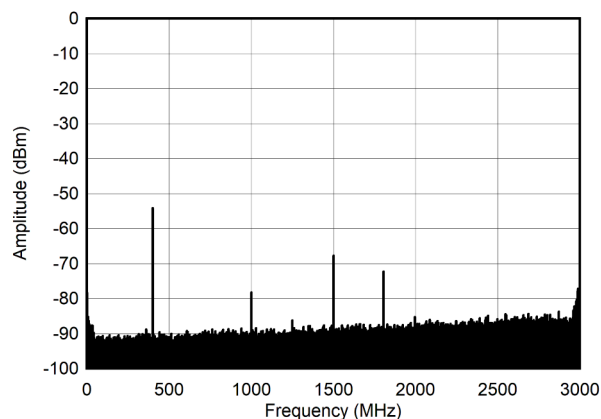


Figure 7-257. Single Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)

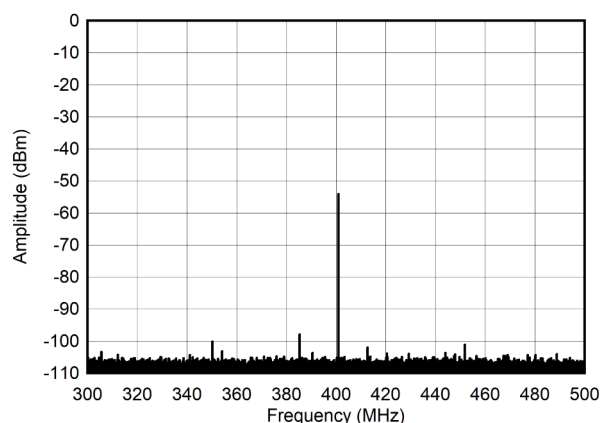
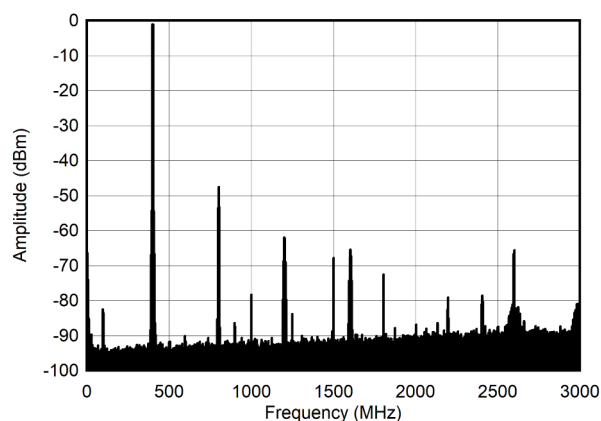


Figure 7-258. Single Tone Spectrum at 400 MHz and -60 dBFS ($\pm 100\text{MHz}$)

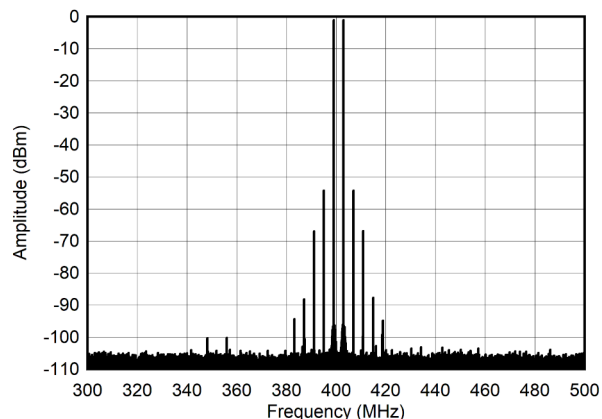


Tone Spacing = 4 MHz

Figure 7-259. Dual Tone Spectrum at 400 MHz and -7 dBFS (Nyquist)

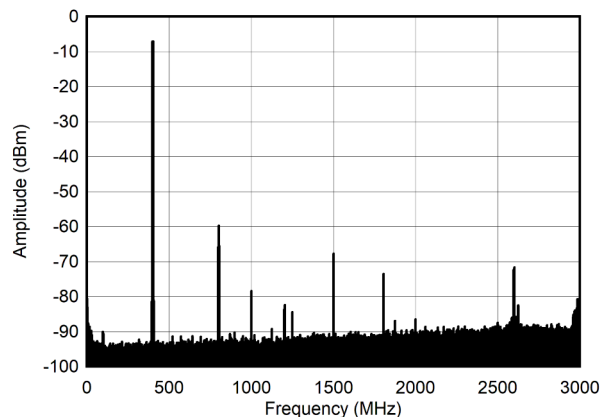
7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



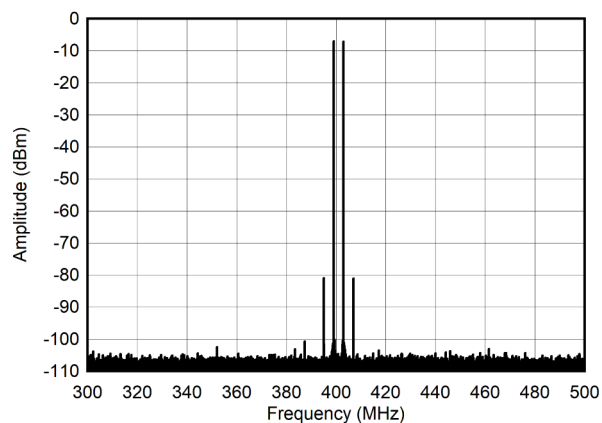
Tone Spacing = 4 MHz

Figure 7-260. Dual Tone Spectrum at 400 MHz and -7 dBFS (±100MHz)



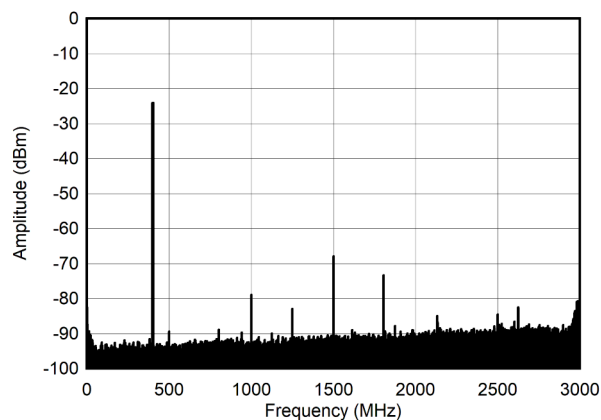
Tone Spacing = 4 MHz

Figure 7-261. Dual Tone Spectrum at 400 MHz and -13 dBFS (Nyquist)



Tone Spacing = 4 MHz

Figure 7-262. Dual Tone Spectrum at 400 MHz and -13 dBFS (±100MHz)



Tone Spacing = 4 MHz

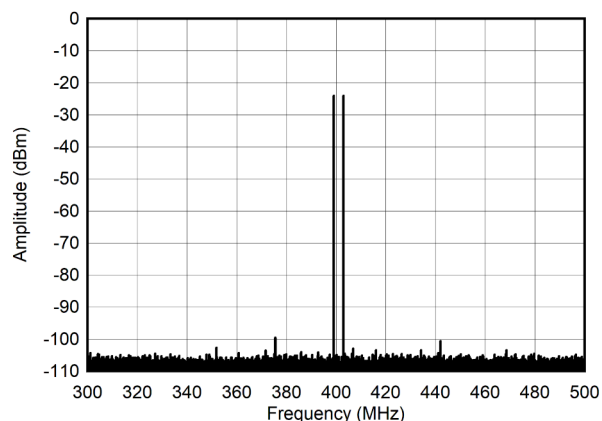
Figure 7-263. Dual Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)

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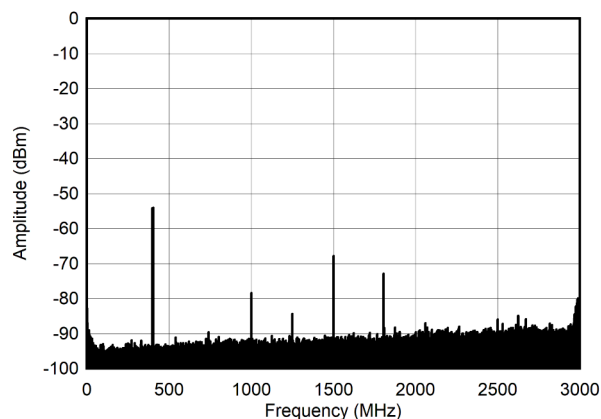
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7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

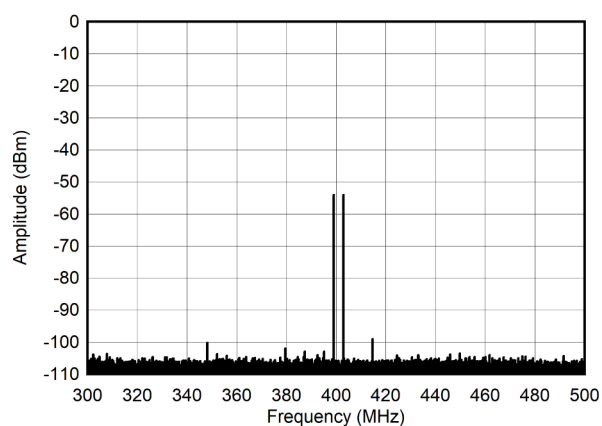
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



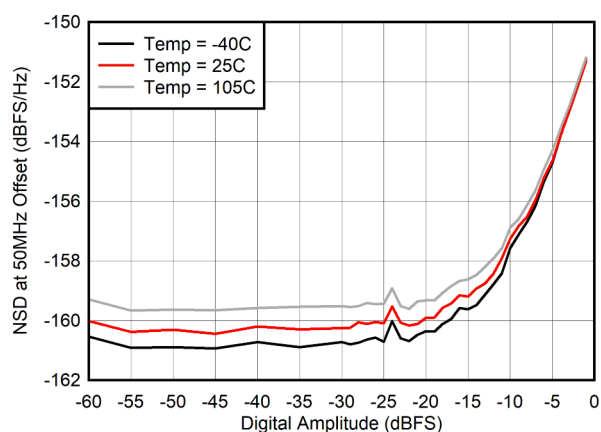
Tone Spacing = 4 MHz

Figure 7-264. Dual Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)

Tone Spacing = 4 MHz

Figure 7-265. Dual Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)

Tone Spacing = 4 MHz

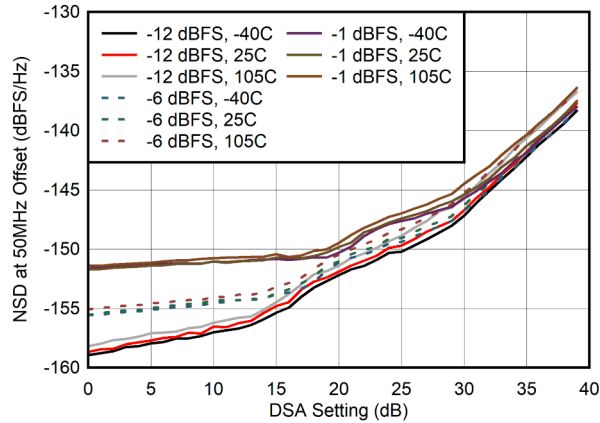
Figure 7-266. Dual Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)

measured at 50 MHz offset

Figure 7-267. Noise Spectral Density vs Digital Amplitude at 400 MHz

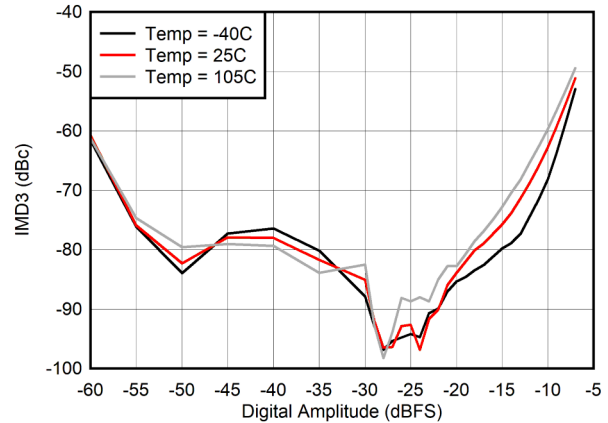
7.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 125 MSPS, $f_{\text{DAC}} = 6000$ MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 500$ MHz. Additional default conditions for all plots, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



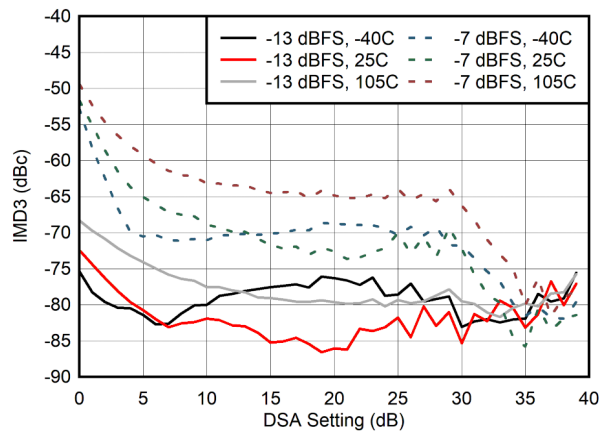
measured at 50 MHz offset

Figure 7-268. Noise Spectral Density vs DSA Setting at 400 MHz



Tone Spacing = 4 MHz

Figure 7-269. IMD3 vs Digital Amplitude at 400 MHz



Tone Spacing = 4 MHz

Figure 7-270. IMD3 vs DSA Setting at 400 MHz

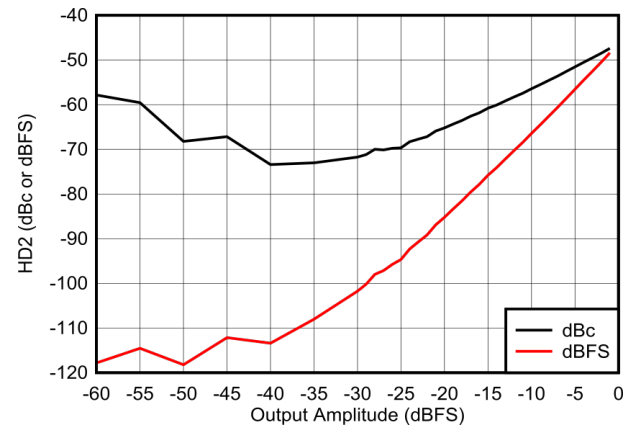


Figure 7-271. HD2 vs Amplitude at 400 MHz

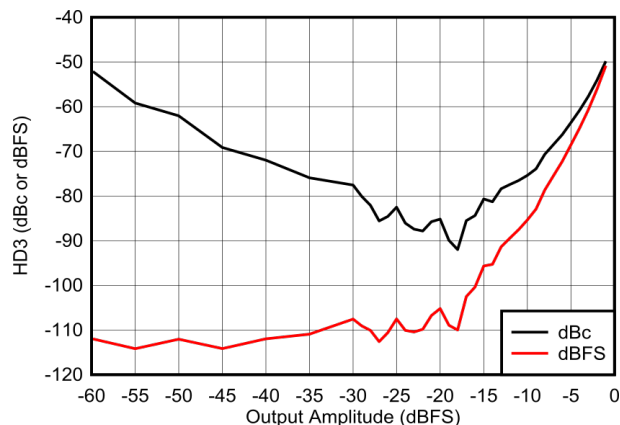


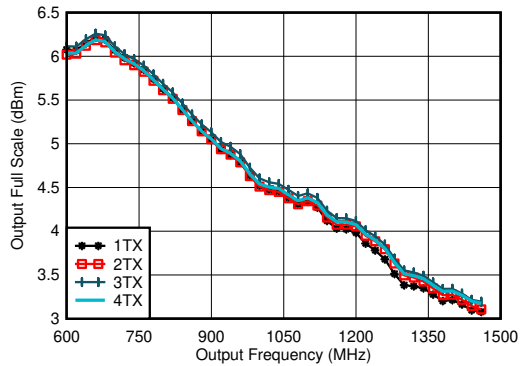
Figure 7-272. HD3 vs Amplitude at 400 MHz

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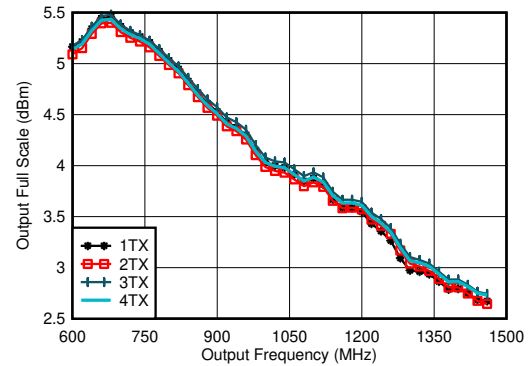
7.12.8 TX Typical Characteristics at 800MHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



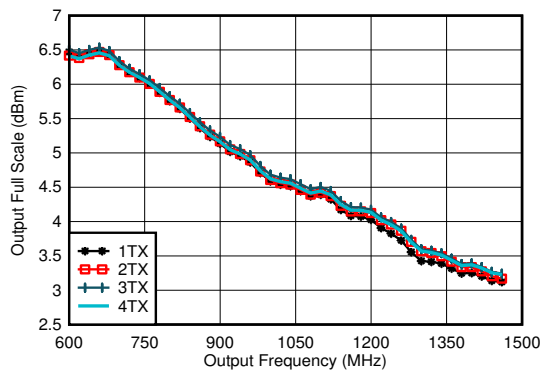
Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dFBS}$, DSA = 0, 0.8 GHz matching

Figure 7-273. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode



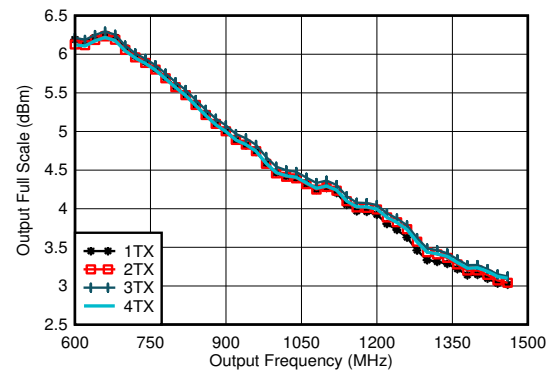
Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dFBS}$, DSA = 0, 0.8 GHz matching

Figure 7-274. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode



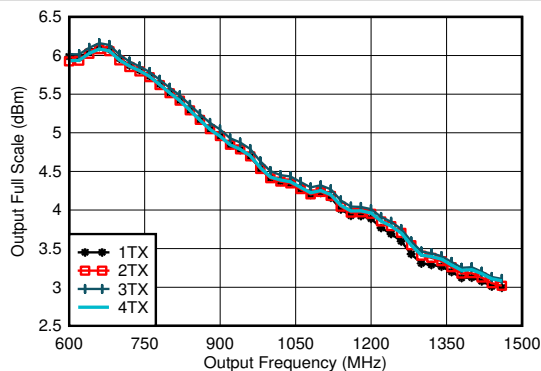
Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dFBS}$, DSA = 0, 0.8 GHz matching

Figure 7-275. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Interleave Mode



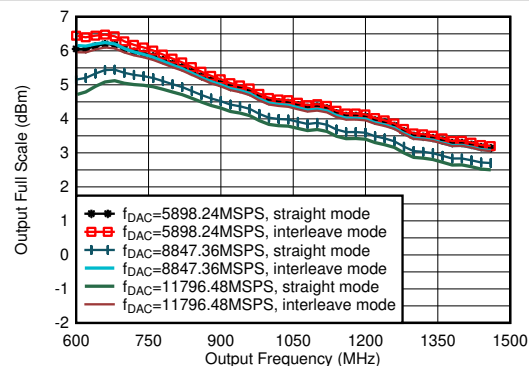
Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dFBS}$, DSA = 0, 0.8 GHz matching

Figure 7-276. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Interleave Mode



Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dFBS}$, DSA = 0, 0.8 GHz matching

Figure 7-277. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS, Interleave Mode

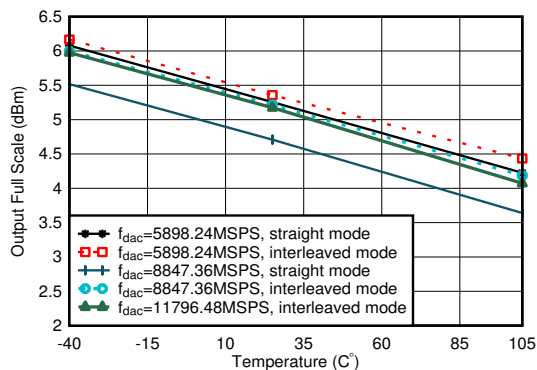


including PCB and cable losses, $A_{\text{out}} = -0.5\text{dFBS}$, DSA = 0, 0.8 GHz matching

Figure 7-278. TX Output Fullscale vs Output Frequency

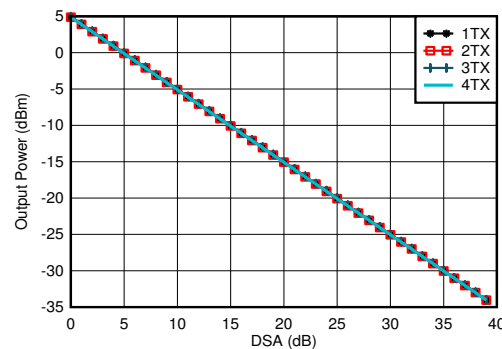
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



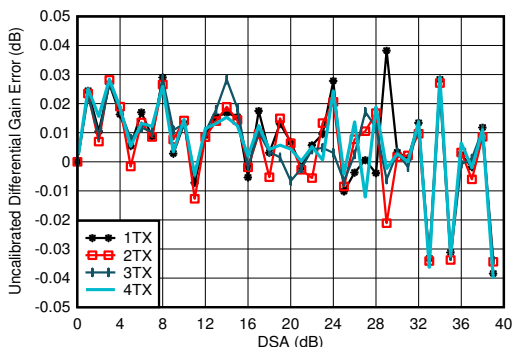
including PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 0.8 GHz matching

Figure 7-279. TX Output Fullscale vs Temperature



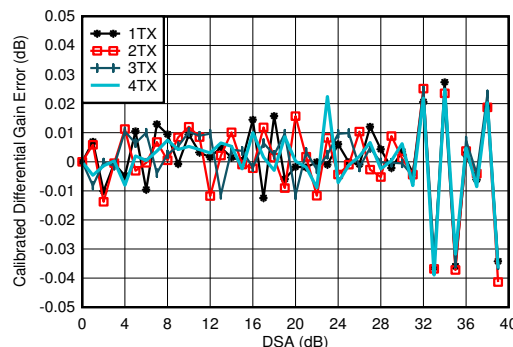
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{out}} = -0.5\text{dBFS}$, matching 0.8 GHz

Figure 7-280. TX Output Power vs DSA Setting and Channel at 0.85 GHz



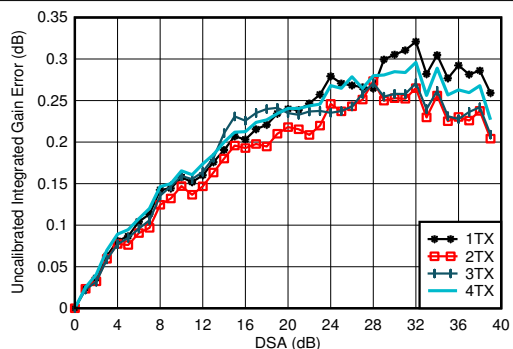
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-281. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



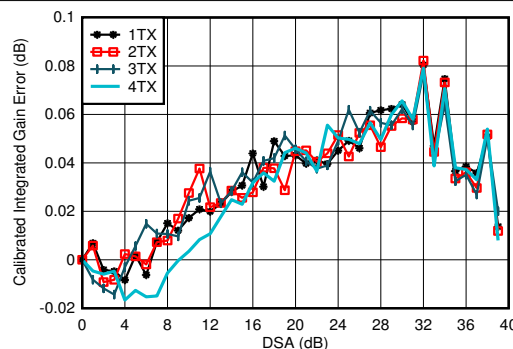
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-282. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Settings}$

Figure 7-283. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

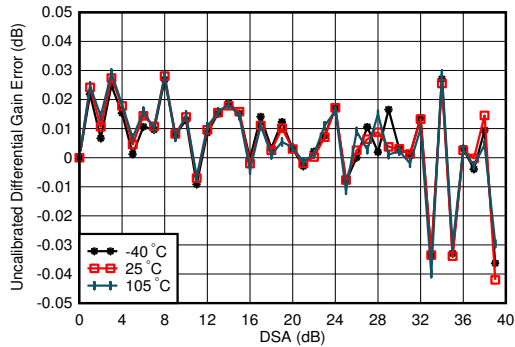
Figure 7-284. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

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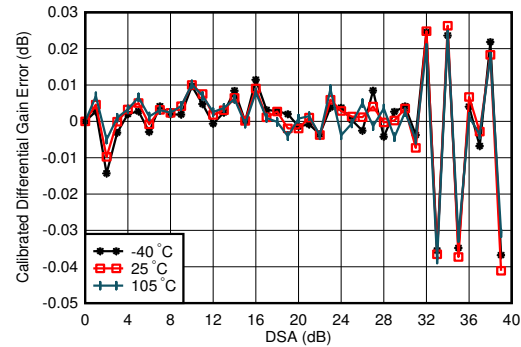
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7.12.8 TX Typical Characteristics at 800MHz (continued)

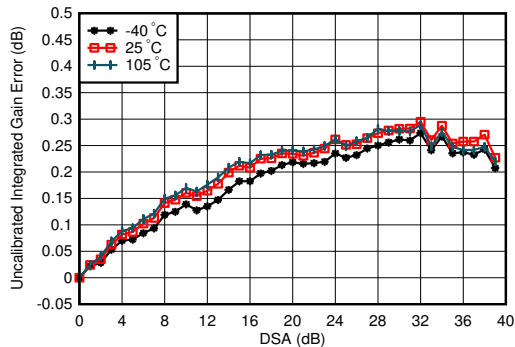
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



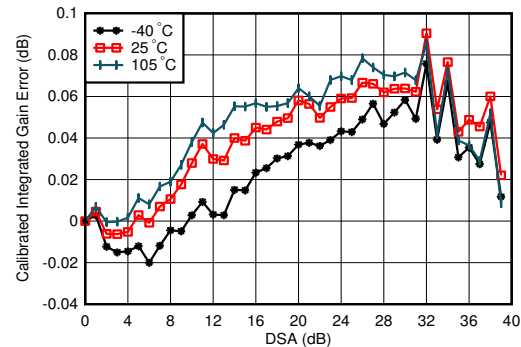
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-285. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz


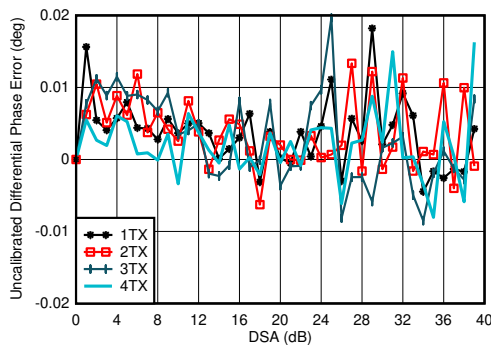
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-286. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz


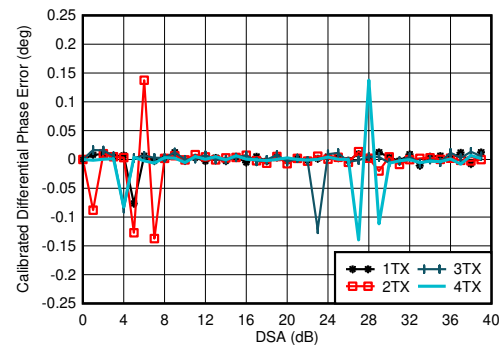
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

Figure 7-287. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz


$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

Figure 7-288. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz


$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

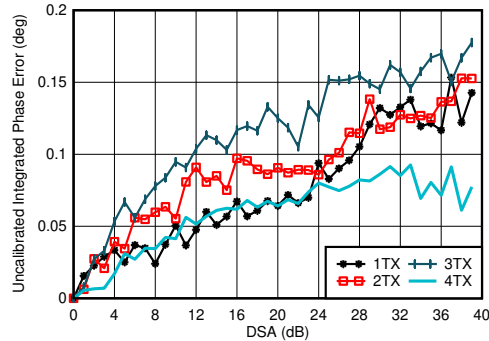
Figure 7-289. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz


$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
Phase DNL spike may occur at any DSA setting.

Figure 7-290. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

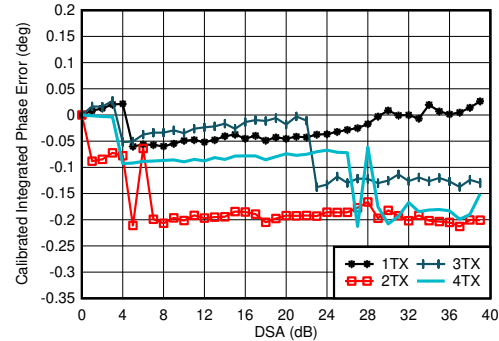
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



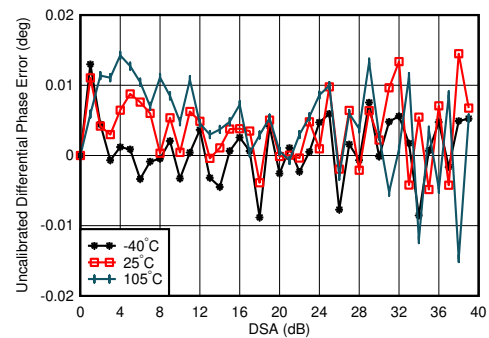
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

Figure 7-291. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



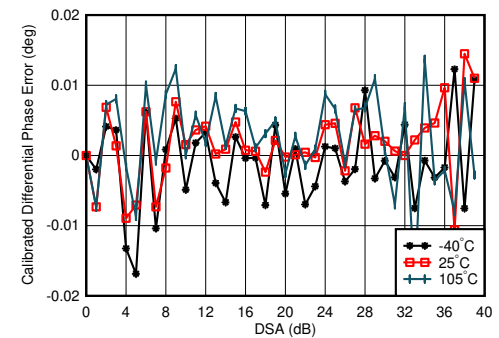
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

Figure 7-292. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



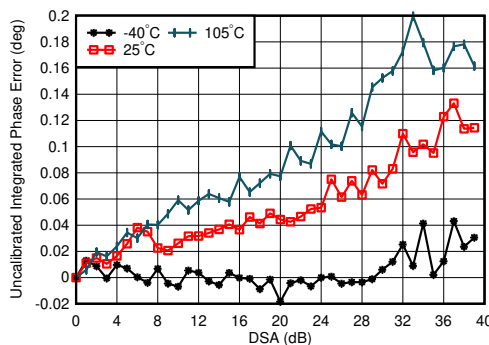
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-293. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



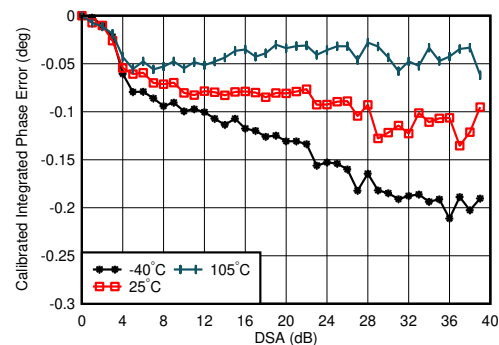
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-294. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

Figure 7-295. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

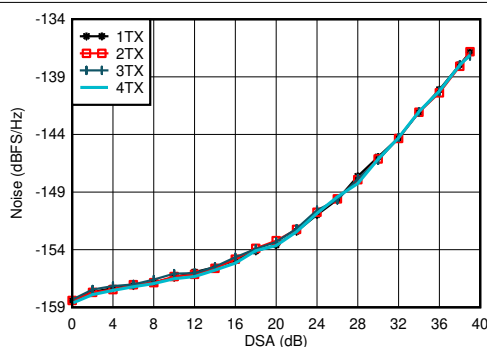
Figure 7-296. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz

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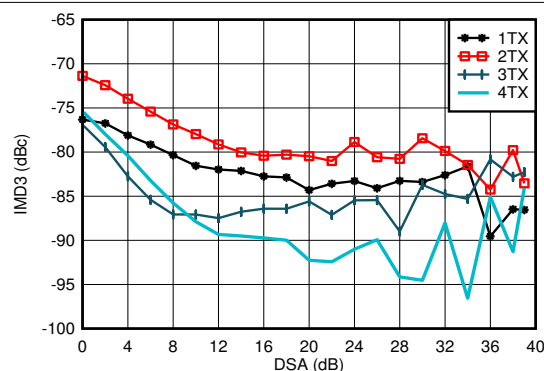
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



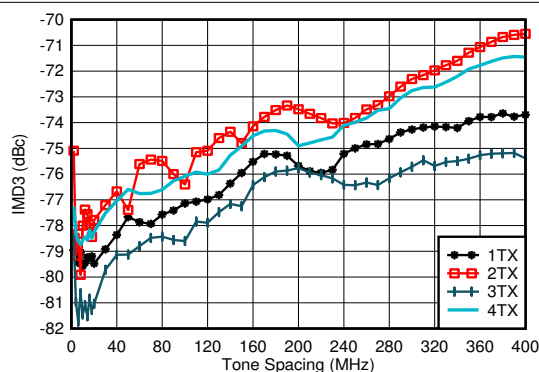
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, matching at 0.8 GHz,
 $P_{\text{OUT}} = -13\text{ dBFS}$

Figure 7-297. TX Output Noise vs Channel and Attenuation at 0.85 GHz



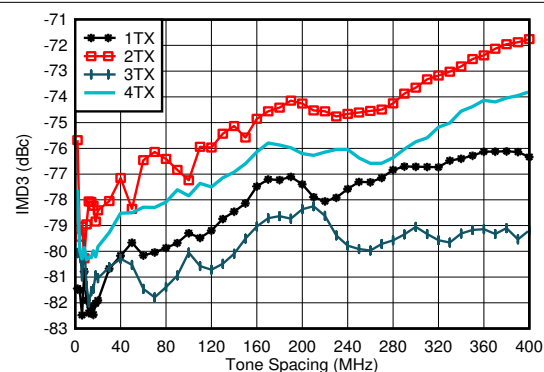
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$,
matching at 0.8 GHz, -13 dBFS each tone

Figure 7-298. TX IMD3 vs DSA Setting at 0.85 GHz



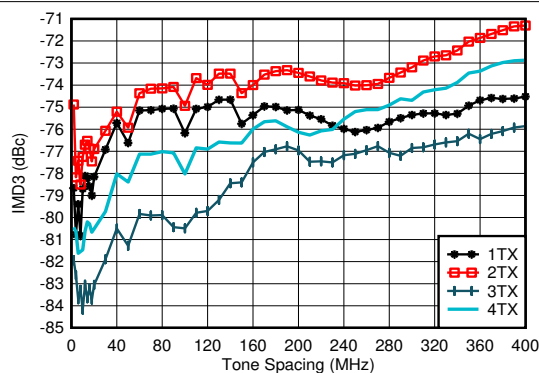
$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$,
matching at 0.8 GHz, -13 dBFS each tone

Figure 7-299. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



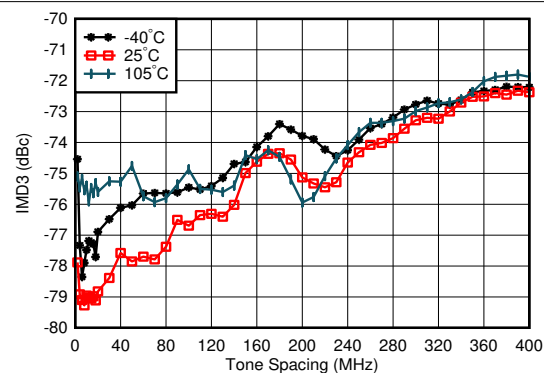
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$,
matching at 0.8 GHz, -13 dBFS each tone

Figure 7-300. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$,
matching at 0.8 GHz, -13 dBFS each tone

Figure 7-301. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz

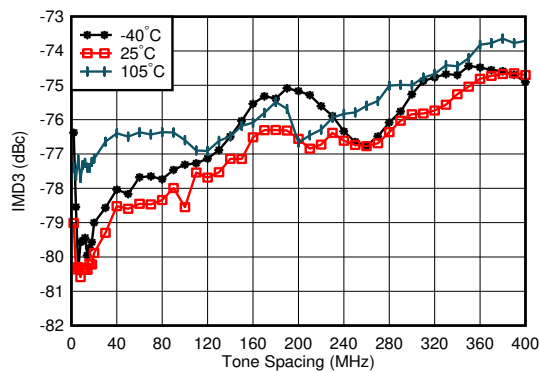


$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$,
matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 7-302. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

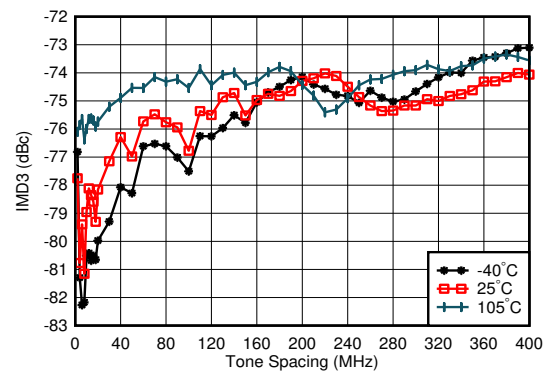
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



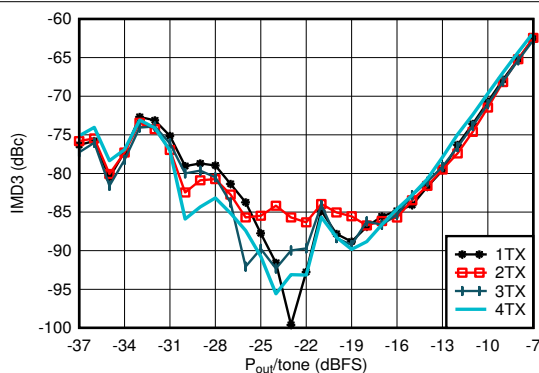
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$, matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 7-303. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



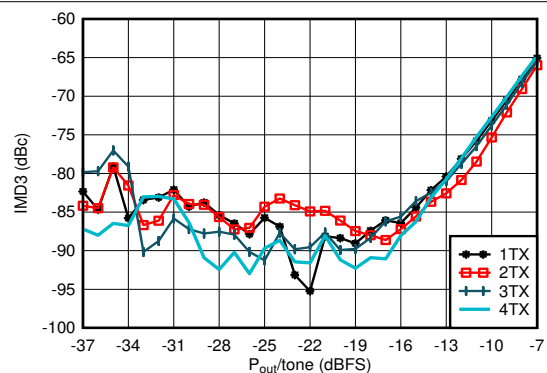
$f_{\text{DAC}} = 11796.48\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$, matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 7-304. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



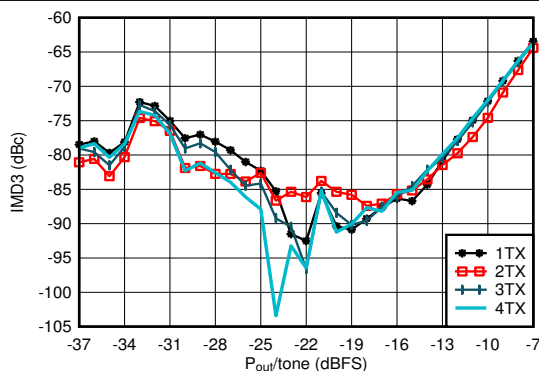
$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$, $f_{\text{SPACING}} = 20\text{ MHz}$, matching at 0.8 GHz

Figure 7-305. TX IMD3 vs Digital Level at 0.85 GHz



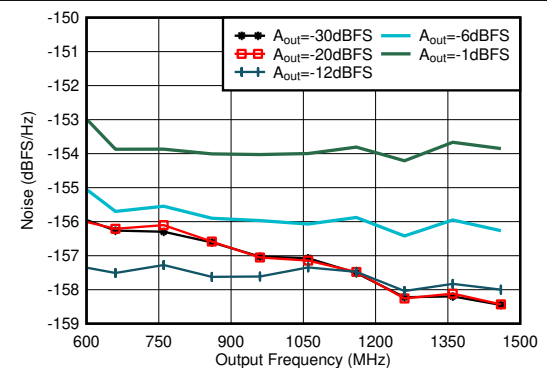
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$, $f_{\text{SPACING}} = 20\text{ MHz}$, matching at 0.8 GHz

Figure 7-306. TX IMD3 vs Digital Level at 0.85 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $f_{\text{CENTER}} = 0.85\text{ GHz}$, $f_{\text{SPACING}} = 20\text{ MHz}$, matching at 0.8 GHz

Figure 7-307. TX IMD3 vs Digital Level at 0.85 GHz



Matching at 0.8 GHz, Single tone, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, 40-MHz offset, DSA = 0dB

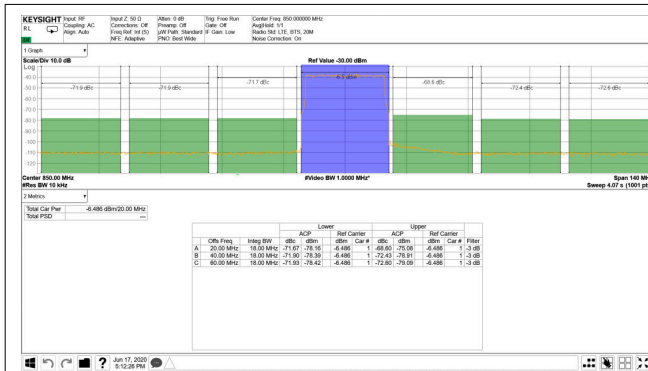
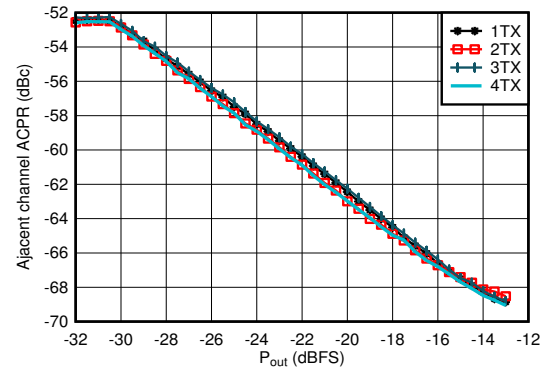
Figure 7-308. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz

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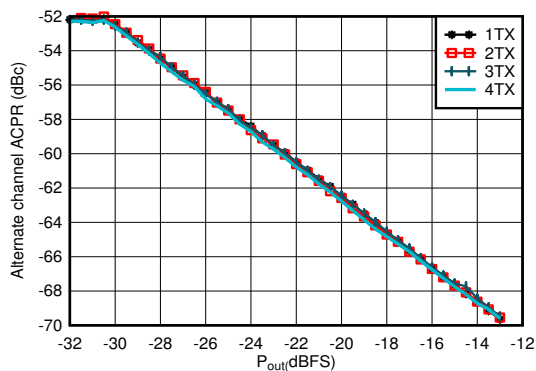
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7.12.8 TX Typical Characteristics at 800MHz (continued)

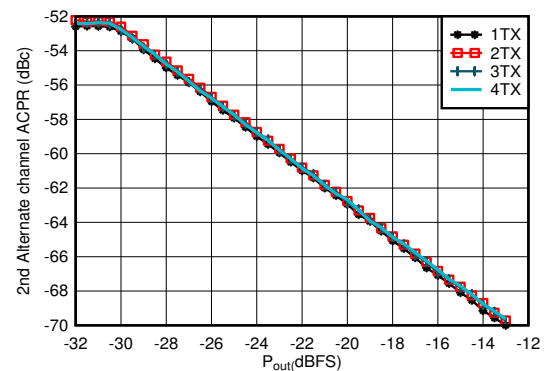
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

TM1.1, $P_{\text{OUT_RMS}} = -13\text{ dBFS}$ **Figure 7-309. TX 20-MHz LTE Output Spectrum at 0.85 GHz**

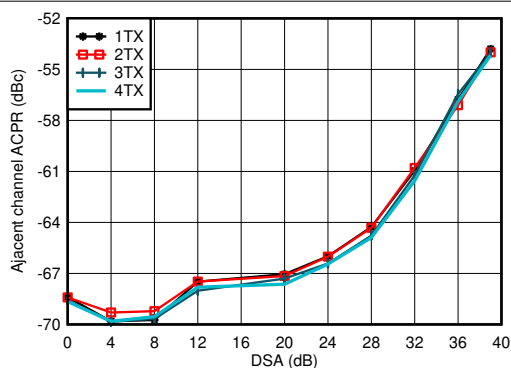
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-310. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz

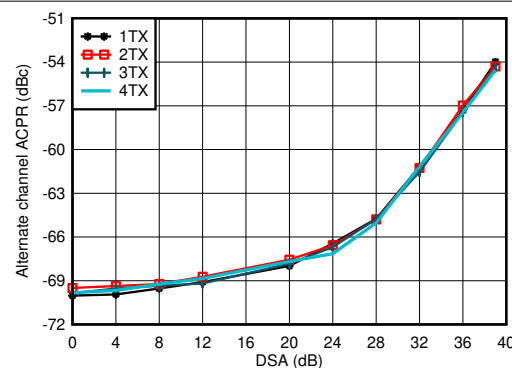
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-311. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz

Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-312. TX 20-MHz LTE alt2-ACPR vs Digital Level at 0.85 GHz

Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

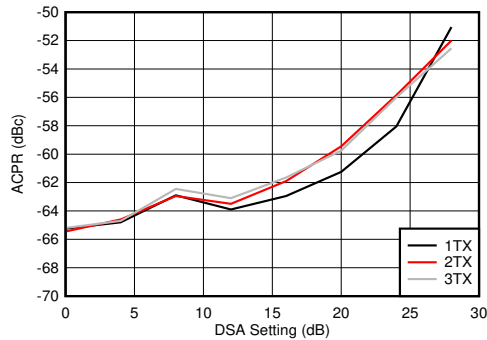
Figure 7-313. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz

Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-314. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz

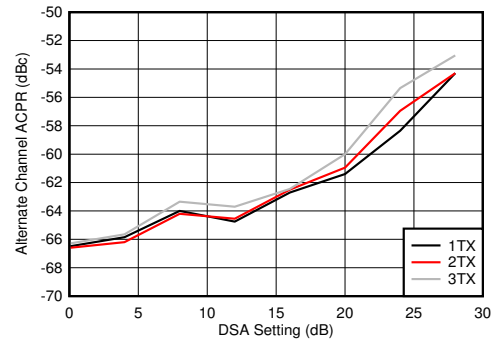
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



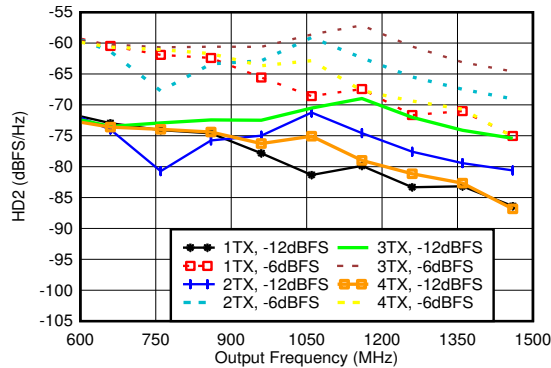
Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-315. TX 100-MHz NR ACPR vs DSA at 0.85 GHz



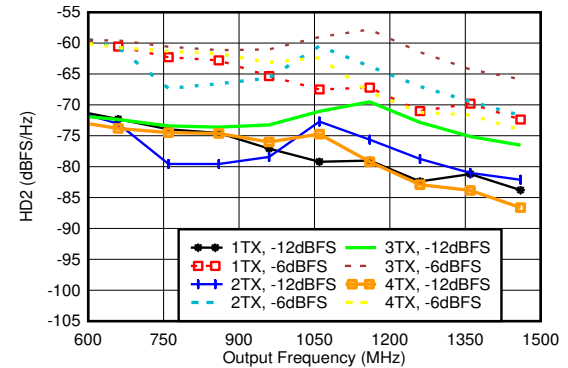
Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-316. TX 100-MHz NR alt-ACPR vs DSA at 0.85 GHz



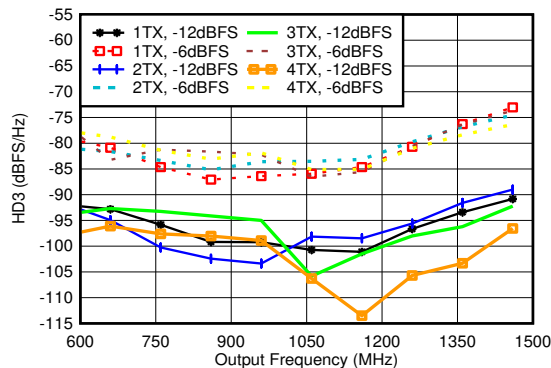
Matching at 0.8 GHz, $f_{\text{DAC}} = 5898.24\text{GSPS}$, straight mode

Figure 7-317. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



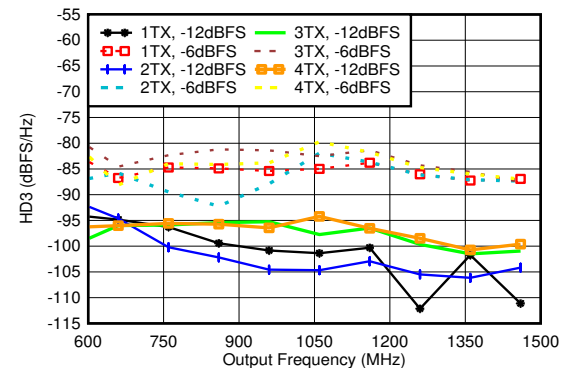
Matching at 0.8 GHz, $f_{\text{DAC}} = 8847.36\text{GSPS}$, straight mode

Figure 7-318. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



Matching at 0.8 GHz, $f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, normalized to output power at harmonic frequency

Figure 7-319. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



Matching at 0.8 GHz, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, normalized to output power at harmonic frequency

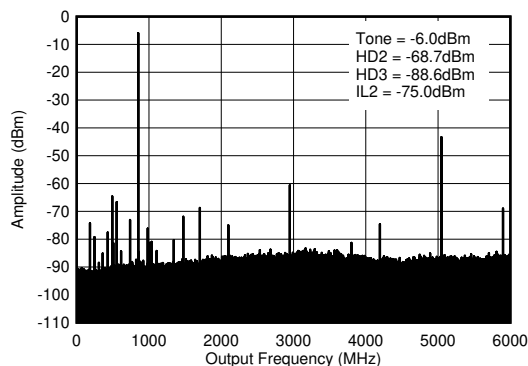
Figure 7-320. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz

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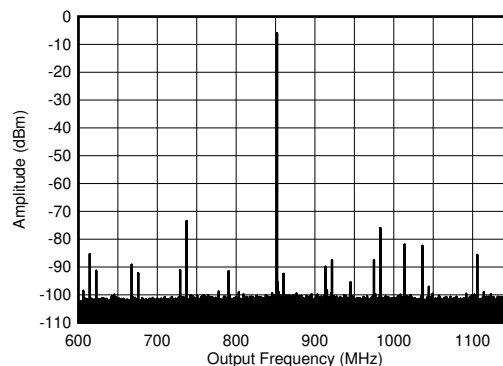
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



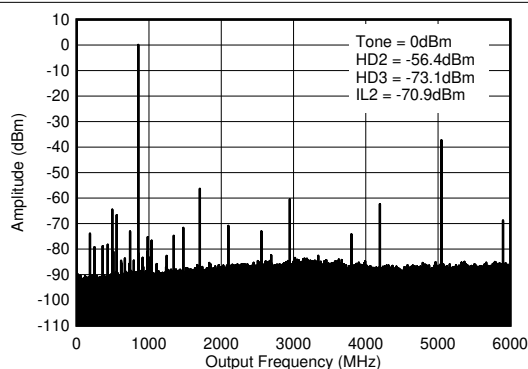
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-321. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)



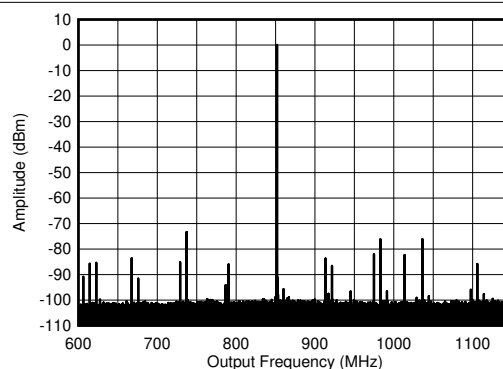
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 7-322. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ($\pm 300\text{ MHz}$)



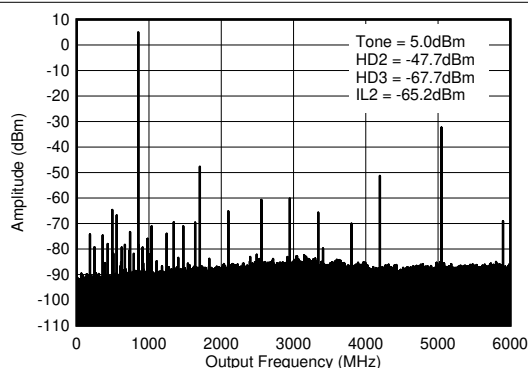
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-323. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)



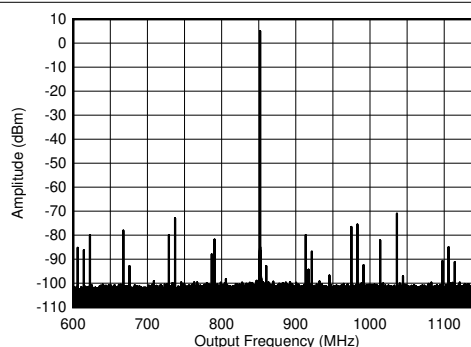
$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 7-324. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ($\pm 300\text{ MHz}$)



$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-325. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)

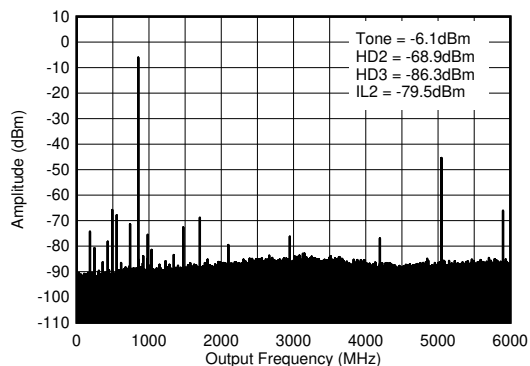


$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode, 0.8 GHz matching, includes PCB and cable losses

Figure 7-326. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ($\pm 300\text{ MHz}$)

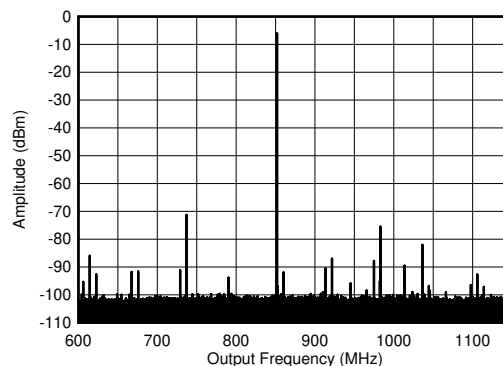
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



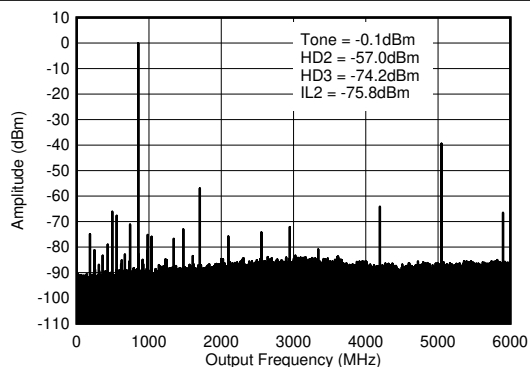
$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILN} = f_{\text{S}}/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-327. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)



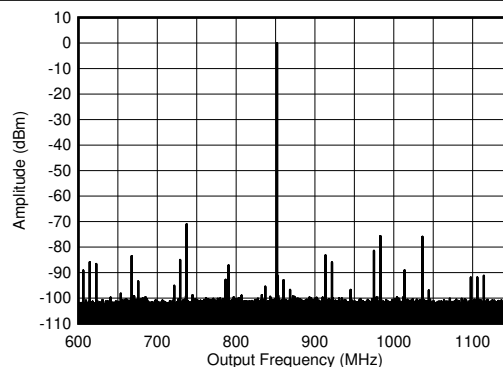
$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 7-328. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ($\pm 300\text{ MHz}$)



$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILN} = f_{\text{S}}/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-329. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, 0.8 GHz matching, includes PCB and cable losses

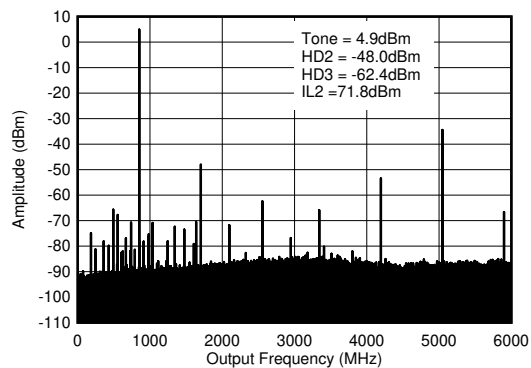
Figure 7-330. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ($\pm 300\text{ MHz}$)

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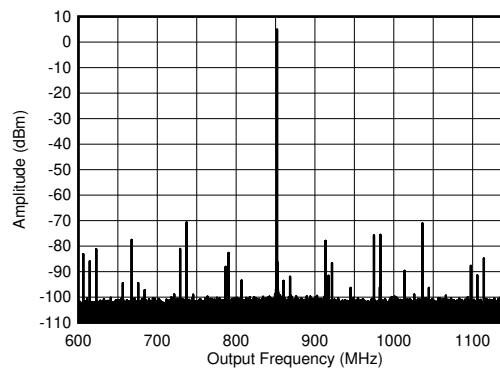
7.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-331. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)

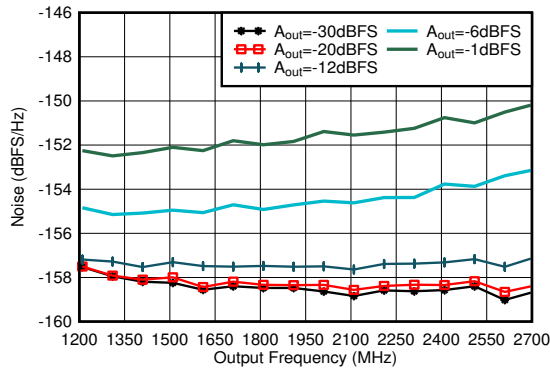


$f_{\text{DAC}} = 5898.24\text{MSPS}$, straight mode, 0.8 GHz matching, includes PCB and cable losses

Figure 7-332. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ($\pm 300\text{ MHz}$)

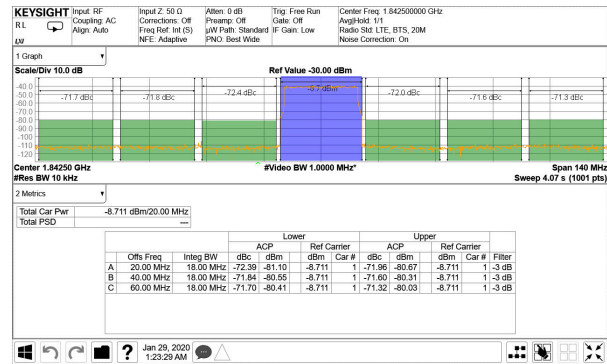
7.12.9 TX Typical Characteristics at 1.8GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



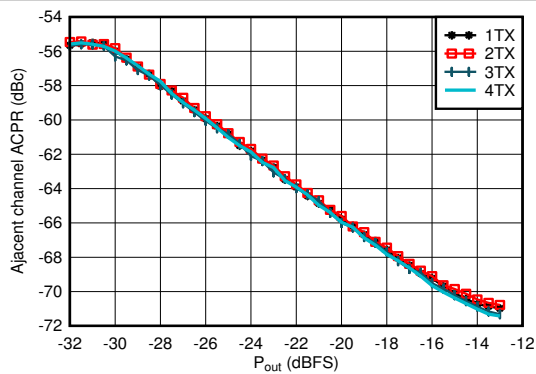
Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, 40-MHz offset

Figure 7-333. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



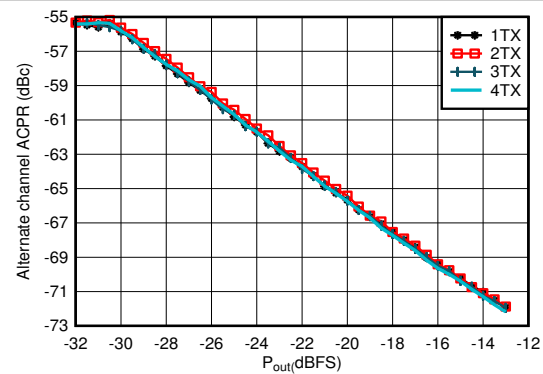
TM1.1, $P_{\text{OUT_RMS}} = -13\text{ dBFS}$

Figure 7-334. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



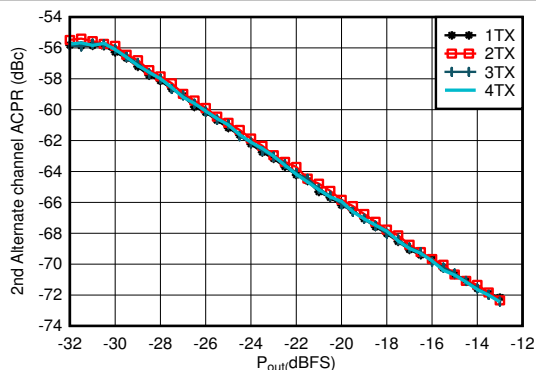
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-335. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



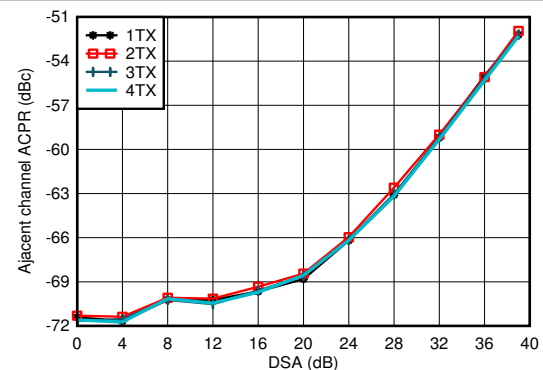
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-336. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-337. TX 20-MHz LTE alt2-ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

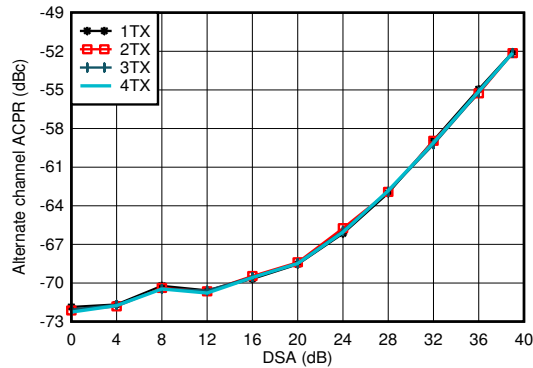
Figure 7-338. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

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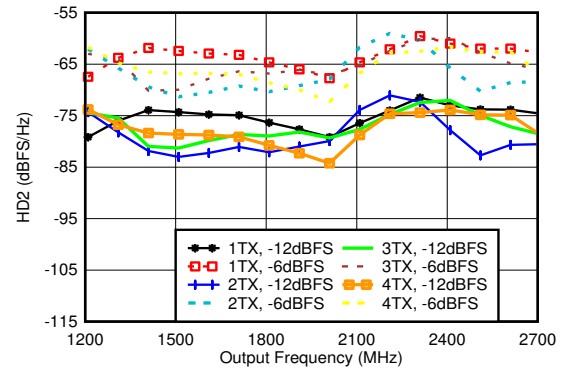
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7.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

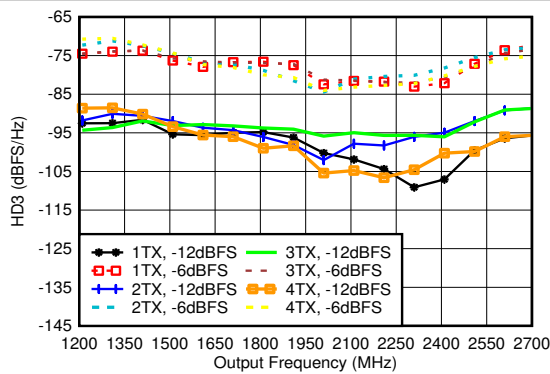


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE
Figure 7-339. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



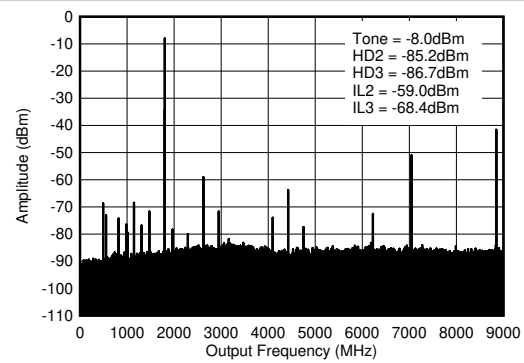
Matching at 1.8 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency

Figure 7-340. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



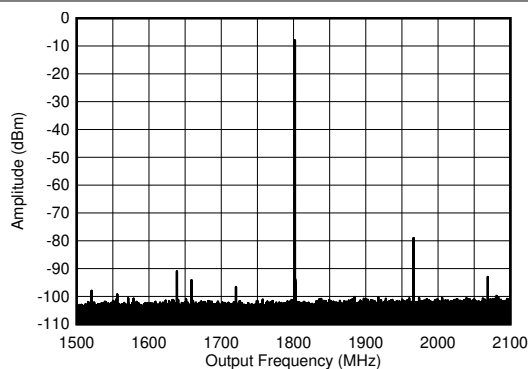
Matching at 1.8 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency

Figure 7-341. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz



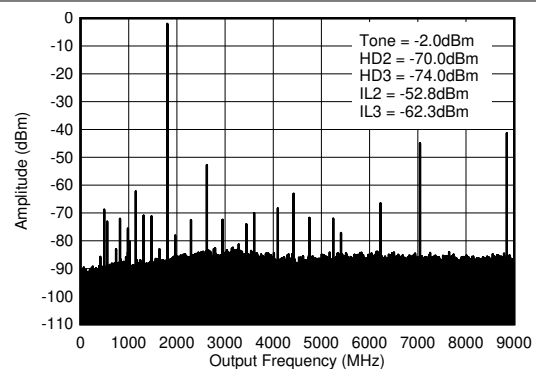
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$.

Figure 7-342. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 7-343. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ($\pm 300\text{ MHz}$)

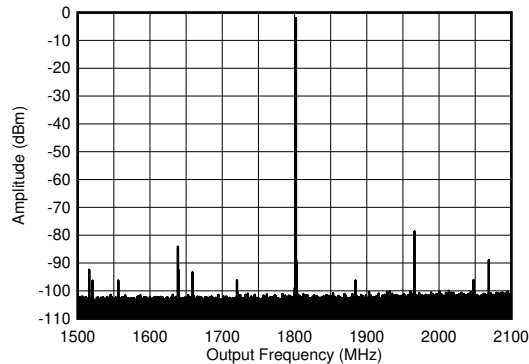


$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$.

Figure 7-344. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)

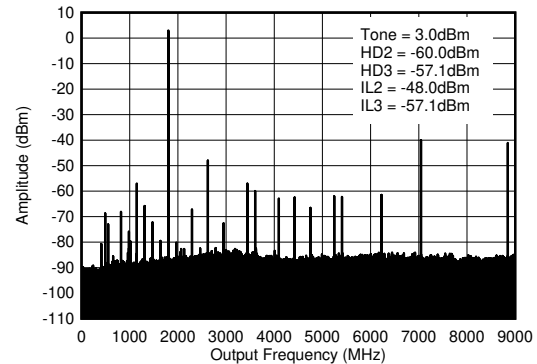
7.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



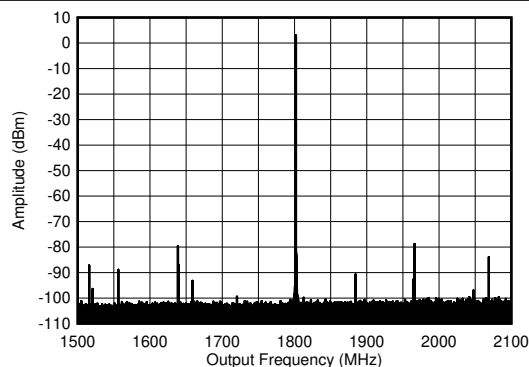
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 7-345. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ($\pm 300\text{ MHz}$)



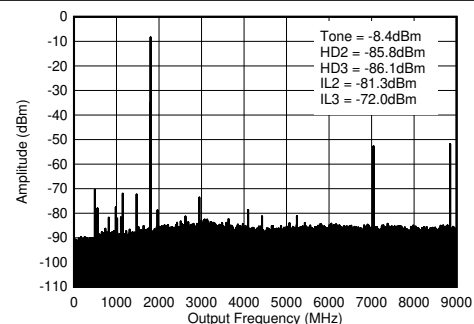
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 1.8 GHz matching, includes PCB and cable losses. $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$.

Figure 7-346. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)



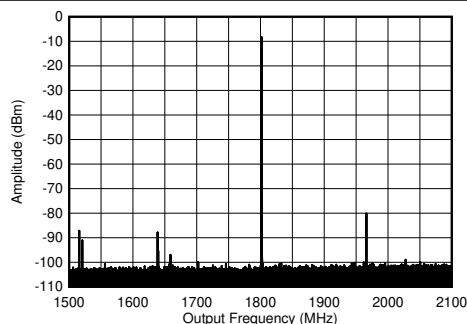
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 1.8 GHz matching, includes PCB and cable losses

Figure 7-347. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ($\pm 300\text{ MHz}$)



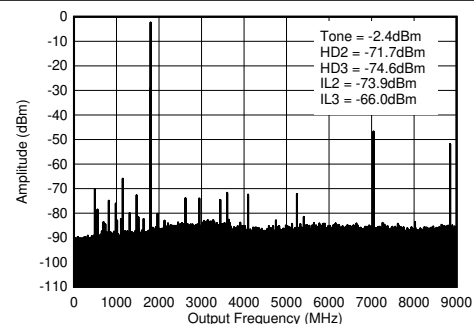
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-348. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 7-349. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ($\pm 300\text{ MHz}$)



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

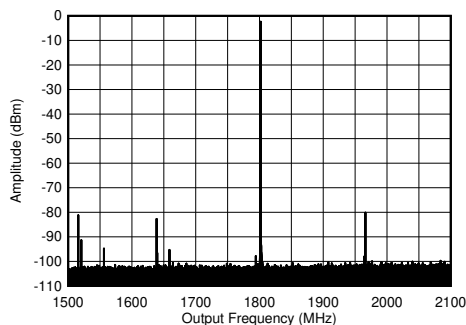
Figure 7-350. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)

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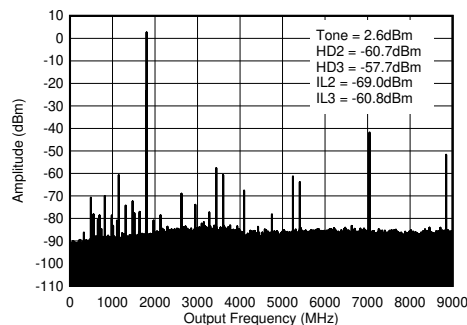
7.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



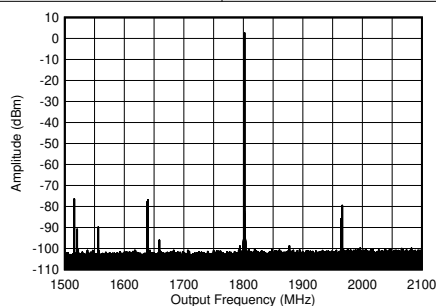
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 7-351. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ($\pm 300\text{ MHz}$)



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-352. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)

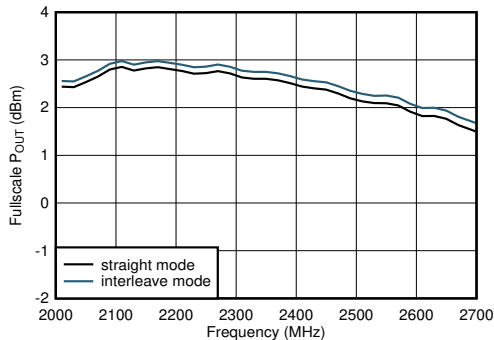


$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 1.8 GHz matching, includes PCB and cable losses

Figure 7-353. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ($\pm 300\text{ MHz}$)

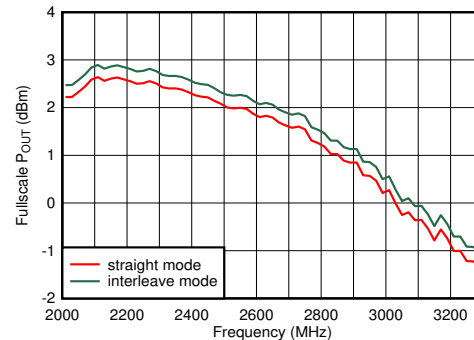
7.12.10 TX Typical Characteristics at 2.6GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



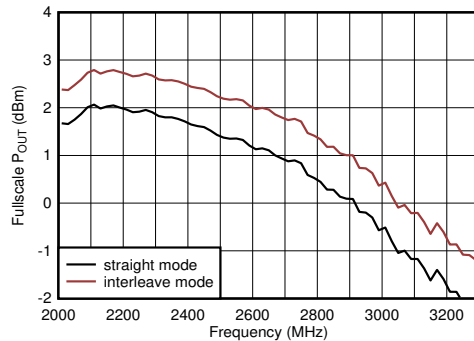
Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 2.6 GHz matching

Figure 7-354. TX Full Scale vs RF Frequency at 5898.24MSPS



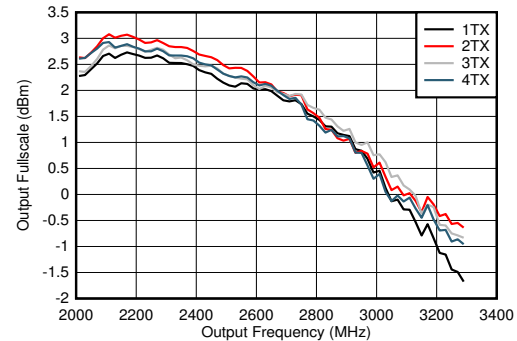
Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 2.6 GHz matching

Figure 7-355. TX Full Scale vs RF Frequency at 8847.36MSPS



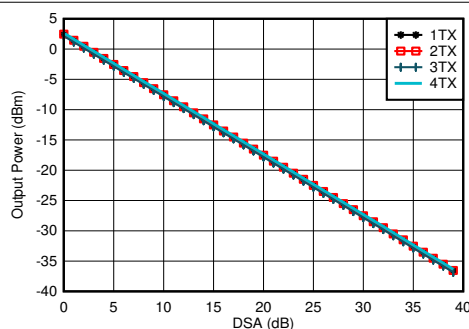
Including PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 2.6 GHz matching

Figure 7-356. TX Full Scale vs RF Frequency at 11796.48MSPS



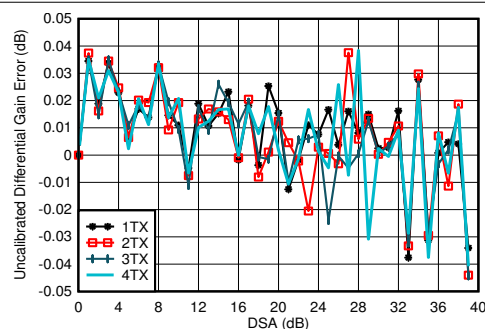
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, including PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 2.6 GHz matching

Figure 7-357. TX Output Fullscale vs Output Frequency and Channel



$f_{\text{DAC}} = 8847.36\text{ MSPS}$, $A_{\text{out}} = -0.5\text{dBFS}$, matching 2.6 GHz

Figure 7-358. TX Output Power vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz

Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

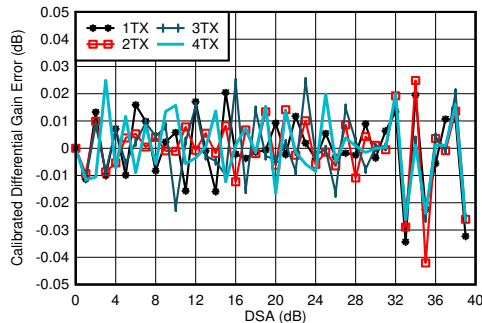
Figure 7-359. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz

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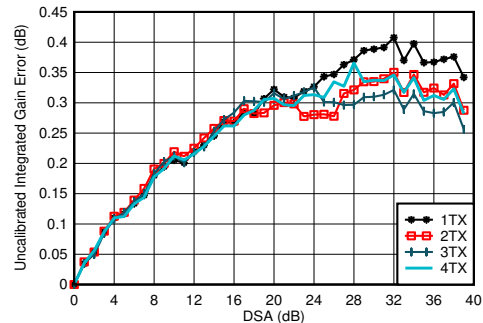
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



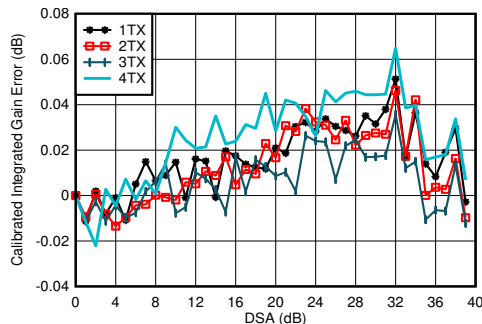
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-360. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



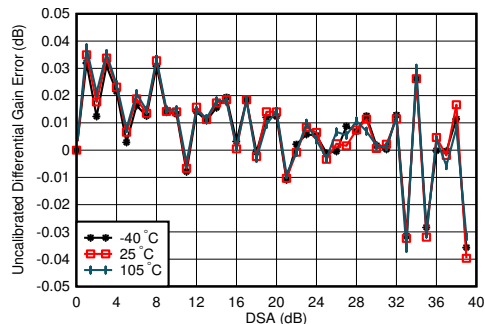
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-361. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



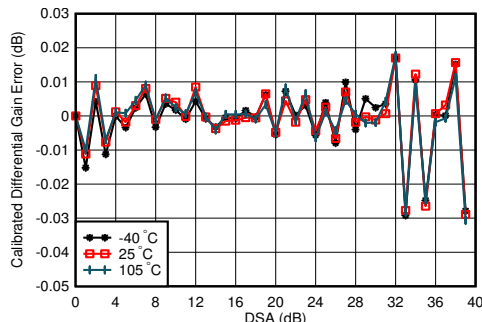
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-362. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



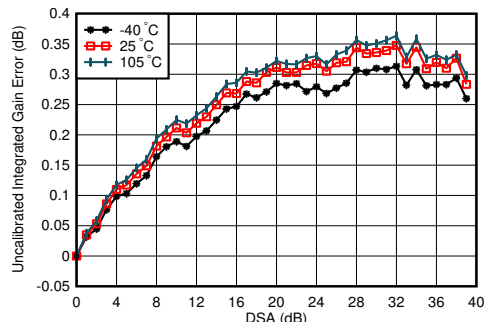
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-363. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-364. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz

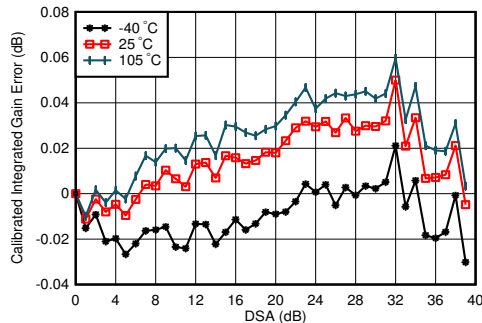


$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-365. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

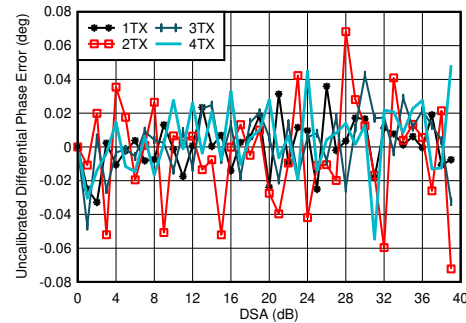
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



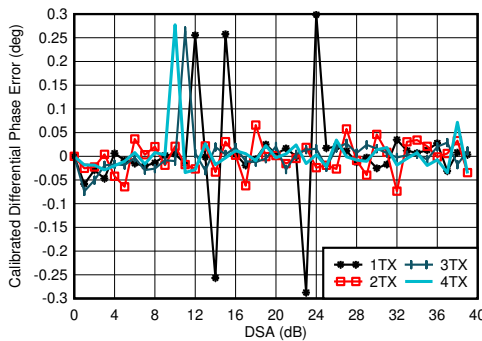
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-366. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



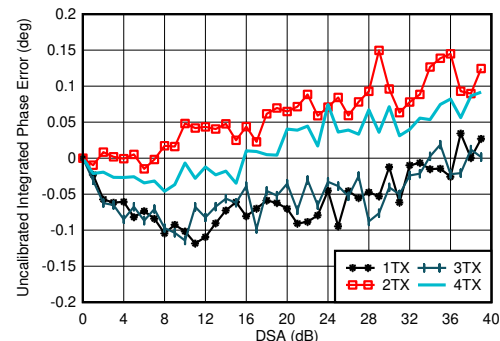
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-367. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
Phase DNL spike may occur at any DSA setting.

Figure 7-368. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

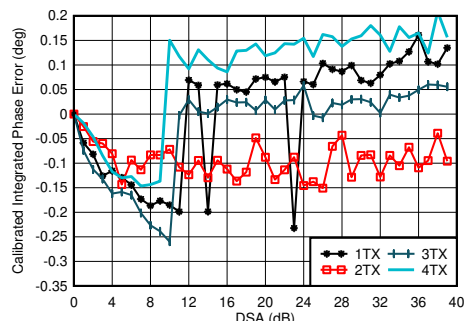
Figure 7-369. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

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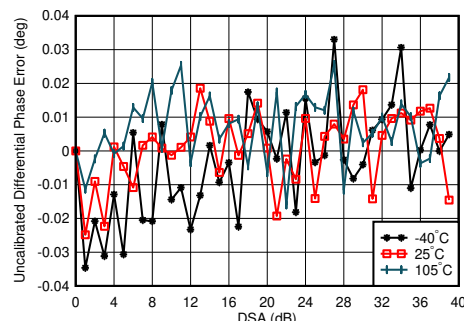
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



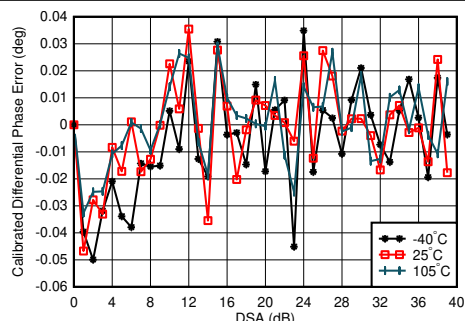
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-370. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz



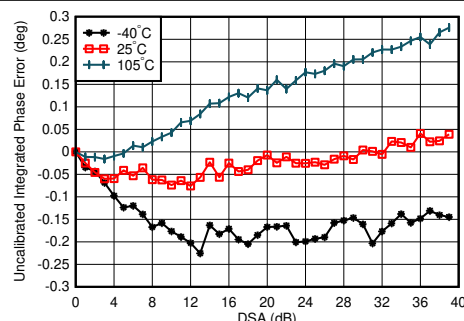
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz,
channel with the median variation over DSA setting at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-371. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



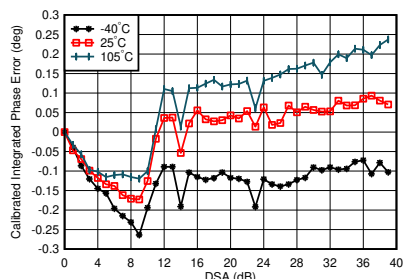
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz,
channel with the median variation over DSA setting at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-372. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



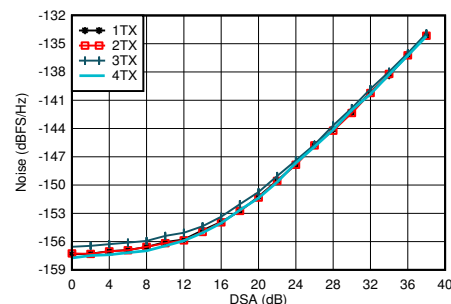
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz,
channel with the median variation over DSA setting at 25°C
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-373. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz,
channel with the median variation over DSA setting at 25°C
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-374. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz

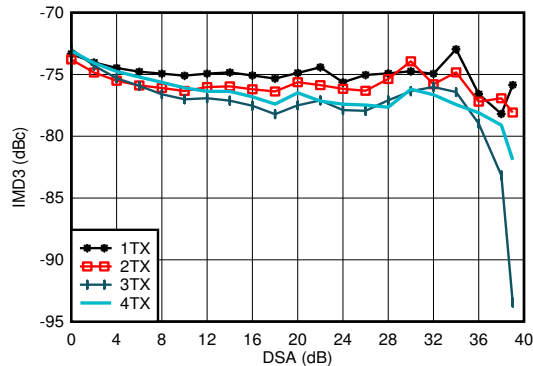


$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, matching at 2.6 GHz,
 $P_{\text{OUT}} = -13\text{ dBFS}$

Figure 7-375. TX Output Noise vs Channel and Attenuation at 2.6 GHz

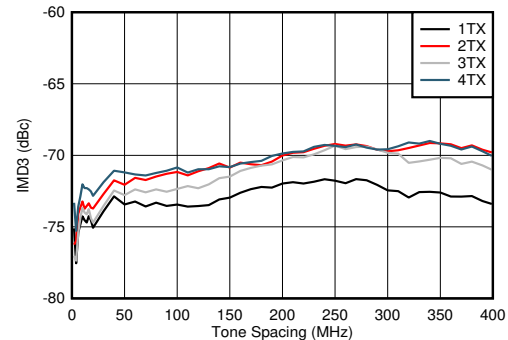
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



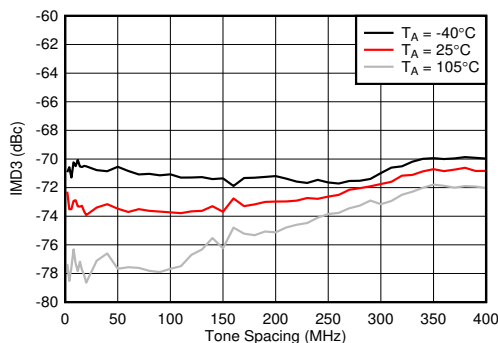
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 2.6\text{ GHz}$, matching at 2.6 GHz, -13 dBFS each tone

Figure 7-376. TX IMD3 vs DSA Setting at 2.6 GHz



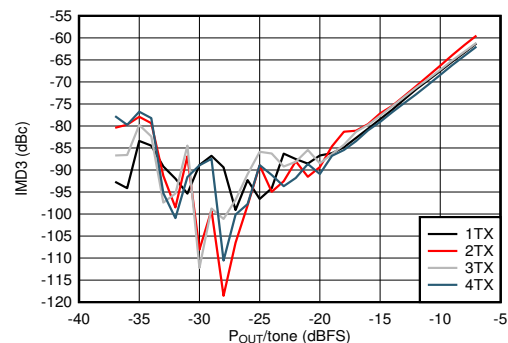
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 2.6\text{ GHz}$, matching at 2.6 GHz, -13 dBFS each tone

Figure 7-377. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



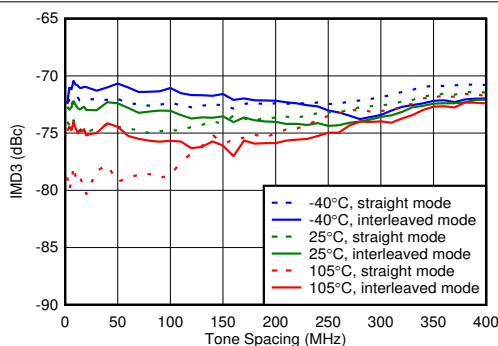
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 2.6\text{ GHz}$, matching at 2.6 GHz, -13 dBFS each tone, worst channel, dither = 1.

Figure 7-378. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



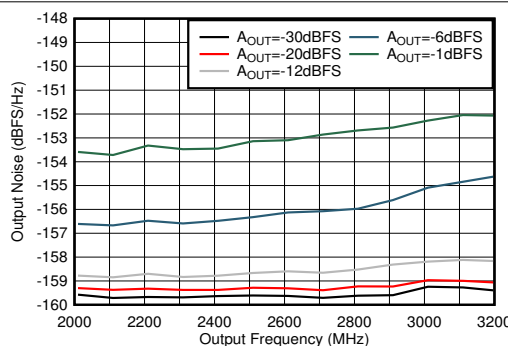
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 2.6\text{ GHz}$, $f_{\text{SPACING}} = 20\text{ MHz}$, dither = 1, matching at 2.6 GHz

Figure 7-379. TX IMD3 vs Digital Level at 2.6 GHz



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, $f_{\text{CENTER}} = 2.6\text{ GHz}$, matching at 2.6 GHz, -13 dBFS each tone

Figure 7-380. TX IMD3 vs Tone Spacing and Temperature



Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, 40-MHz offset

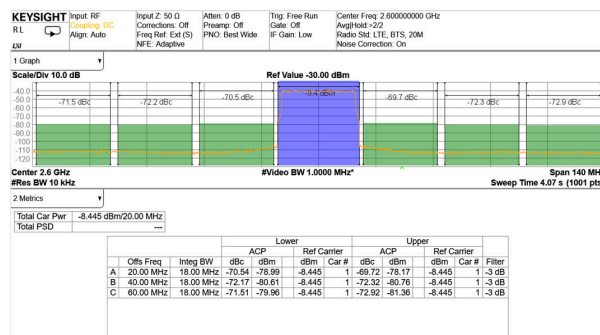
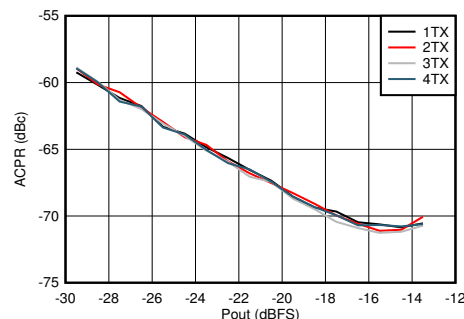
Figure 7-381. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz

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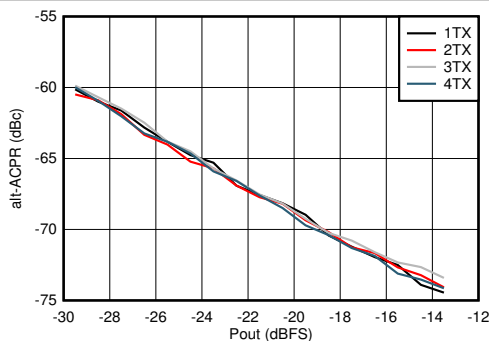
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7.12.10 TX Typical Characteristics at 2.6GHz (continued)

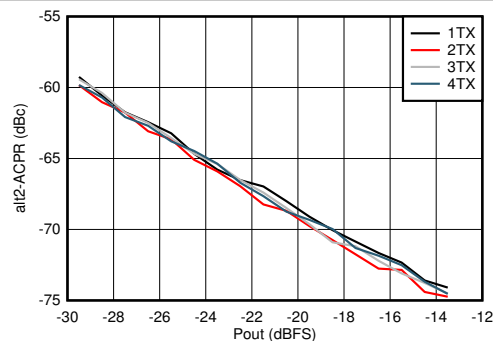
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

TM1.1, $P_{\text{OUT,RMS}} = -13\text{ dBFS}$ **Figure 7-382. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)**

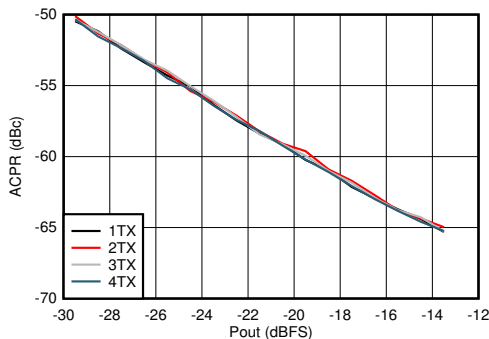
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-383. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz

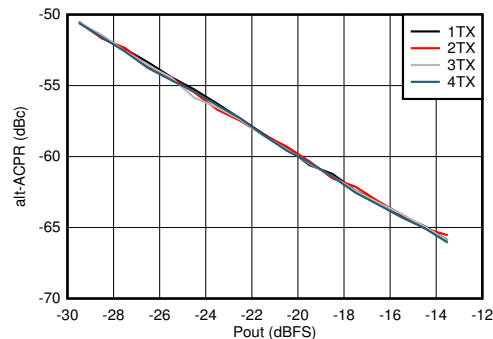
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-384. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz

Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-385. TX 20-MHz LTE alt2-ACPR vs Digital Level at 2.6 GHz

Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

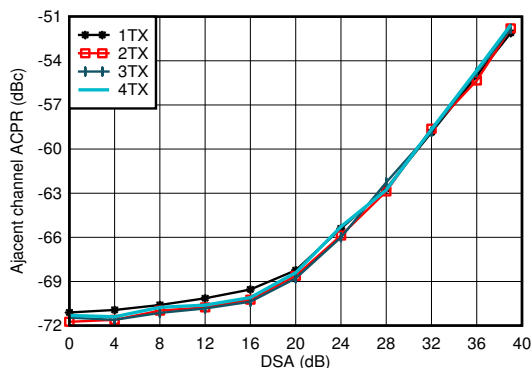
Figure 7-386. TX 100-MHz NR ACPR vs Digital Level at 2.6 GHz

Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-387. TX 100-MHz NR alt-ACPR vs Digital Level at 2.6 GHz

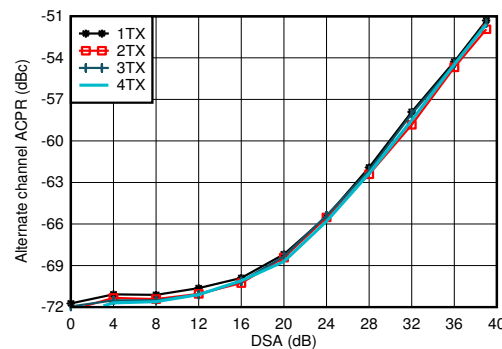
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



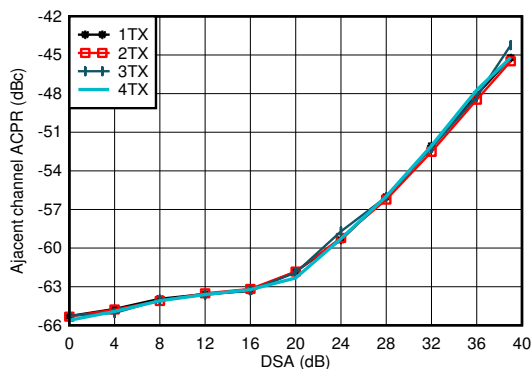
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-388. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



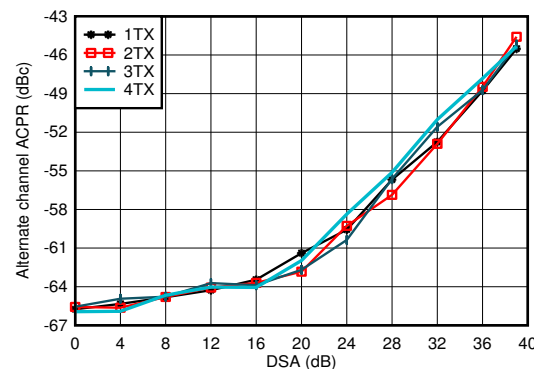
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-389. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



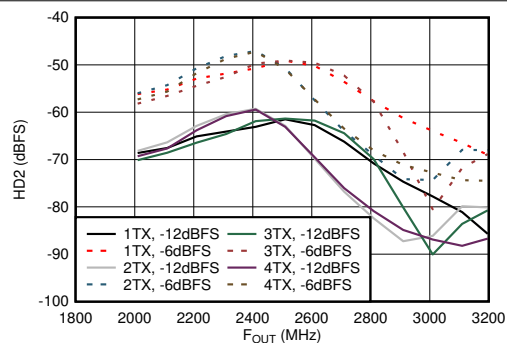
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-390. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



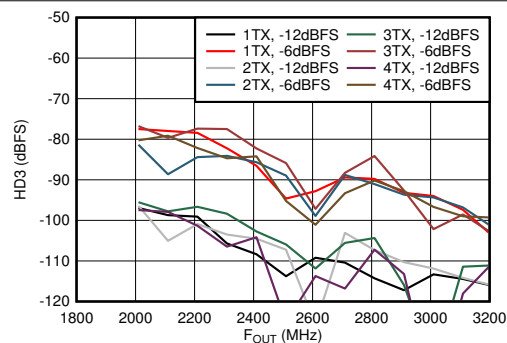
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-391. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency

Figure 7-392. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz



Matching at 2.6 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency

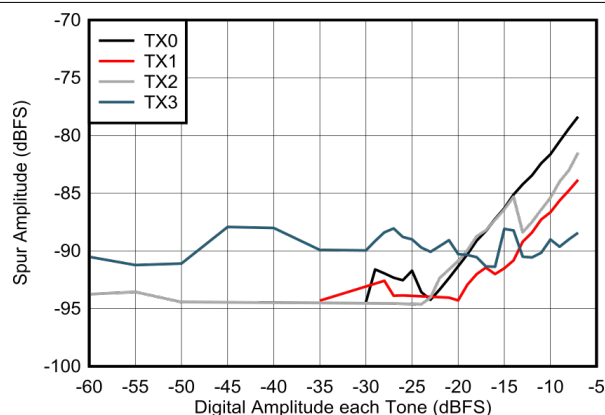
Figure 7-393. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz

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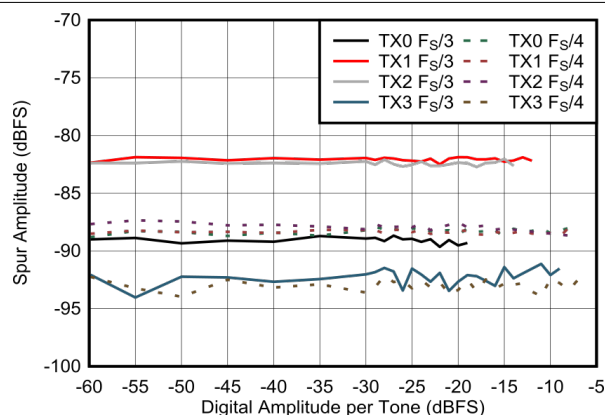
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



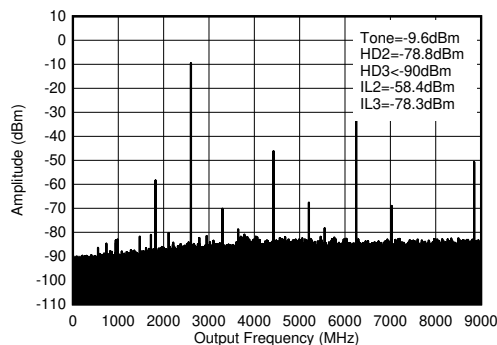
Inband = $2600\text{MHz} \pm 600\text{MHz}$, $f_{\text{DAC}} = 12\text{GSPS}$, not including $F_S/3$ and $F_S/4$, external clock mode, non-interleave mode

Figure 7-394. Two Tone Inband SFDR vs Digital Amplitude at 2.6 GHz



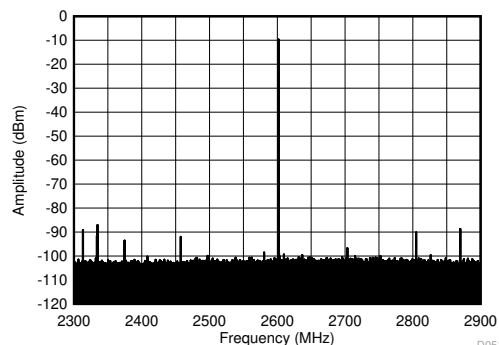
Inband = $2600\text{MHz} \pm 600\text{MHz}$, $f_{\text{DAC}} = 12\text{GSPS}$, external clock mode, non-interleave mode

Figure 7-395. Two Tone Inband Fixed Spurs vs Digital Amplitude at 2.6 GHz



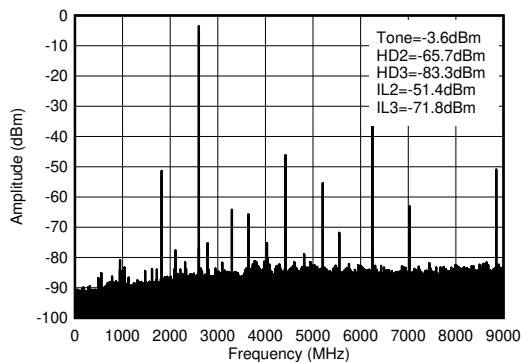
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_S/n \pm f_{\text{OUT}}$.

Figure 7-396. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)



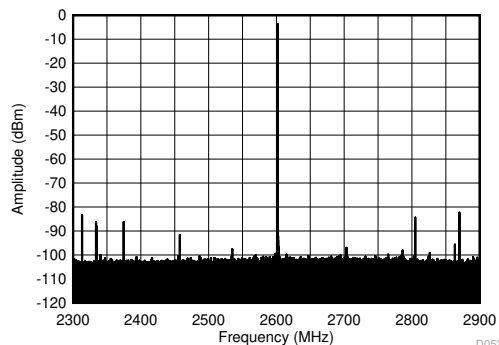
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 7-397. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ($\pm 300\text{ MHz}$)



$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_S/n \pm f_{\text{OUT}}$.

Figure 7-398. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)

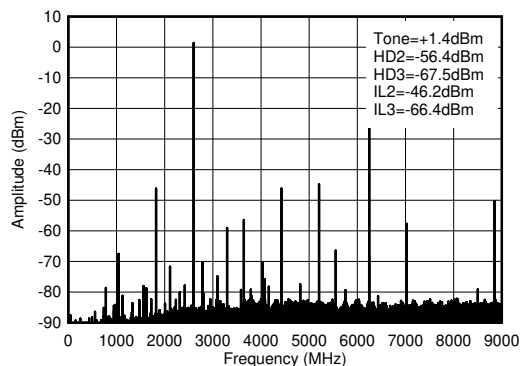


$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 7-399. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ($\pm 300\text{ MHz}$)

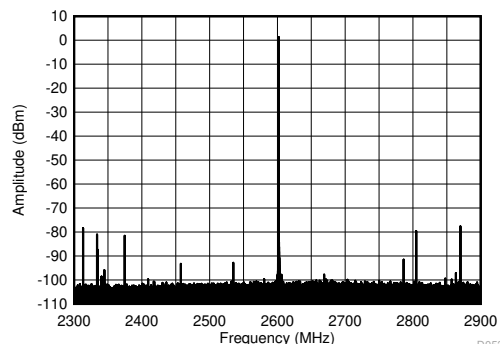
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



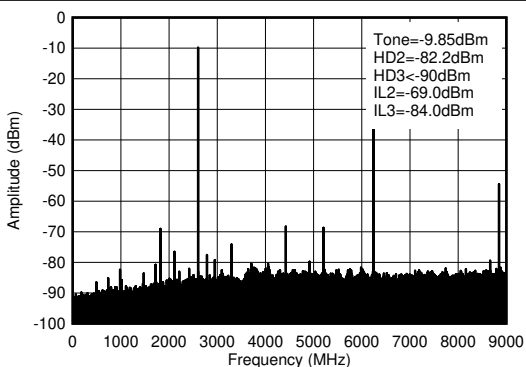
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-400. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)



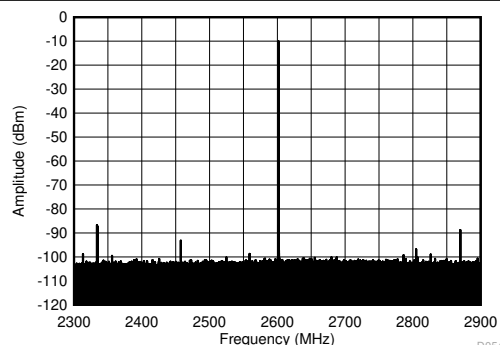
$f_{\text{DAC}} = 8847.36\text{MSPS}$, interleave mode, 2.6 GHz matching, includes PCB and cable losses

Figure 7-401. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ($\pm 300\text{ MHz}$)



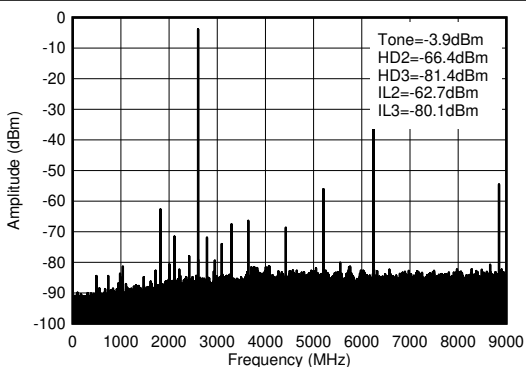
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-402. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)



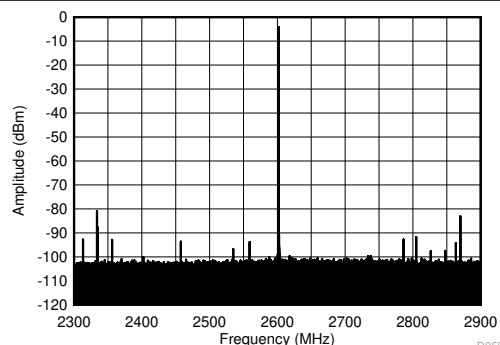
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 7-403. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ($\pm 300\text{ MHz}$)



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-404. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 2.6 GHz matching, includes PCB and cable losses

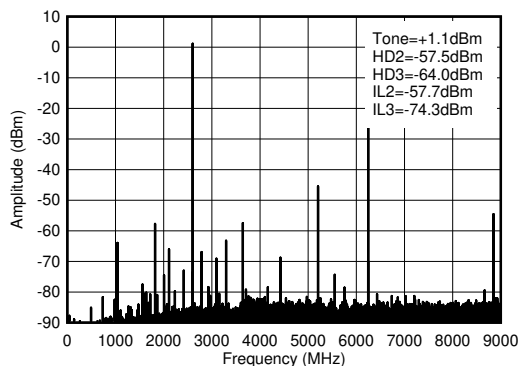
Figure 7-405. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ($\pm 300\text{ MHz}$)

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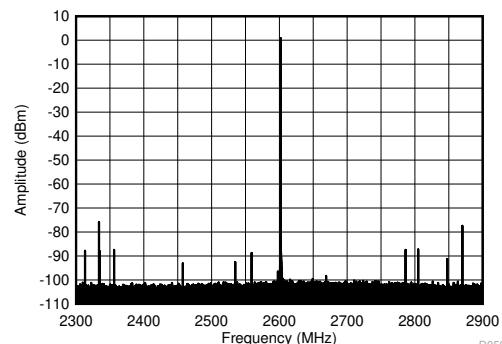
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



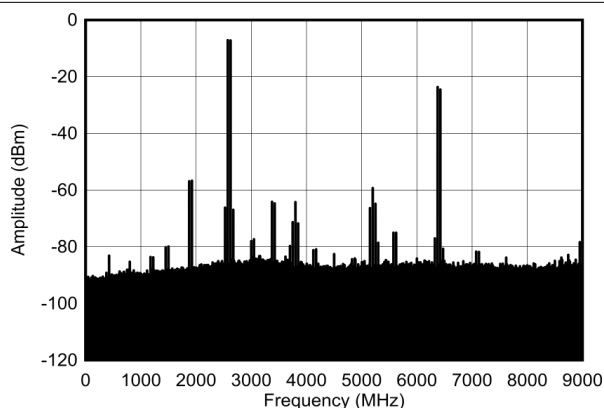
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-406. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ($0 - f_{\text{DAC}}$)



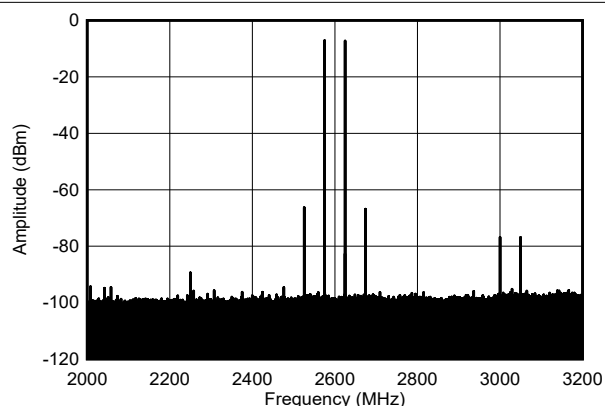
$f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode, 2.6 GHz matching, includes PCB and cable losses

Figure 7-407. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ($\pm 300\text{ MHz}$)



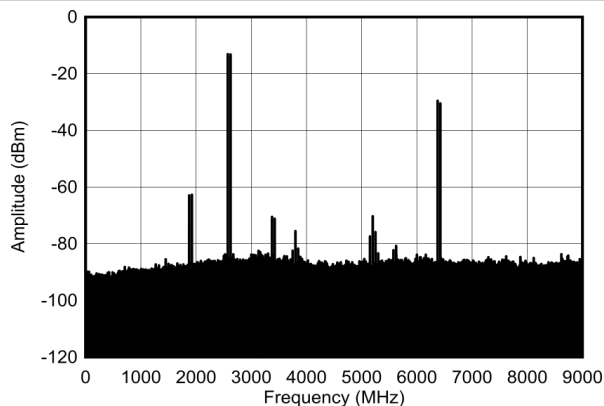
$f_{\text{DAC}} = 9000\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-408. TX Dual Tone Output Spectrum at 2.6 GHz, -7dBFS each ($0 - f_{\text{DAC}}$)



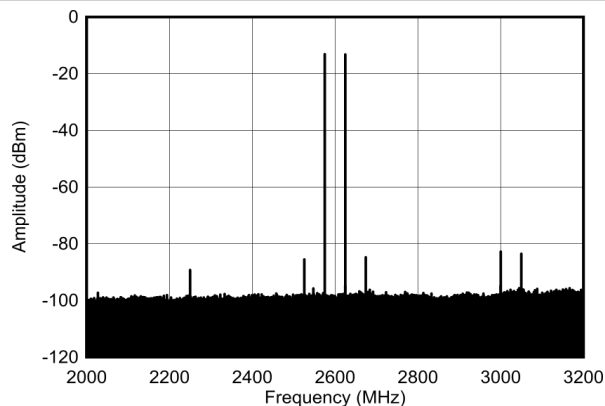
$f_{\text{DAC}} = 9000\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-409. TX Dual Tone Output Spectrum at 2.6 GHz, -7dBFS each ($\pm 600\text{ MHz}$)



$f_{\text{DAC}} = 9000\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-410. TX Dual Tone Output Spectrum at 2.6 GHz, -13dBFS each ($0 - f_{\text{DAC}}$)

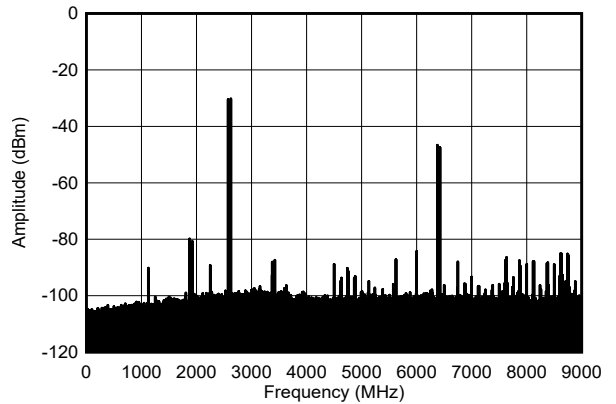


$f_{\text{DAC}} = 9000\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-411. TX Dual Tone Output Spectrum at 2.6 GHz, -13dBFS each ($\pm 600\text{ MHz}$)

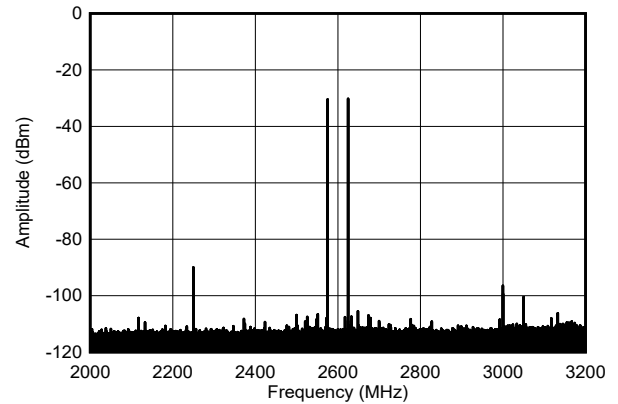
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



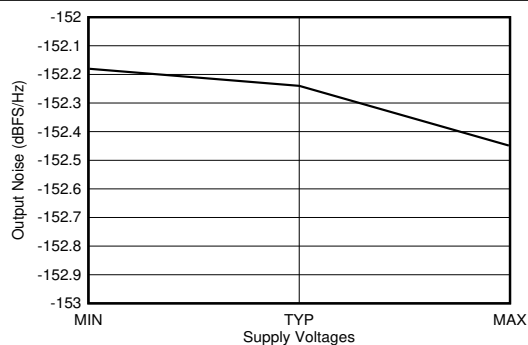
$f_{\text{DAC}} = 9000\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-412. TX Dual Tone Output Spectrum at 2.6 GHz, -30dBFS each (0 - DAC)



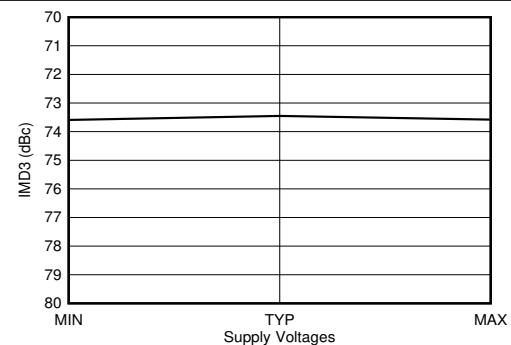
$f_{\text{DAC}} = 9000\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-413. TX Dual Tone Output Spectrum at 2.6 GHz, -30dBFS each ($\pm 600\text{ MHz}$)



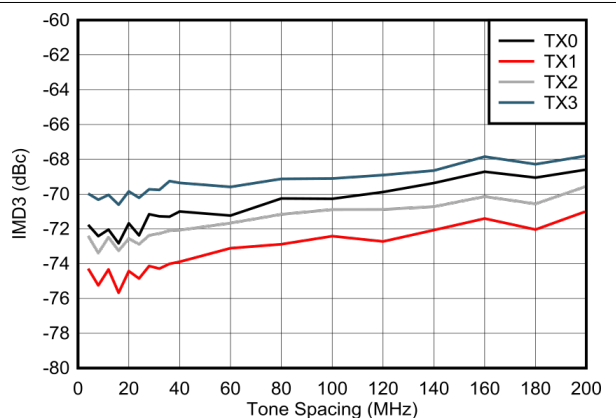
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = -1 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 7-414. TX Output Noise vs Supply Voltage at 2.6 GHz



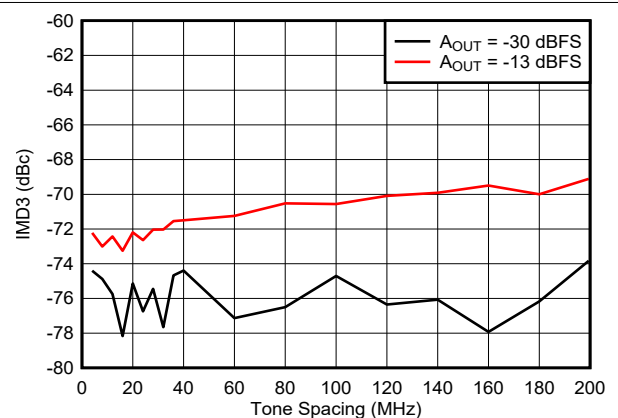
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = -13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 7-415. TX IMD3 vs Supply Voltage at 2.6 GHz



$f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, external clock mode

Figure 7-416. IMD3 vs Tone Spacing and Channel at 2.6 GHz



$f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, external clock mode

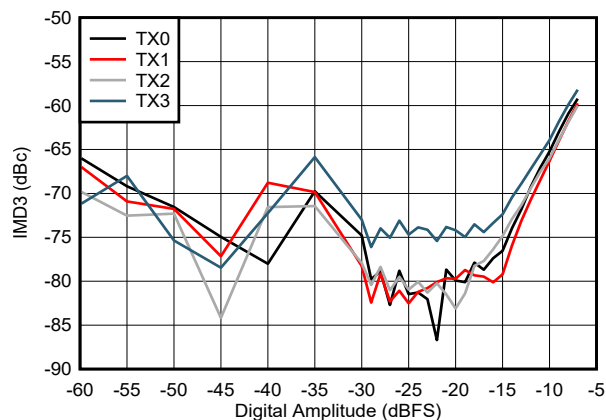
Figure 7-417. IMD3 vs Tone Spacing and Amplitude at 2.6 GHz

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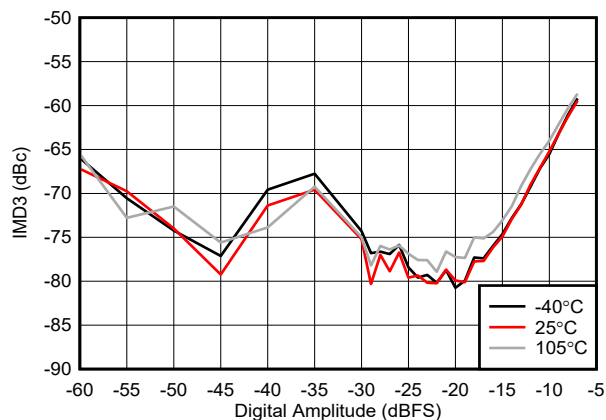
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7.12.10 TX Typical Characteristics at 2.6GHz (continued)

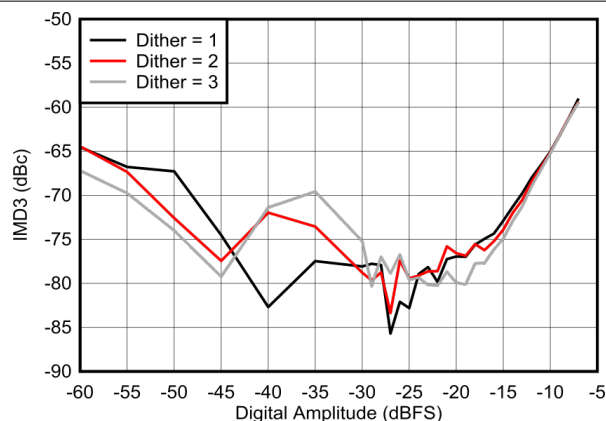
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



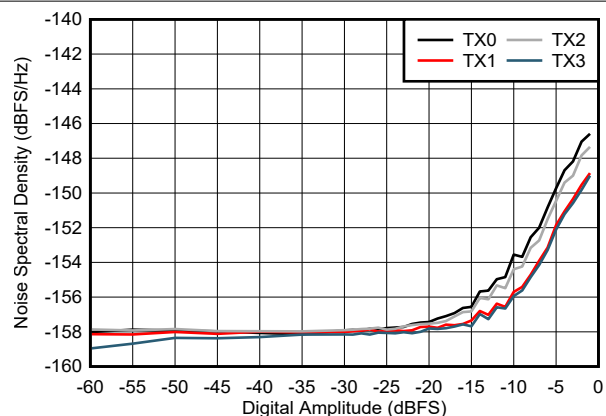
$f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, external clock mode

Figure 7-418. IMD3 vs Digital Amplitude and Channel at 2.6 GHz

$f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, external clock mode

Figure 7-419. IMD3 vs Digital Amplitude and Temperature at 2.6 GHz

$f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, external clock mode

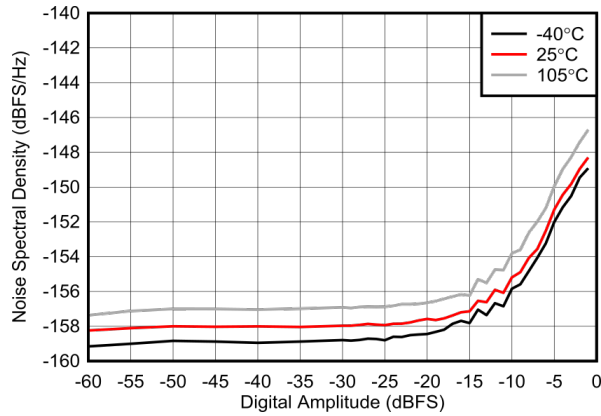
Figure 7-420. IMD3 vs Digital Amplitude and Dither at 2.6 GHz

$f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, external clock mode, 50MHz offset

Figure 7-421. NSD vs Digital Amplitude and Channel at 2.6 GHz

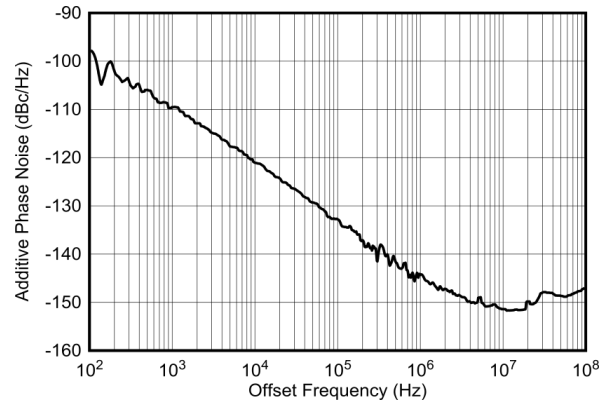
7.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, external clock mode, 50MHz offset

Figure 7-422. NSD vs Digital Amplitude and Temperature at 2.6 GHz



$f_{\text{DAC}} = f_{\text{CLK}} = 9000\text{MSPS}$, non-interleave mode

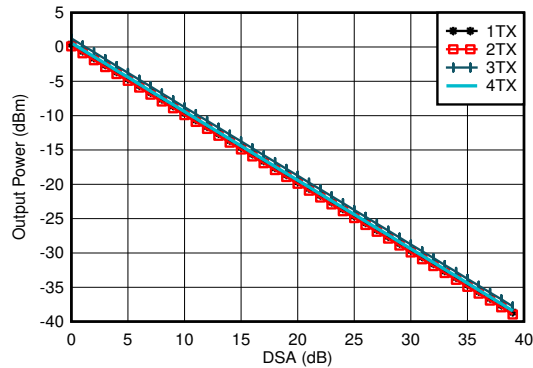
Figure 7-423. External Clock Additive Phase Noise at 2.6 GHz

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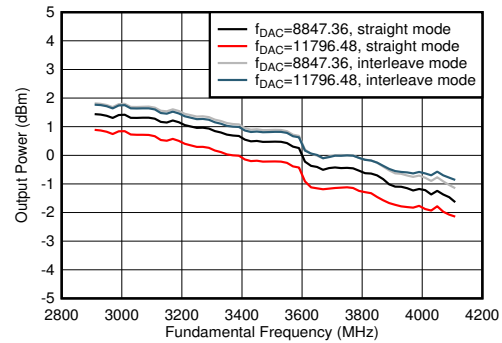
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7.12.11 TX Typical Characteristics at 3.5GHz

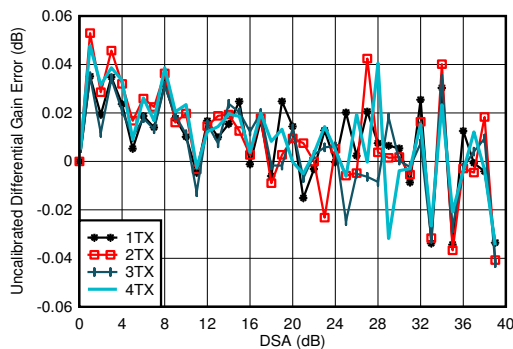
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



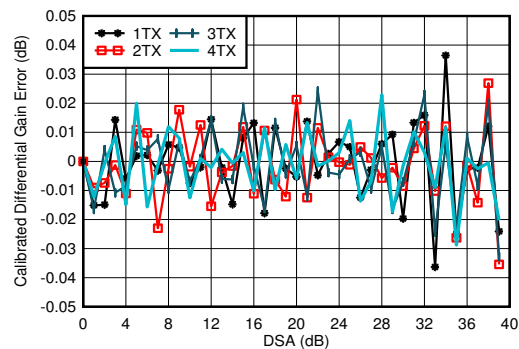
$A_{\text{out}} = -0.5\text{dBFS}$, 3.5 GHz Matching, included PCB and cable losses

Figure 7-424. TX Output Power vs DSA Setting at 3.5 GHz

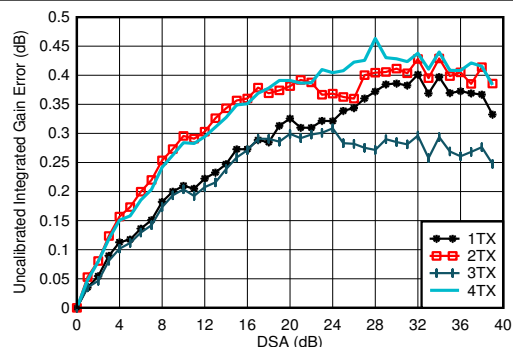
$A_{\text{out}} = -0.5\text{dBFS}$, 3.5 GHz Matching, included PCB and cable losses

Figure 7-425. TX Output Power vs Frequency

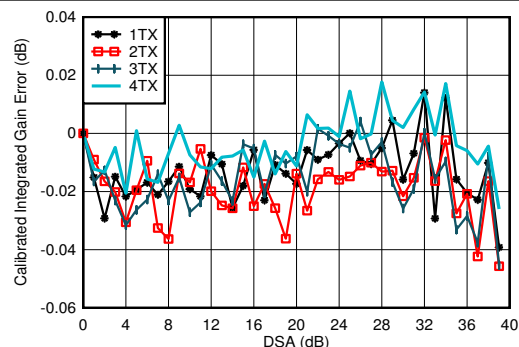
3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-426. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz

3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-427. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz

3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

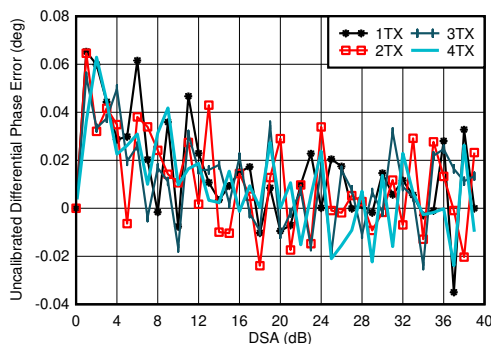
Figure 7-428. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-429. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

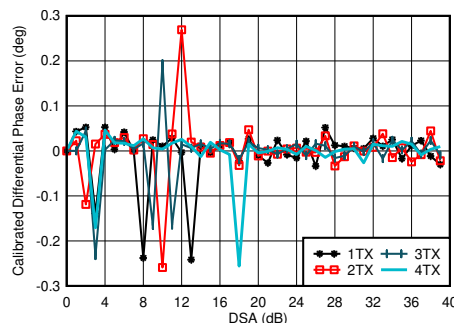
7.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



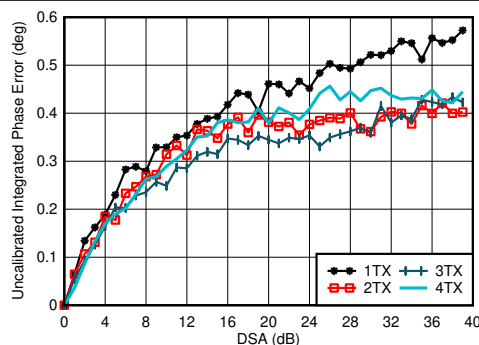
3.5 GHz Matching, included PCB and cable losses
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-430. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



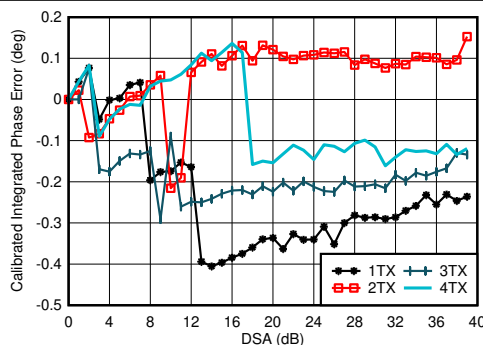
3.5 GHz Matching, included PCB and cable losses
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$. Phase DNL spike may occur at any DSA setting.

Figure 7-431. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



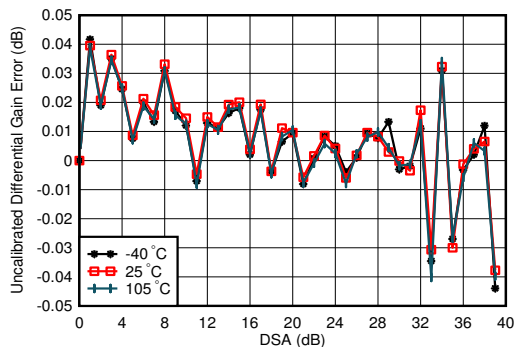
3.5 GHz Matching, included PCB and cable losses
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-432. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



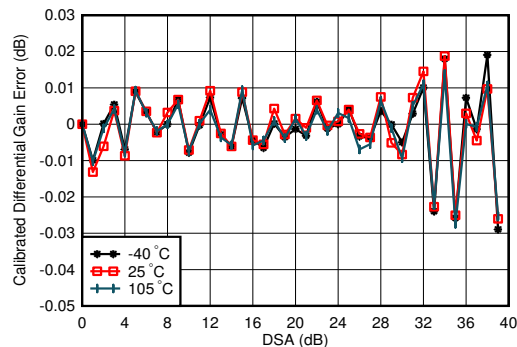
3.5 GHz Matching, included PCB and cable losses
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-433. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, 0TX
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-434. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX, Calibrated at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

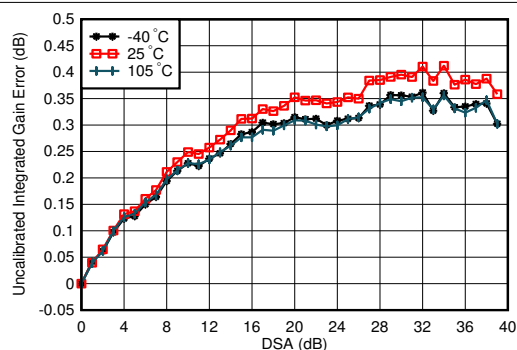
Figure 7-435. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

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7.12.11 TX Typical Characteristics at 3.5GHz (continued)

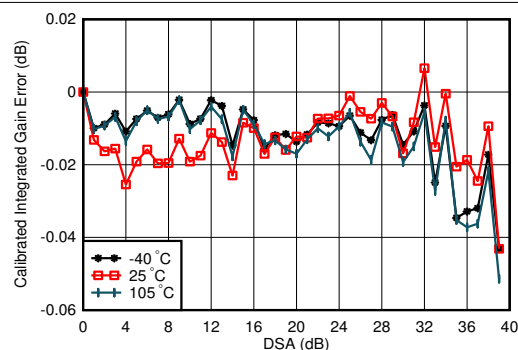
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



3.5 GHz Matching, 0TX

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

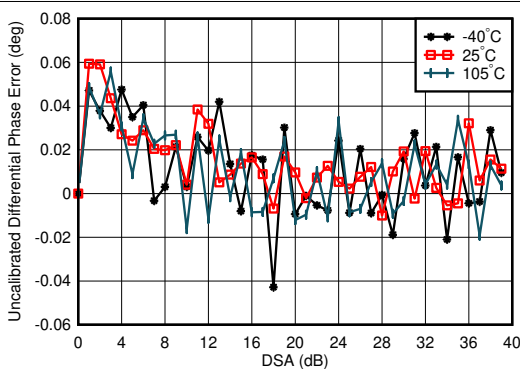
Figure 7-436. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX, Calibrated at 25°C

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

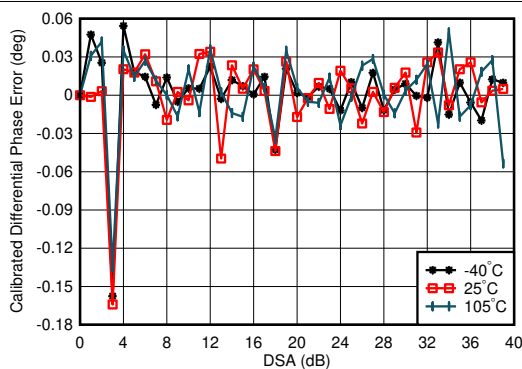
Figure 7-437. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-438. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



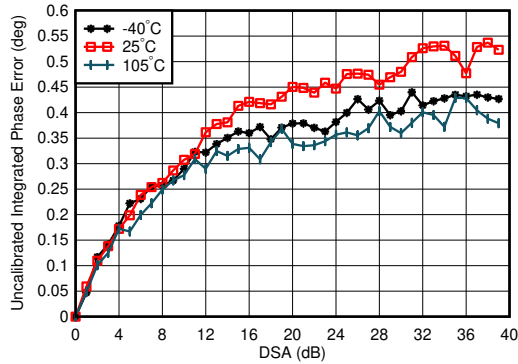
3.5 GHz Matching, 0TX, Calibrated at 25°C

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-439. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz

7.12.11 TX Typical Characteristics at 3.5GHz (continued)

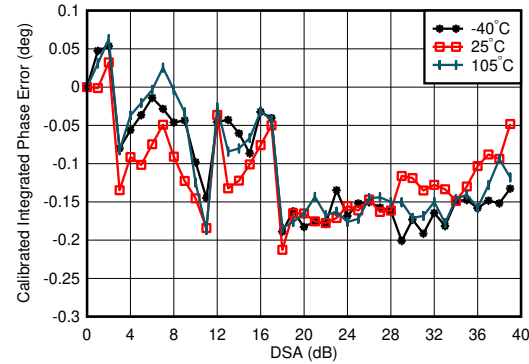
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



3.5 GHz Matching, 0TX

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

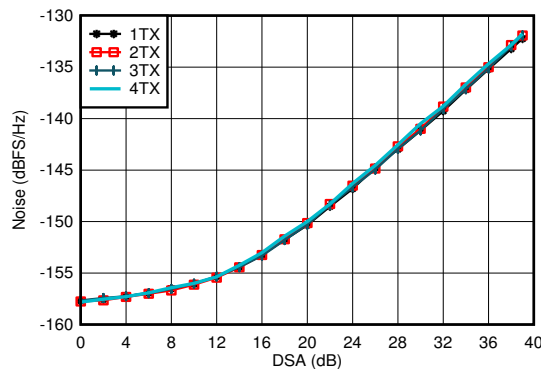
Figure 7-440. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 0TX, Calibrated at 25°C

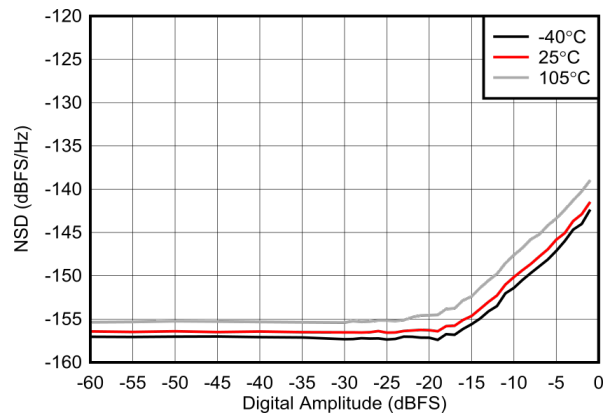
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-441. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



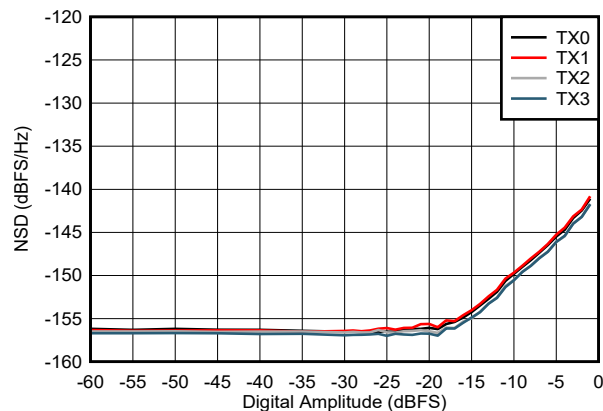
A. $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, matching at 3.5GHz, $A_{\text{out}} = -13\text{ dBFS}$.

Figure 7-442. TX NSD vs DSA Setting at 3.5 GHz



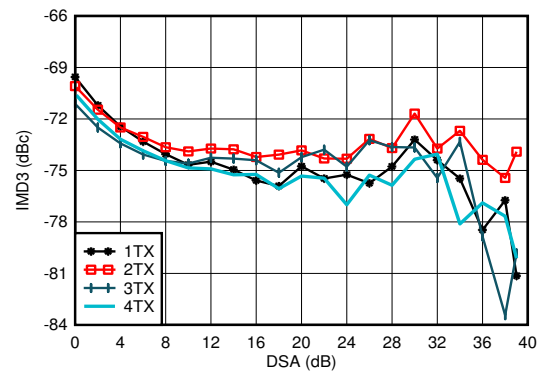
A. $f_{\text{DAC}} = 12\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-443. TX NSD vs Digital Amplitude and Temperature at 3.75 GHz



A. $f_{\text{DAC}} = 12\text{MSPS}$, external clock mode, non-interleave mode

Figure 7-444. TX NSD vs Digital Amplitude and Channel at 3.75 GHz



20-MHz tone spacing, 3.5 GHz Matching, -13 dBFS each tone, included PCB and cable losses

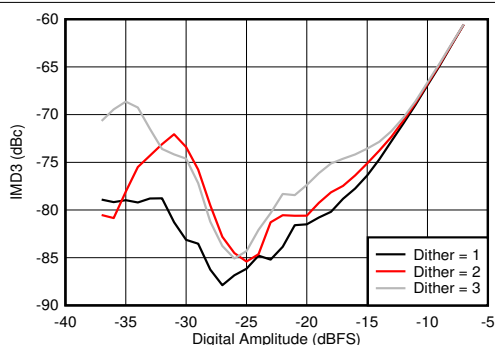
Figure 7-445. TX IMD3 vs DSA Setting at 3.5 GHz

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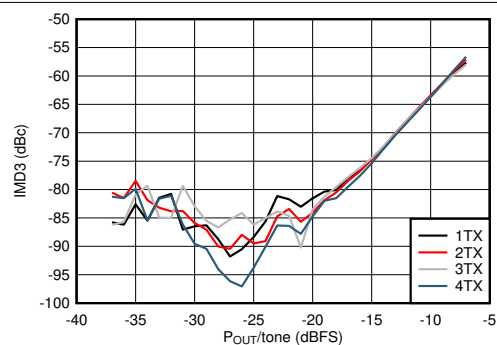
7.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



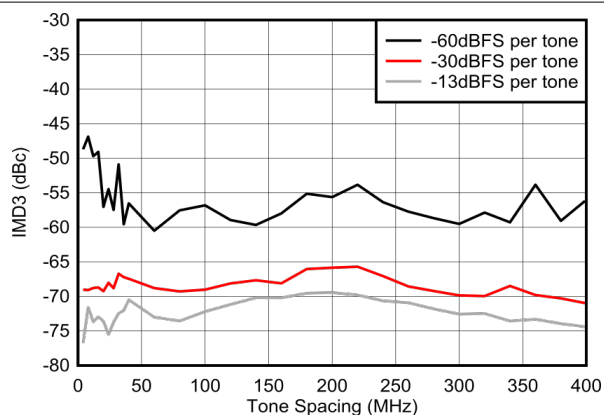
20-MHz tone spacing, 3.5 GHz Matching, included PCB and cable losses

Figure 7-446. TX IMD3 vs Digital Amplitude and Dither Setting at 3.5 GHz



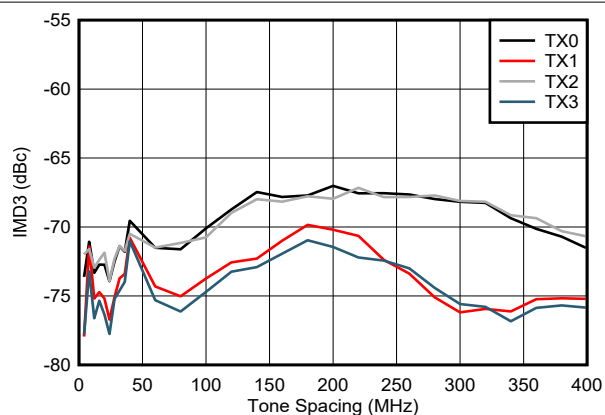
20-MHz tone spacing, 3.5 GHz Matching

Figure 7-447. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz



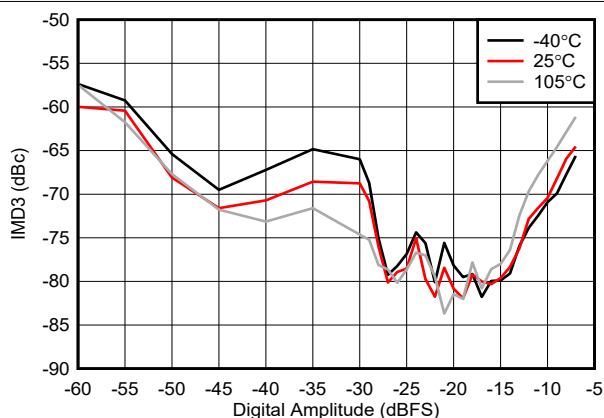
50-MHz tone spacing, external clock mode, non-interleave mode

Figure 7-448. TX IMD3 vs Tone Spacing and Amplitude at 3.75GHz



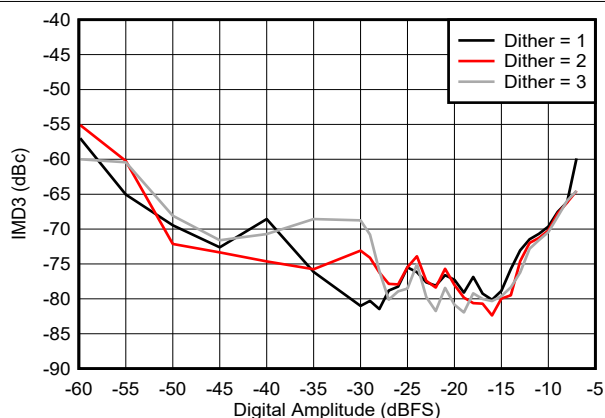
50-MHz tone spacing, external clock mode, non-interleave mode

Figure 7-449. TX IMD3 vs Tone Spacing and Channel at 3.75GHz



50-MHz tone spacing, external clock mode, non-interleave mode

Figure 7-450. TX IMD3 vs Digital Amplitude and Temperature at 3.75GHz

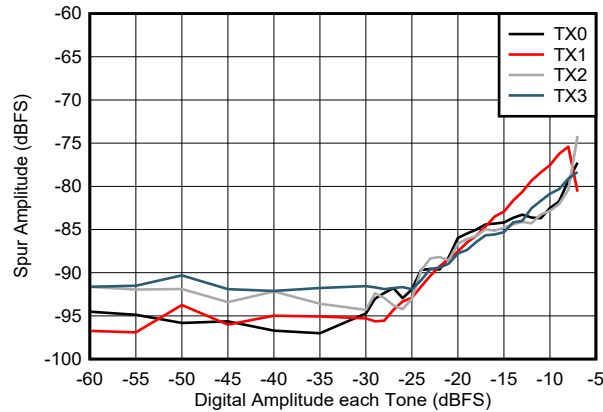


50-MHz tone spacing, external clock mode, non-interleave mode

Figure 7-451. TX IMD3 vs Digital Amplitude and Dither at 3.75GHz

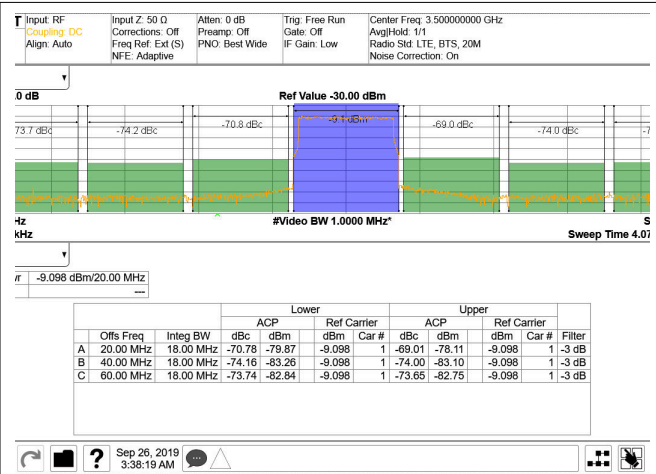
7.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



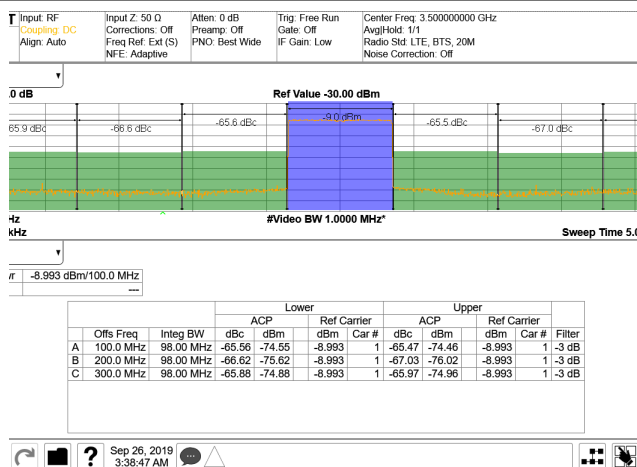
Inband = $3.75\text{GHz} \pm 600\text{MHz}$, $f_{\text{DAC}} = 9\text{GSPS}$, external clock mode, non-interleave mode.

Figure 7-452. Two Tone Inband SFDR vs Digital Amplitude at 3.75GHz



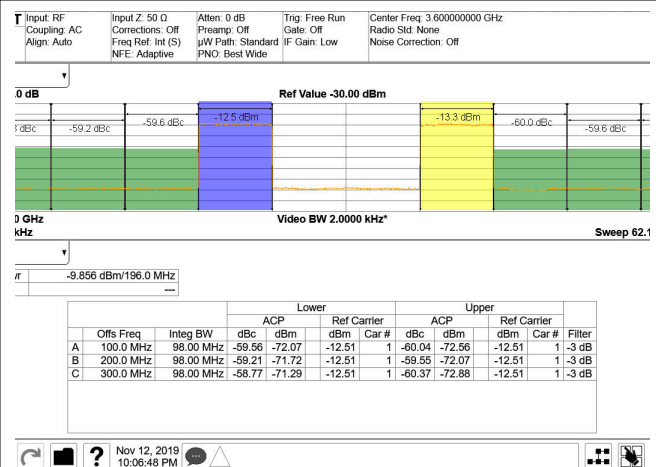
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-453. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 7-454. TX 100-MHz NR Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

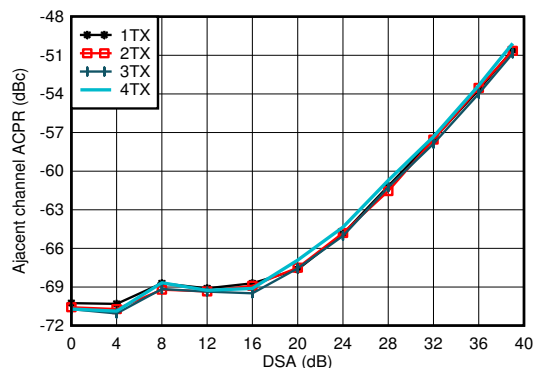
Figure 7-455. TX 2 carrier 100-MHz NR Output Spectrum at 3.45 GHz and 3.75 GHz

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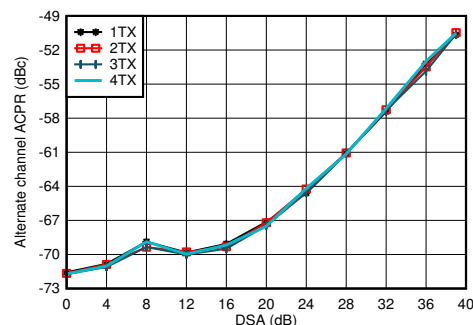
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7.12.11 TX Typical Characteristics at 3.5GHz (continued)

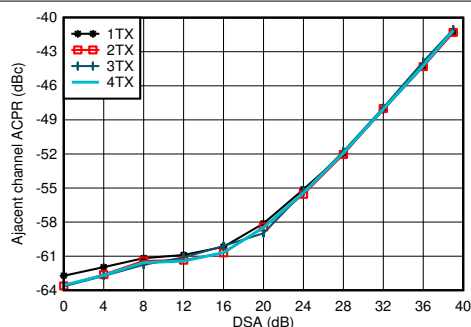
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



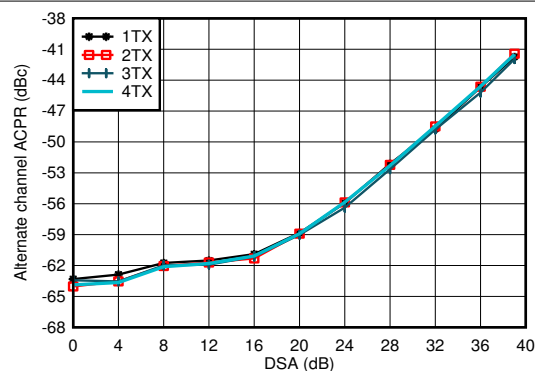
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-456. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz

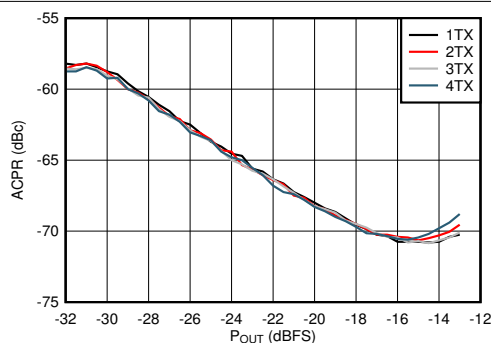
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-457. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz

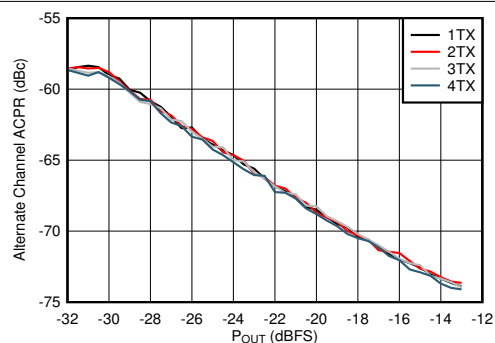
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 7-458. TX 100-MHz NR ACPR vs DSA Setting at 3.5 GHz

3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 7-459. TX 100-MHz NR alt-ACPR vs DSA Setting at 3.5 GHz

3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

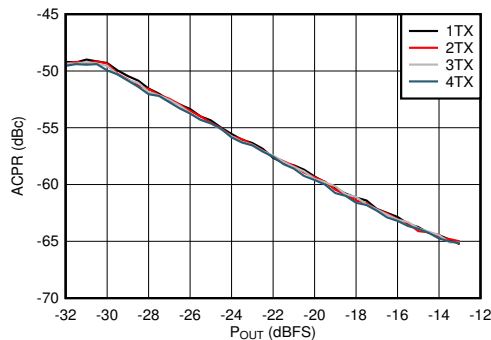
Figure 7-460. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz

3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-461. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz

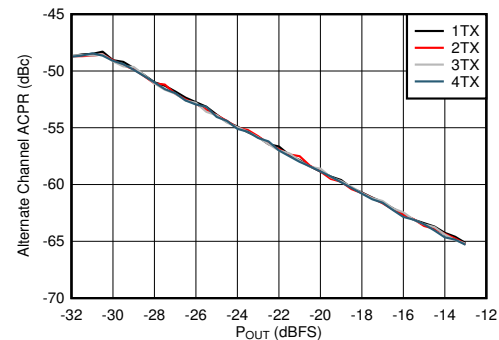
7.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



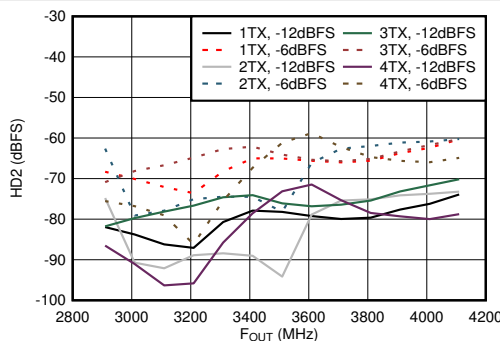
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 7-462. TX 100-MHz NR ACPR vs Digital Level at 3.5 GHz



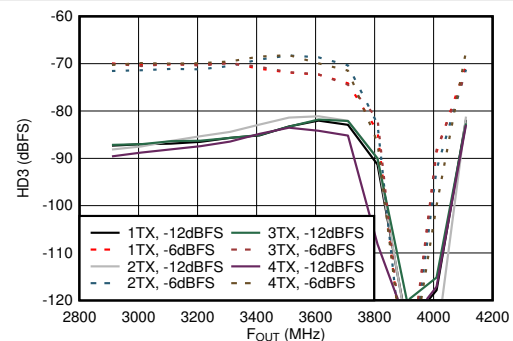
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

Figure 7-463. TX 100-MHz NR alt-ACPR vs Digital Level at 3.5 GHz



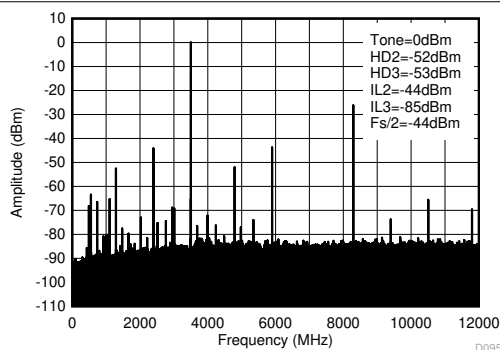
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency

Figure 7-464. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



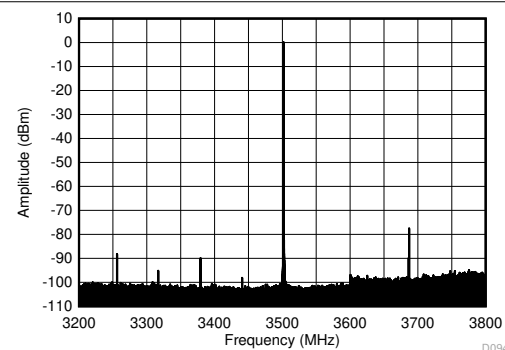
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

Figure 7-465. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode.

Figure 7-466. TX Single Tone (-1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})



Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode.

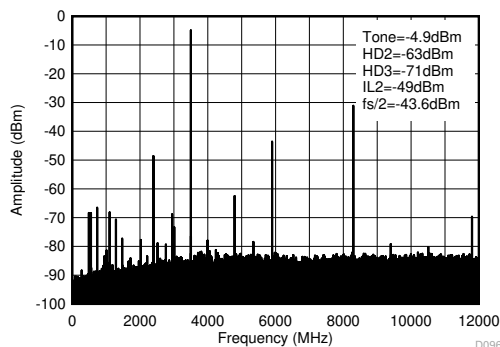
Figure 7-467. TX Single Tone (-1 dBFS) Output Spectrum at 3.5 GHz ($\pm 300\text{ MHz}$)

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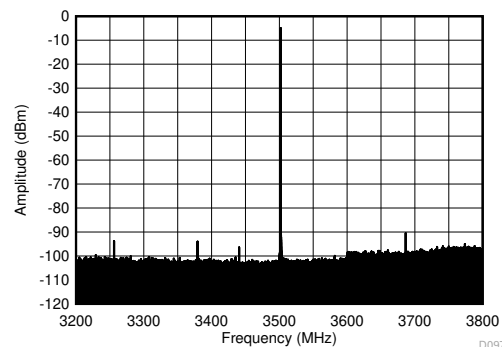
7.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



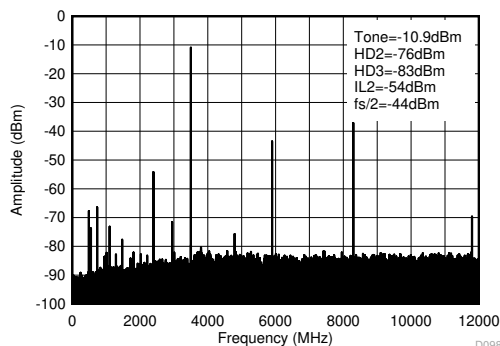
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode.

Figure 7-468. TX Single Tone (-6 dBFS) Output Spectrum at 3.5 GHz (0- f_{DAC})



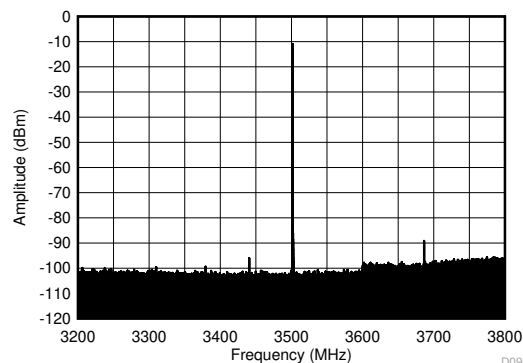
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode.

Figure 7-469. TX Single Tone (-6 dBFS) Output Spectrum at 3.5 GHz ($\pm 300\text{ MHz}$)



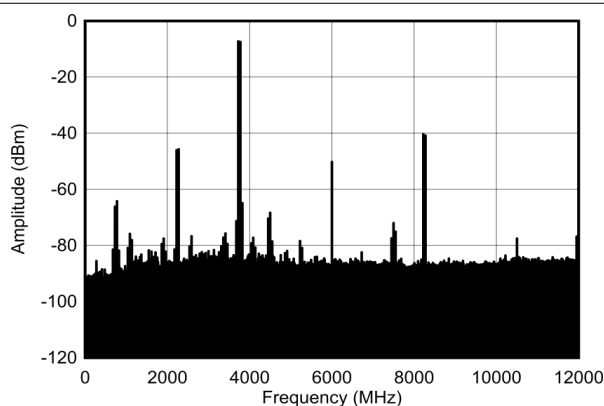
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode.

Figure 7-470. TX Single Tone (-12 dBFS) Output Spectrum at 3.5 GHz (0- f_{DAC})



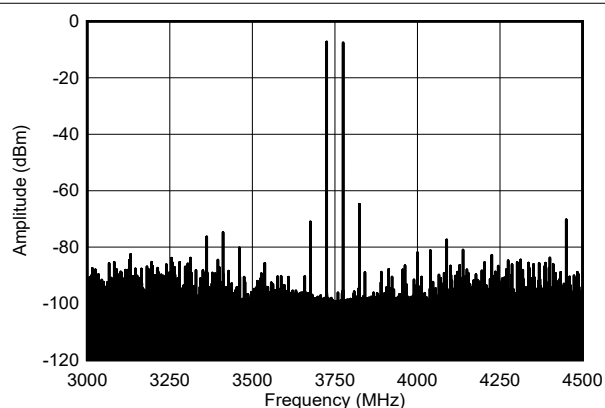
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode.

Figure 7-471. TX Single Tone (-12 dBFS) Output Spectrum at 3.5 GHz ($\pm 300\text{ MHz}$)



Matching at 3.5 GHz, 50MHz tone spacing, $f_{\text{DAC}} = 12\text{GSPS}$, non-interleave mode.

Figure 7-472. TX Dual Tone Output Spectrum at 3.75 GHz, -7dBFS each (0 - f_{DAC})

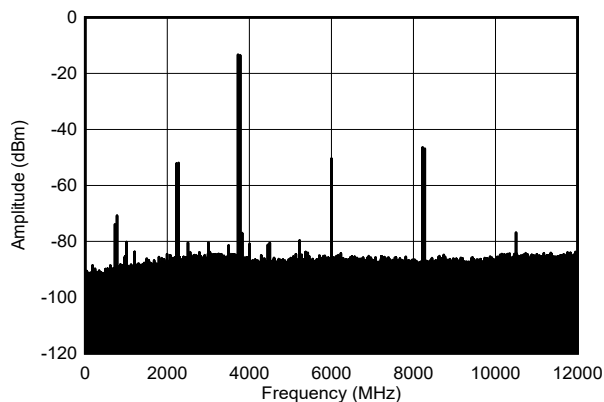


Matching at 3.5 GHz, 50MHz tone spacing, $f_{\text{DAC}} = 12\text{GSPS}$, non-interleave mode.

Figure 7-473. TX Dual Tone Output Spectrum at 3.75 GHz, -7dBFS each ($\pm 600\text{ MHz}$)

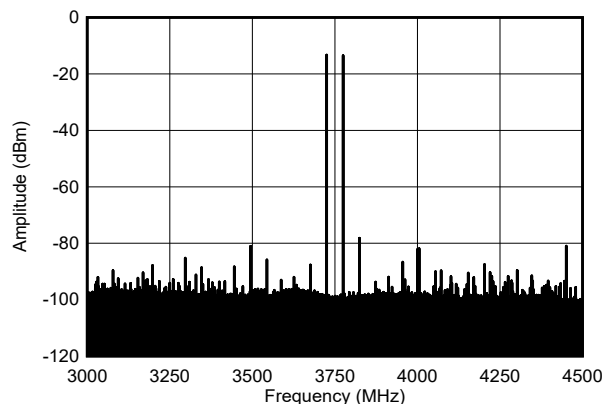
7.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



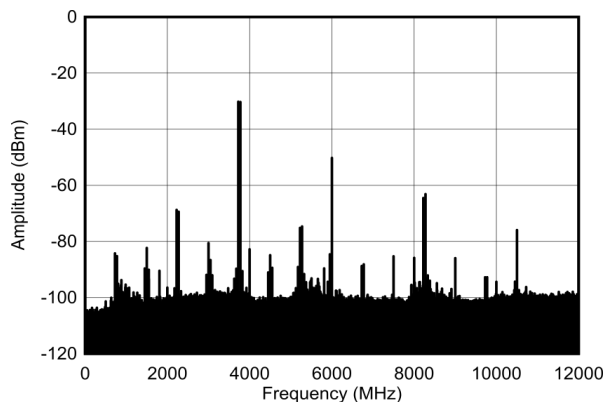
Matching at 3.5 GHz, 50MHz tone spacing, $f_{\text{DAC}} = 12\text{GSPS}$, non-interleave mode.

Figure 7-474. TX Dual Tone Output Spectrum at 3.75 GHz, -13dBFS each (0 - f_{DAC})



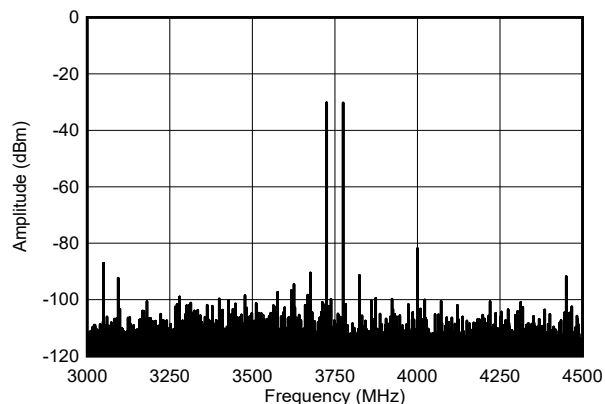
Matching at 3.5 GHz, 50MHz tone spacing, $f_{\text{DAC}} = 12\text{GSPS}$, non-interleave mode.

Figure 7-475. TX Dual Tone Output Spectrum at 3.75 GHz, -13dBFS each ($\pm 600\text{ MHz}$)



Matching at 3.5 GHz, 50MHz tone spacing, $f_{\text{DAC}} = 12\text{GSPS}$, non-interleave mode.

Figure 7-476. TX Dual Tone Output Spectrum at 3.75 GHz, -30dBFS each (0 - f_{DAC})



Matching at 3.5 GHz, 50MHz tone spacing, $f_{\text{DAC}} = 12\text{GSPS}$, non-interleave mode.

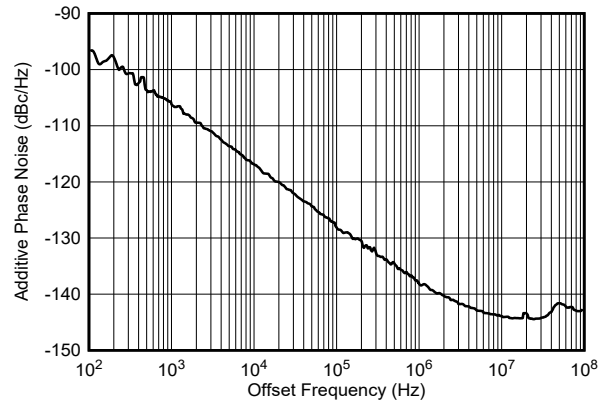
Figure 7-477. TX Dual Tone Output Spectrum at 3.75 GHz, -30dBFS each ($\pm 600\text{ MHz}$)

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7.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

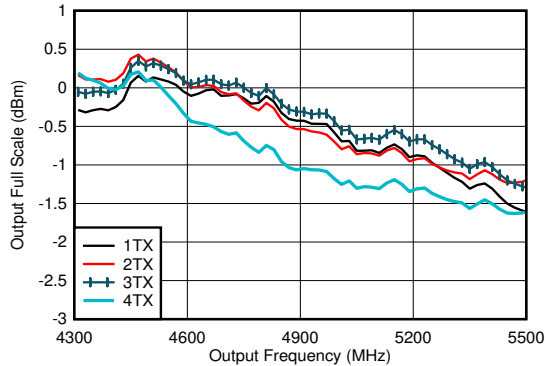


$f_{\text{DAC}} = f_{\text{CLK}} = 12\text{GSPS}$, non-interleave mode.

Figure 7-478. External Clock Additive Phase Noise at 3.7GHz

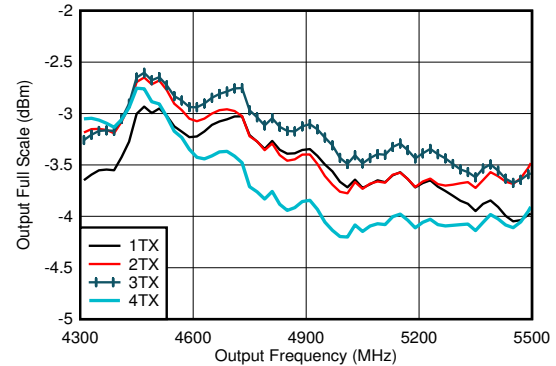
7.12.12 TX Typical Characteristics at 4.9GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



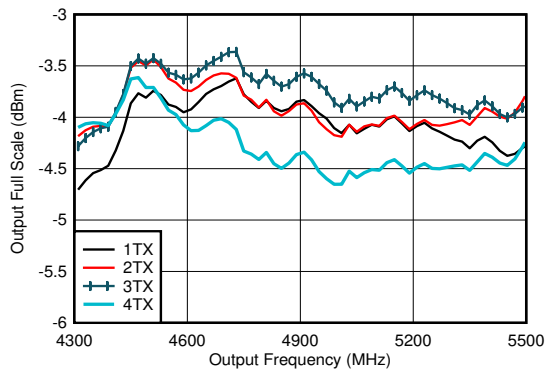
Excluding PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 4.9 GHz matching

Figure 7-479. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS



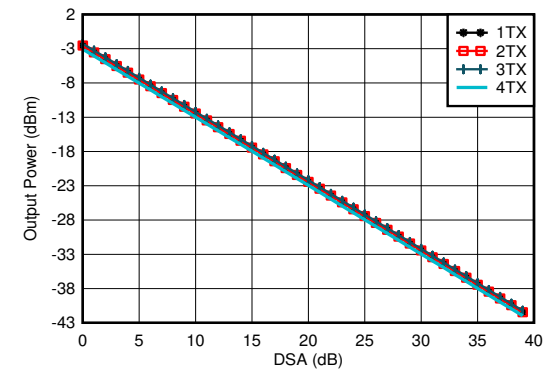
Excluding PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 4.9 GHz matching

Figure 7-480. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode, 2nd Nyquist Zone



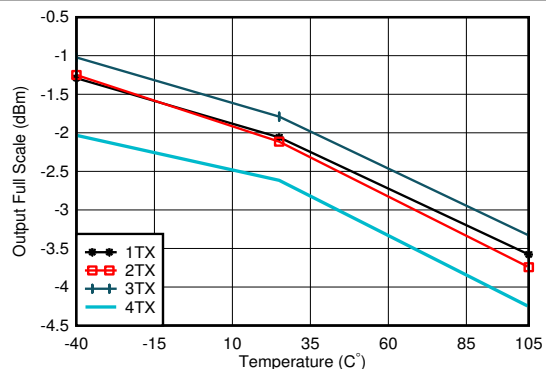
Excluding PCB and cable losses, $A_{\text{out}} = -0.5\text{dBFS}$, DSA = 0, 4.9 GHz matching

Figure 7-481. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode, 2nd Nyquist Zone



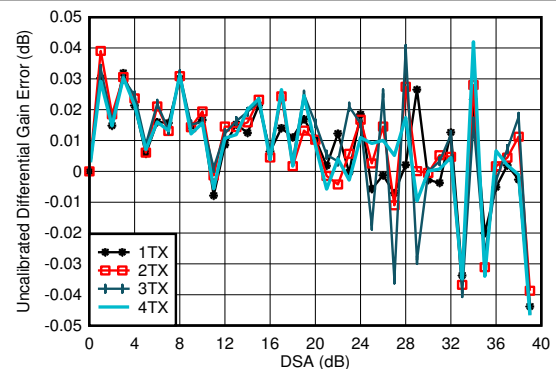
$f_{\text{DAC}} = 11796.48\text{MSPS}$, $A_{\text{out}} = -0.5\text{dBFS}$, matching 4.9 GHz

Figure 7-482. TX Output Power vs DSA Setting and Channel at 4.9 GHz



$A_{\text{out}} = -0.5\text{dBFS}$, 4.9 GHz Matching, PCB and cable losses included.

Figure 7-483. TX Full Scale Output Power vs Temperature and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

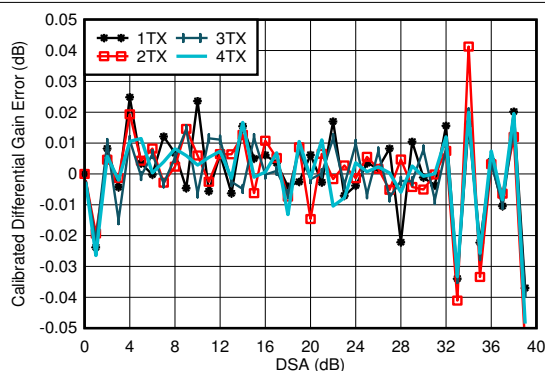
Figure 7-484. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

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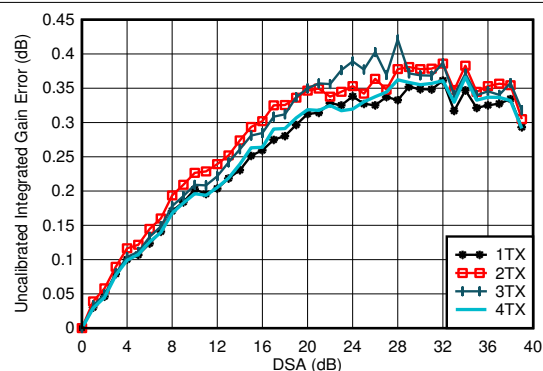
7.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



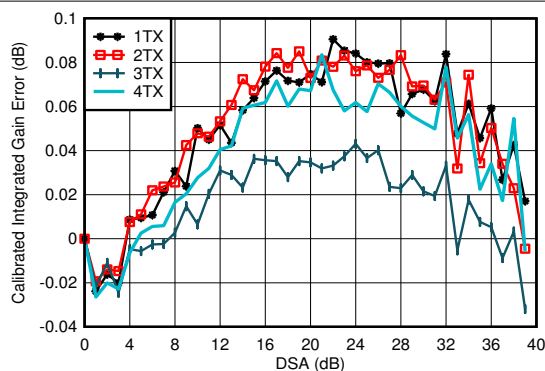
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, matching at 4.9 GHz
 Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-485. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



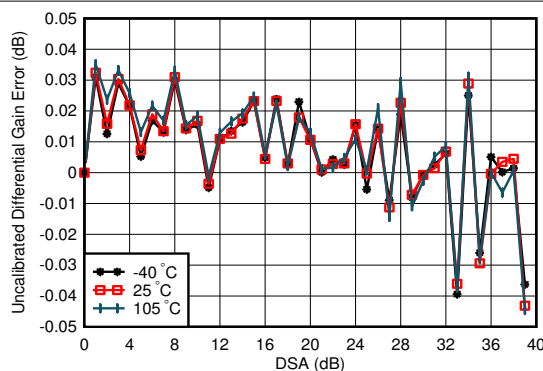
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, matching at 4.9 GHz
 Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-486. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, matching at 4.9 GHz
 Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-487. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz

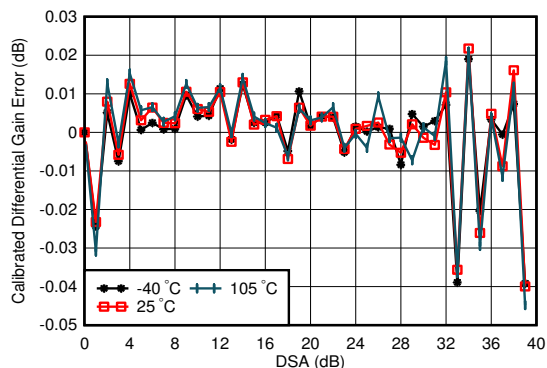


$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz
 Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-488. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

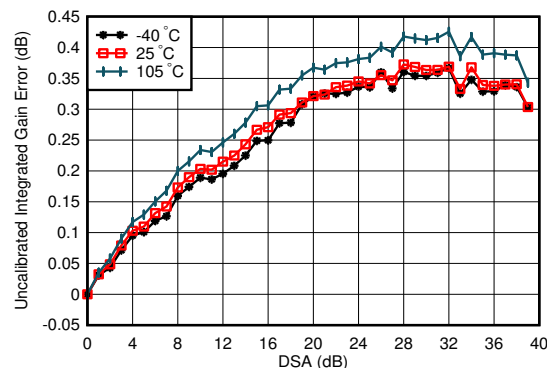
7.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



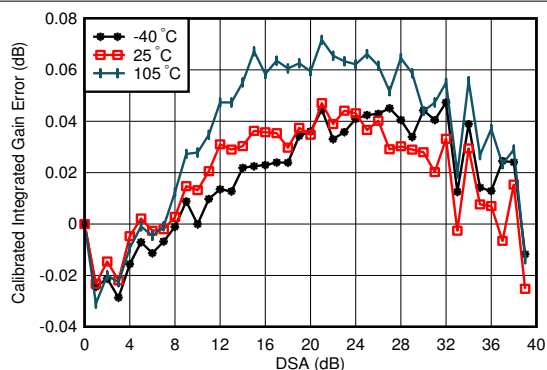
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-489. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



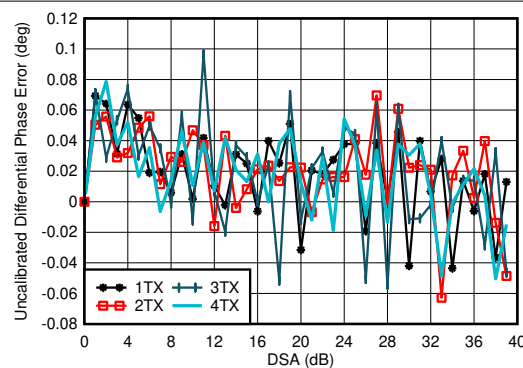
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-490. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-491. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

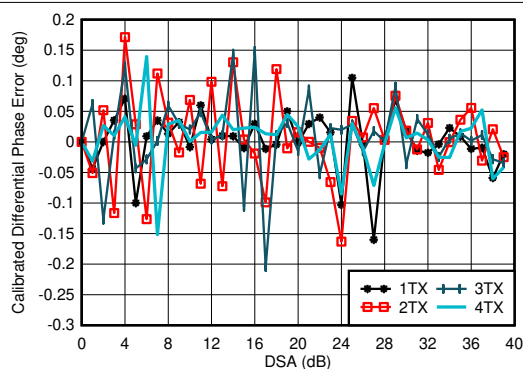
Figure 7-492. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

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7.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled

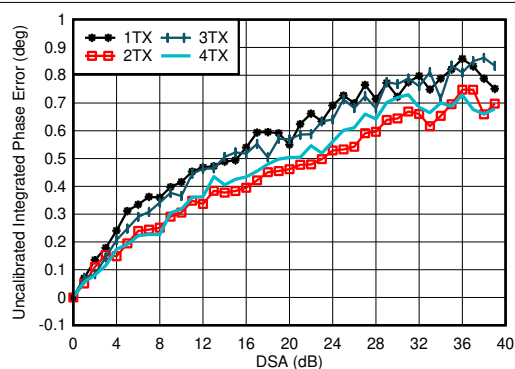


$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Phase DNL spike may occur at any DSA setting.

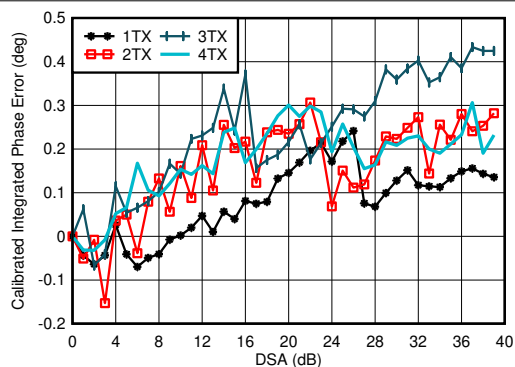
Figure 7-493. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

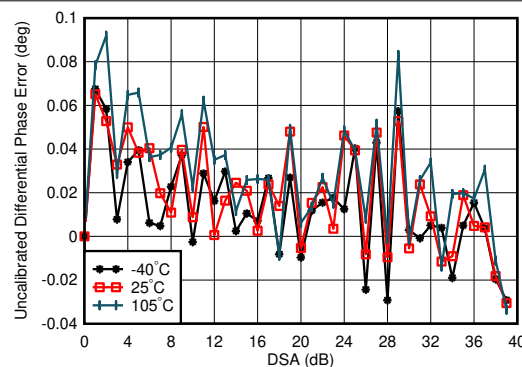
Figure 7-494. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-495. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



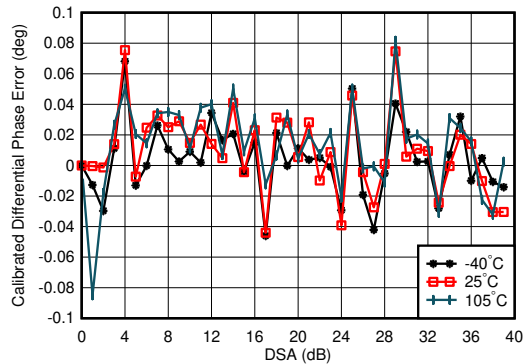
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-496. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz

7.12.12 TX Typical Characteristics at 4.9GHz (continued)

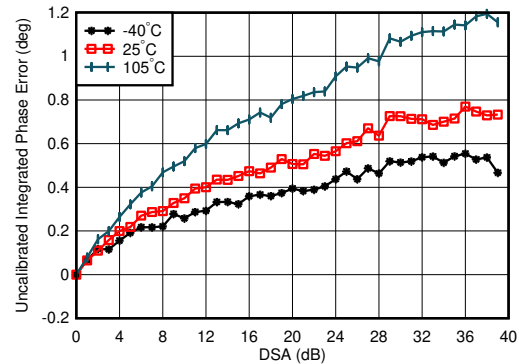
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

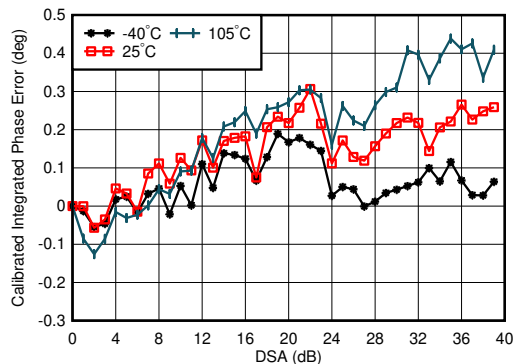
Figure 7-497. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

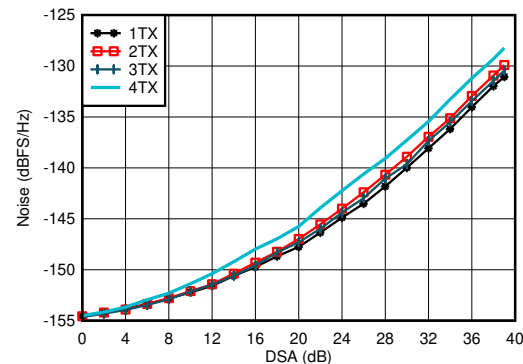
Figure 7-498. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-499. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9 GHz, $P_{\text{OUT}} = -13\text{ dBFS}$

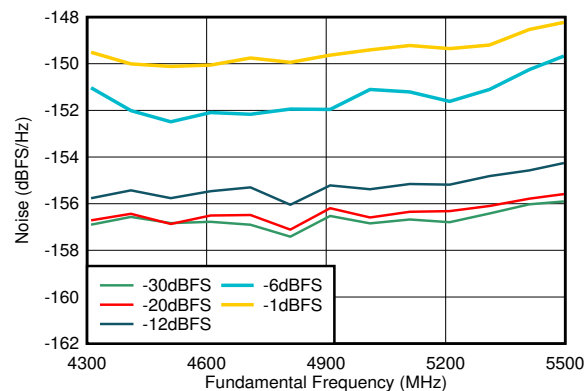
Figure 7-500. TX Output Noise vs Channel and Attenuation at 4.9 GHz

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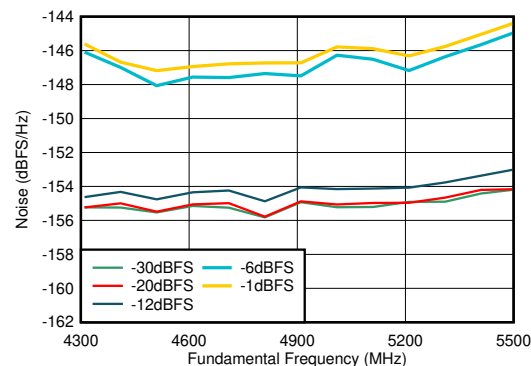
7.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



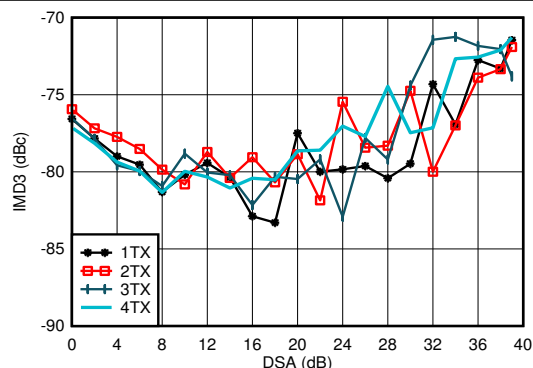
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, matching at 4.9GHz,
 $A_{\text{out}} = -13\text{ dBFS}$.

Figure 7-501. TX NSD vs Output Frequency and Digital Amplitude at 4.9 GHz (DSA=0dB)



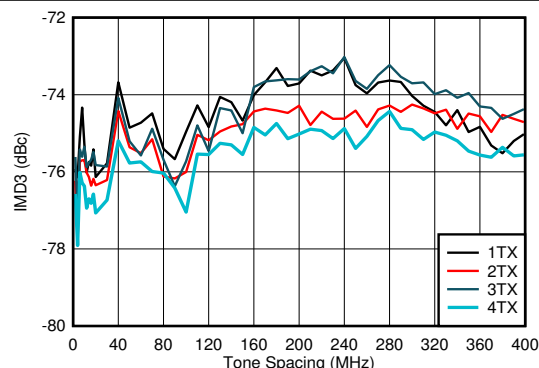
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, matching at 4.9GHz,
 $A_{\text{out}} = -13\text{ dBFS}$.

Figure 7-502. TX NSD vs Output Frequency and Digital Amplitude at 4.9GHz (DSA=6dB)



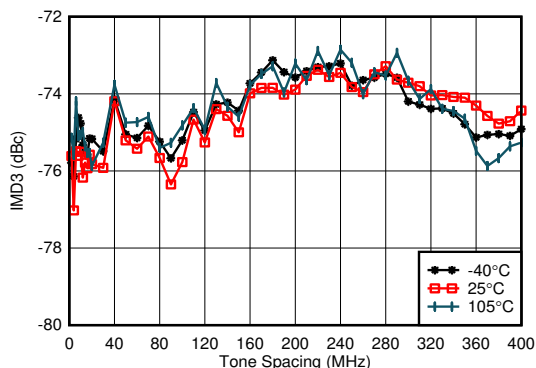
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9
GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, -13 dBFS each tone

Figure 7-503. TX IMD3 vs DSA Setting at 4.9 GHz



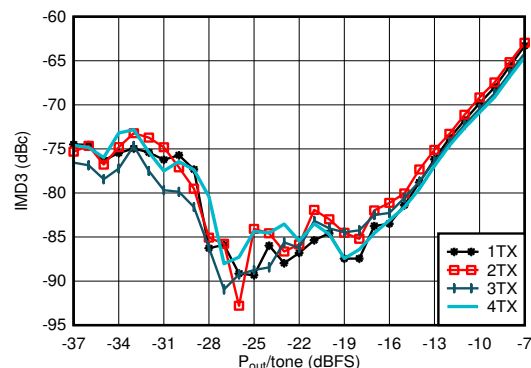
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9
GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, -13 dBFS each tone

Figure 7-504. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9
GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, -13 dBFS each tone, worst channel

Figure 7-505. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz

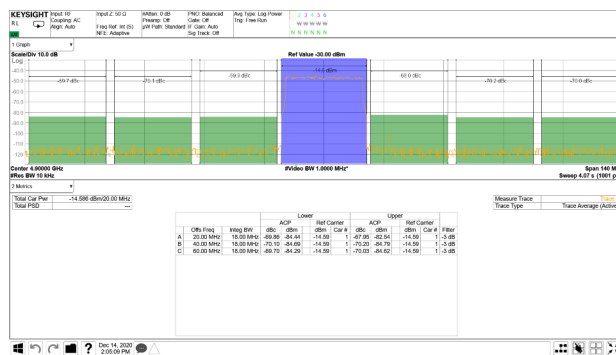


$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleaved mode, matching at 4.9
GHz, $f_{\text{CENTER}} = 4.9\text{GHz}$, $f_{\text{SPACING}} = 20\text{ MHz}$

Figure 7-506. TX IMD3 vs Digital Level at 4.9 GHz

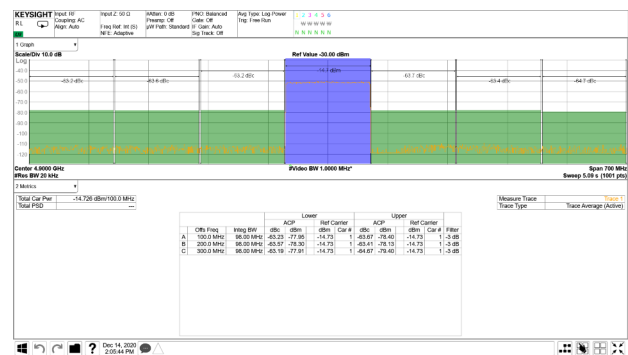
7.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



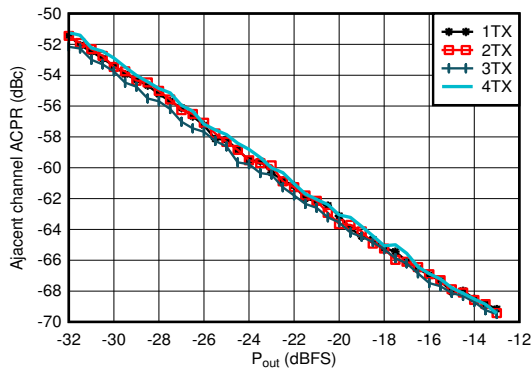
TM1.1, $P_{\text{OUT_RMS}} = -13\text{ dBFS}$

Figure 7-507. TX 20-MHz LTE Output Spectrum at 4.9 GHz



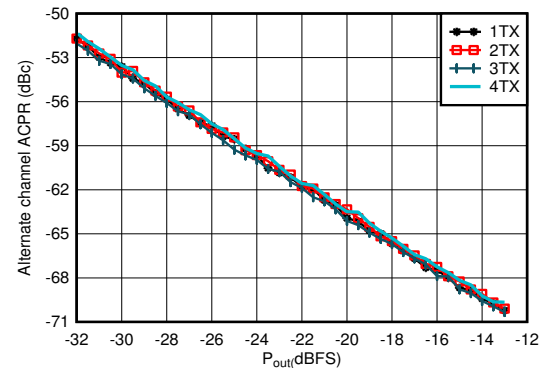
TM1.1, $P_{\text{OUT_RMS}} = -13\text{ dBFS}$

Figure 7-508. TX 100-MHz NR Output Spectrum at 4.9 GHz



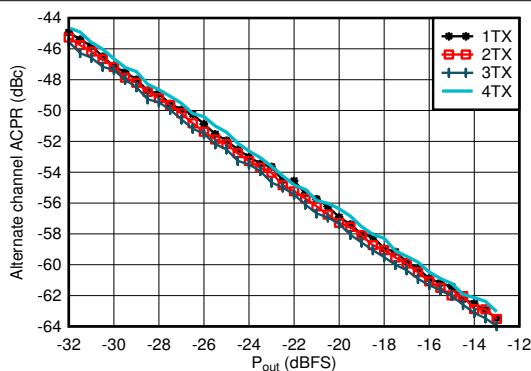
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-509. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



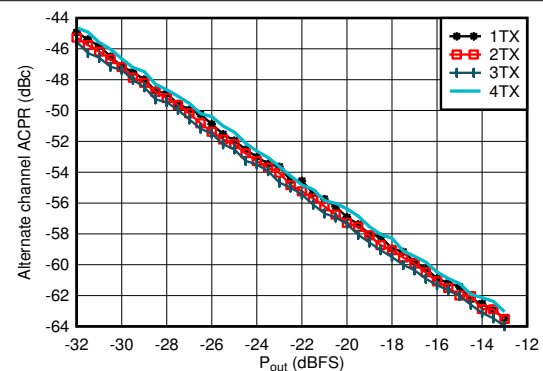
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-510. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-511. TX 100-MHz NR ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

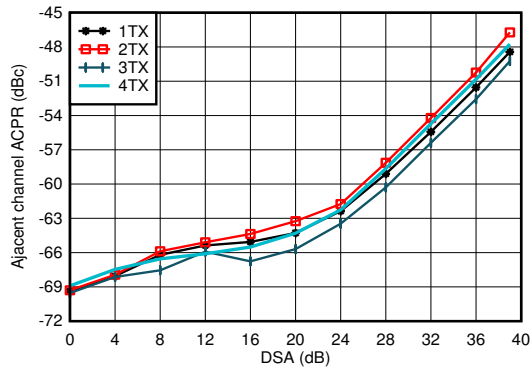
Figure 7-512. TX 100-MHz NR alt-ACPR vs Digital Level at 4.9 GHz

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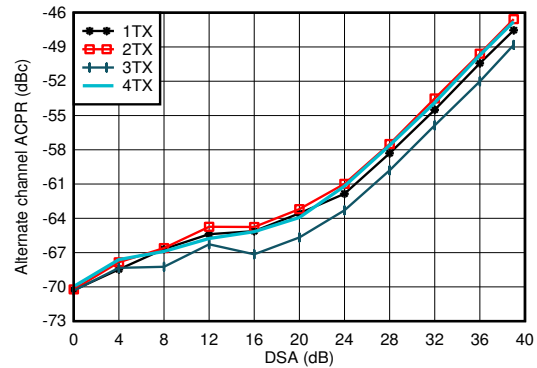
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7.12.12 TX Typical Characteristics at 4.9GHz (continued)

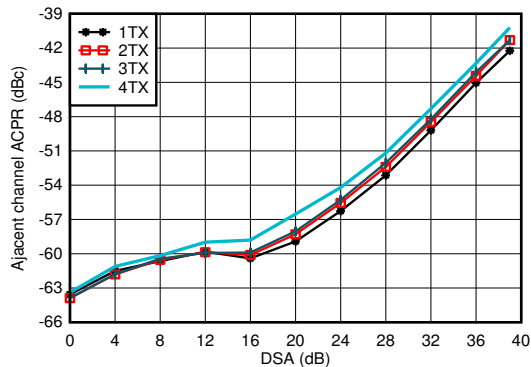
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



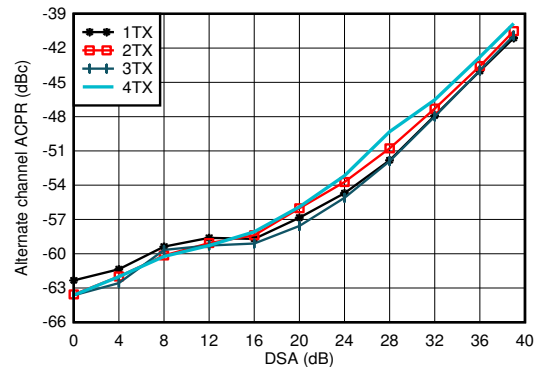
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-513. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz

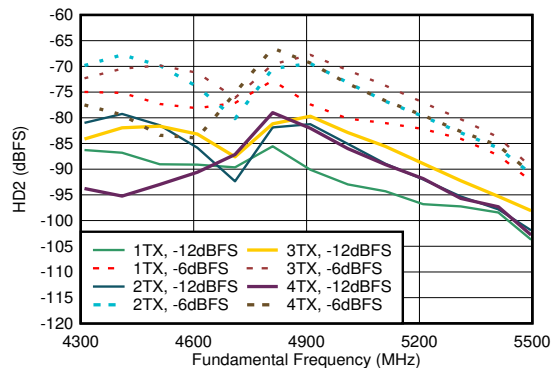
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-514. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz

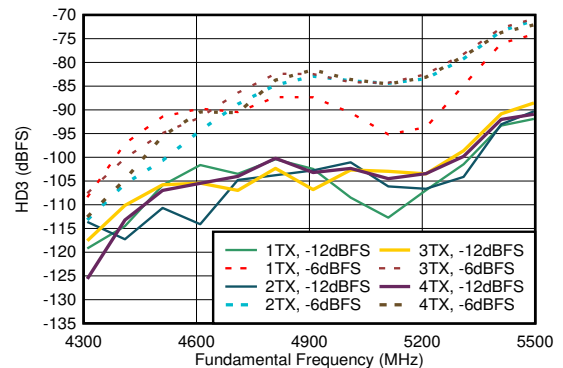
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-515. TX 100-MHz NR ACPR vs DSA at 4.9 GHz

Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-516. TX 100-MHz NR alt-ACPR vs DSA at 4.9 GHz

Matching at 4.9 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency

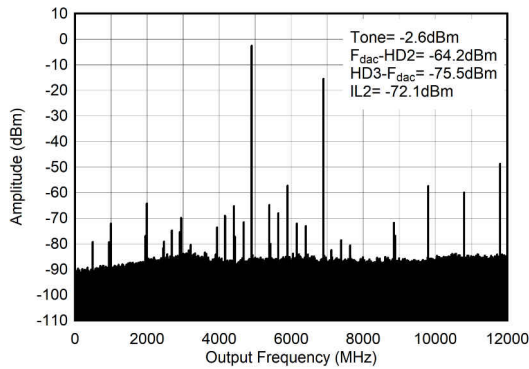
Figure 7-517. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz

Matching at 4.9 GHz, $f_{\text{DAC}} = 11.79648\text{GSPS}$, interleave mode, normalized to output power at harmonic frequency

Figure 7-518. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz

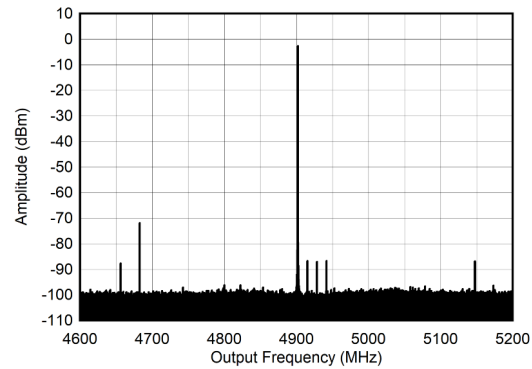
7.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



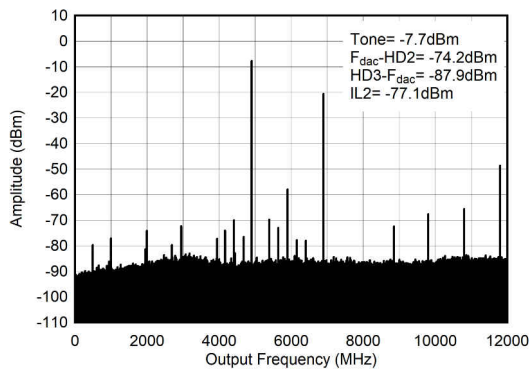
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$.

Figure 7-519. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)



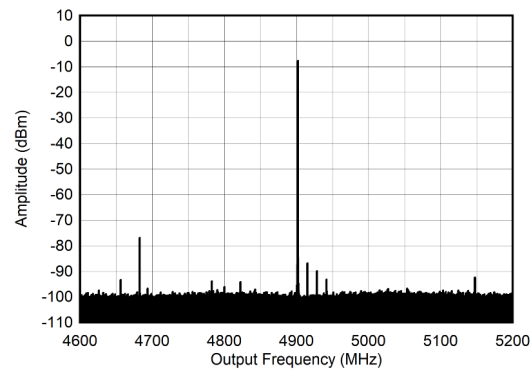
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 7-520. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz ($\pm 300\text{ MHz}$)



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$.

Figure 7-521. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 4.9 GHz matching, includes PCB and cable losses

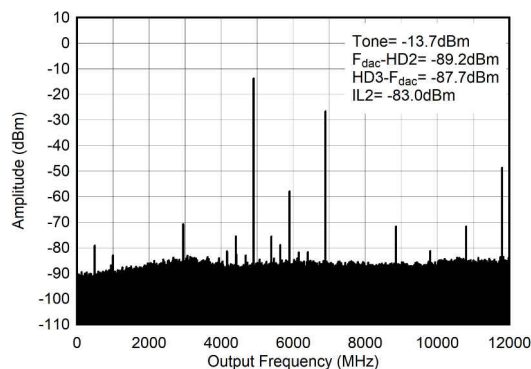
Figure 7-522. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz ($\pm 300\text{ MHz}$)

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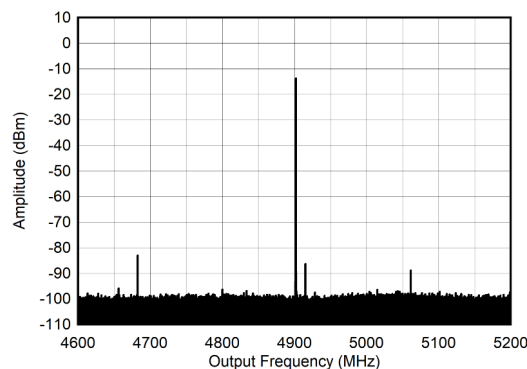
7.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, $f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, Internal PLL, $f_{\text{REF}} = 491.52\text{MSPS}$, 24x Interpolation, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled



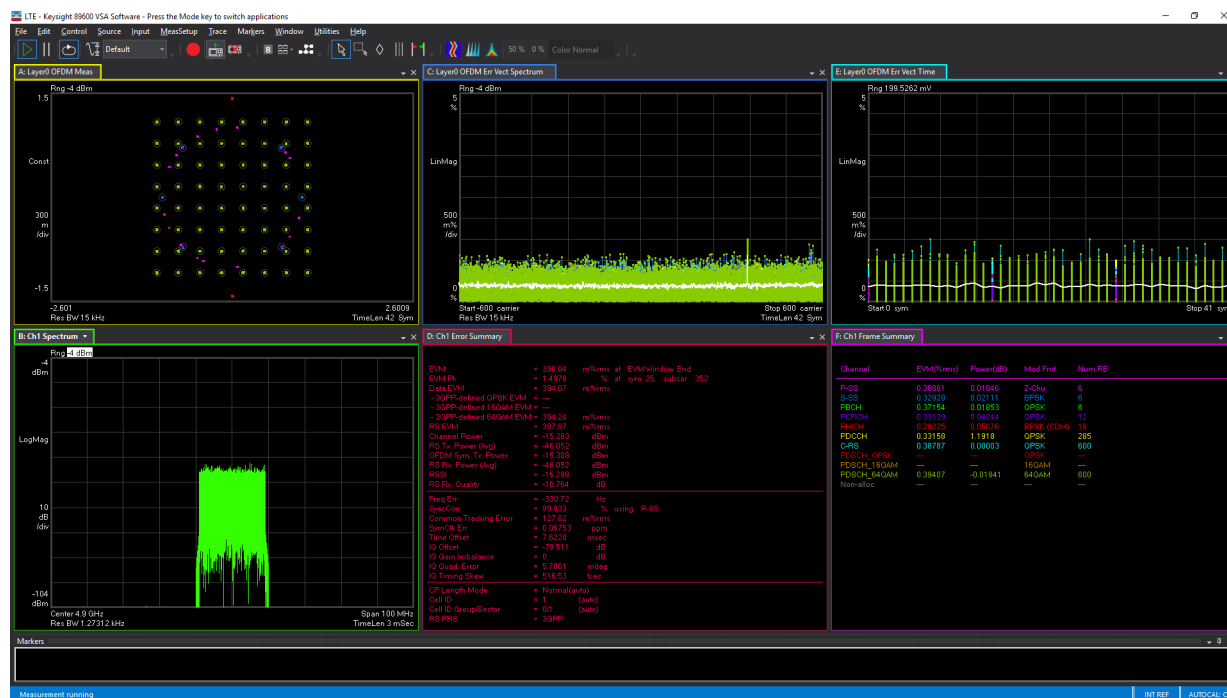
$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-523. TX Single Tone (-12 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode, 4.9 GHz matching, includes PCB and cable losses

Figure 7-524. TX Single Tone (-12 dBFS) Output Spectrum at 4.9 GHz ($\pm 300\text{ MHz}$)

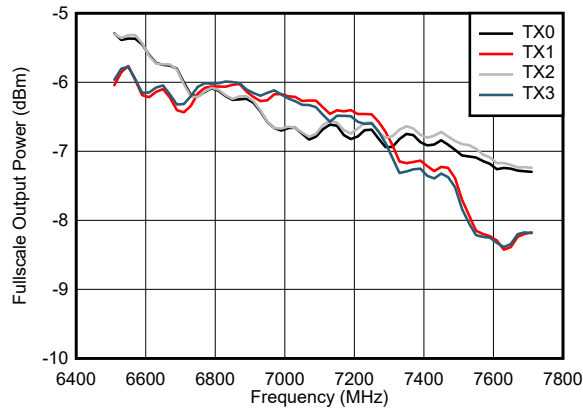


TM1.1, $P_{\text{OUT_RMS}} = -13\text{ dBFS}$

Figure 7-525. TX 20-MHz LTE Error Vector Magnitude at 4.9 GHz

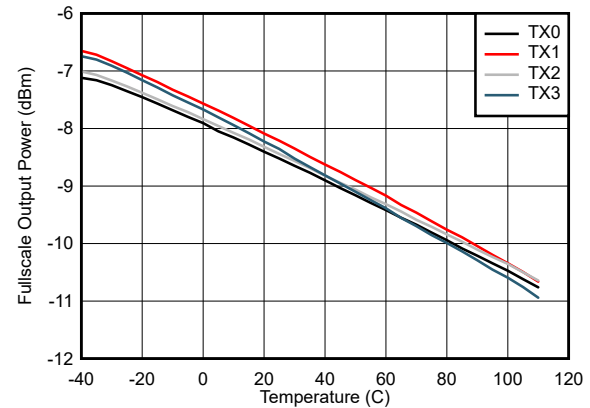
7.12.13 TX Typical Characteristics at 7.1GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



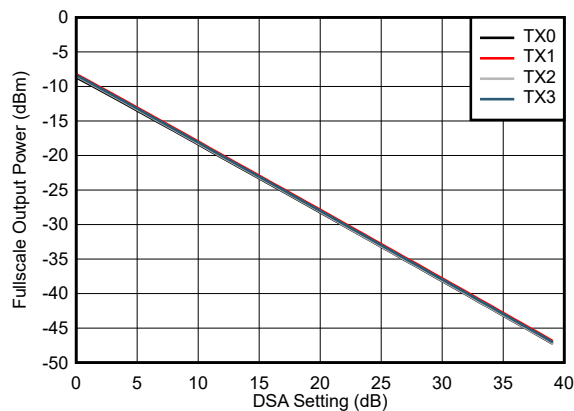
Excluding PCB and cable losses

Figure 7-526. TX Full Scale vs RF Frequency and Channel



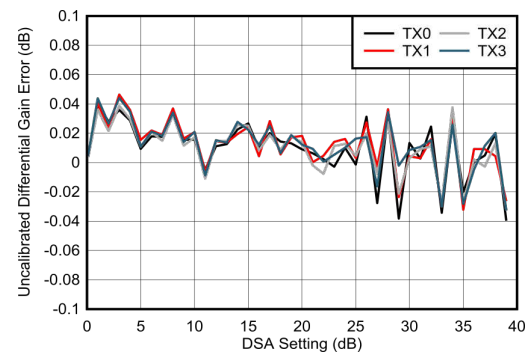
Excluding PCB and cable losses

Figure 7-527. TX Full Scale vs Temperature and Channel at 7.1GHz



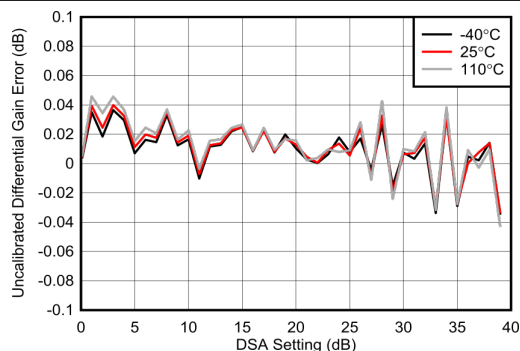
Excluding PCB and cable losses

Figure 7-528. TX Full Scale vs DSA Setting and Channel at 7.1 GHz



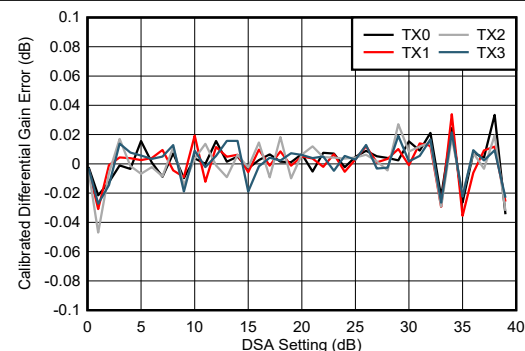
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 7-529. Uncalibrated Differential Gain Error vs Channel at 7.1 GHz



Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

Figure 7-530. Uncalibrated Differential Gain Error vs Temperature at 7.1 GHz



Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

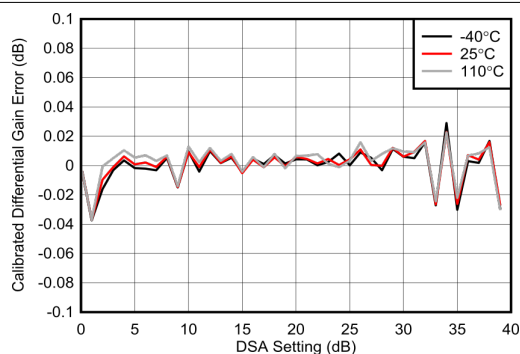
Figure 7-531. Calibrated Differential Gain Error vs Channel at 7.1 GHz

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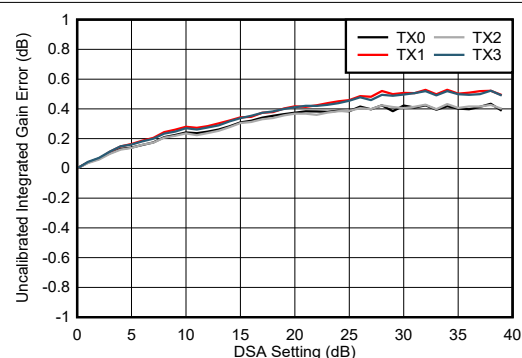
7.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



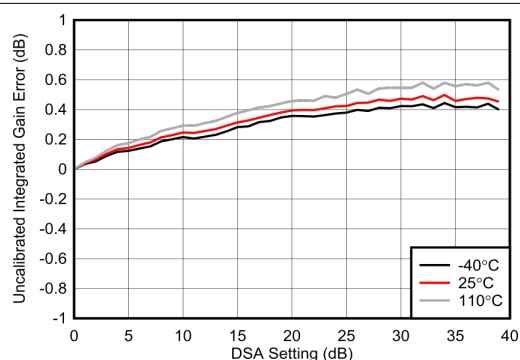
Differential Gain Error = $\text{Gain}(\text{DSA Setting} - 1) - \text{Gain}(\text{DSA Setting})$

Figure 7-532. Calibrated Differential Gain Error vs Temperature at 7.1 GHz



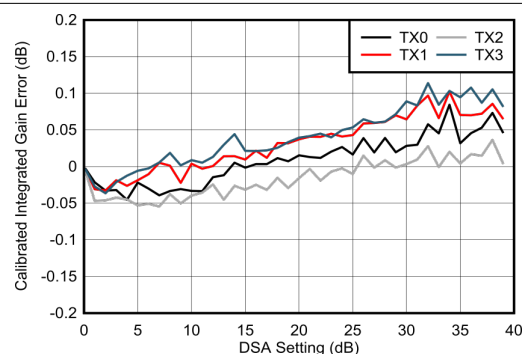
Integrated Gain Error = $\text{Gain}(\text{DSA Setting}) - \text{Gain}(\text{DSA Setting} = 0)$.

Figure 7-533. Uncalibrated Integrated Gain Error vs Channel at 7.1 GHz



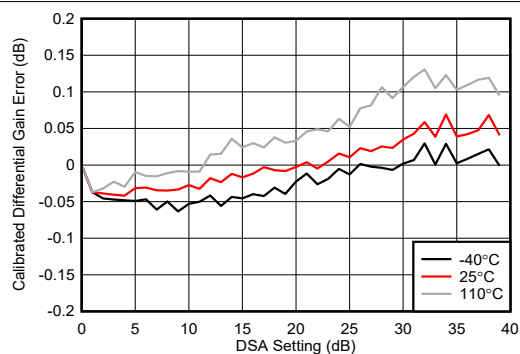
Integrated Gain Error = $\text{Gain}(\text{DSA Setting}) - \text{Gain}(\text{DSA Setting} = 0)$.

Figure 7-534. Uncalibrated Integrated Gain Error vs Temperature at 7.1 GHz



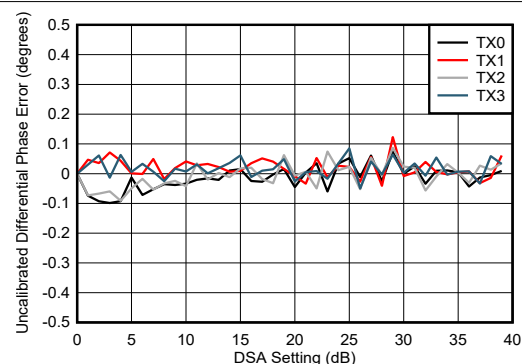
Integrated Gain Error = $\text{Gain}(\text{DSA Setting}) - \text{Gain}(\text{DSA Setting} = 0)$.

Figure 7-535. Calibrated Integrated Gain Error vs Channel at 7.1 GHz



Integrated Gain Error = $\text{Gain}(\text{DSA Setting}) - \text{Gain}(\text{DSA Setting} = 0)$.

Figure 7-536. Calibrated Integrated Gain Error vs Temperature at 7.1 GHz

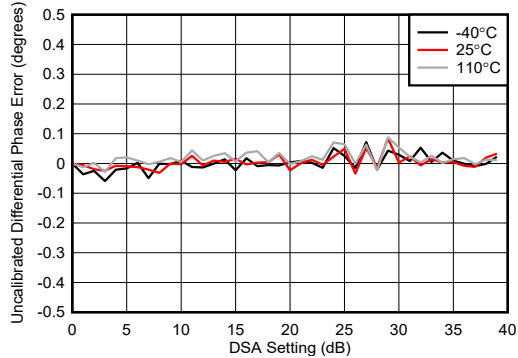


Differential Phase Error = $\text{Phase}(\text{DSA Setting} - 1) - \text{Phase}(\text{DSA Setting})$

Figure 7-537. Uncalibrated Differential Phase Error vs Channel at 7.1 GHz

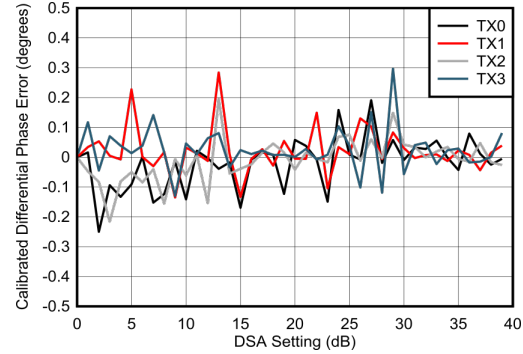
7.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



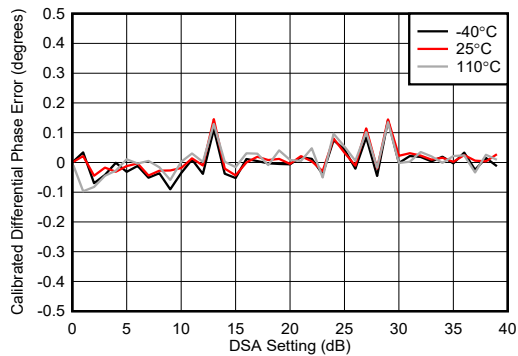
Differential Phase Error = $\text{Phase}(\text{DSA Setting} - 1) - \text{Phase}(\text{DSA Setting})$

Figure 7-538. Uncalibrated Differential Phase Error vs Temperature at 7.1 GHz



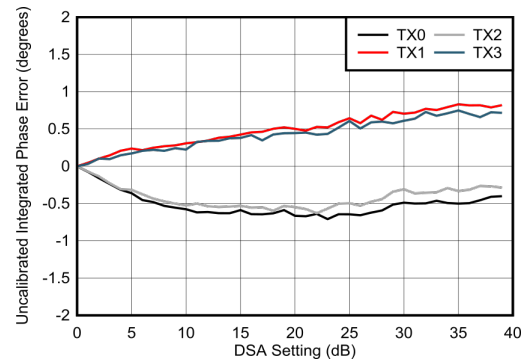
Differential Phase Error = $\text{Phase}(\text{DSA Setting} - 1) - \text{Phase}(\text{DSA Setting})$

Figure 7-539. Calibrated Differential Phase Error vs Channel at 7.1 GHz



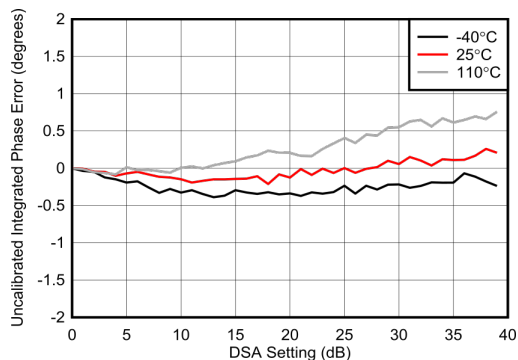
Differential Phase Error = $\text{Phase}(\text{DSA Setting} - 1) - \text{Phase}(\text{DSA Setting})$

Figure 7-540. Calibrated Differential Phase Error vs Temperature at 7.1 GHz



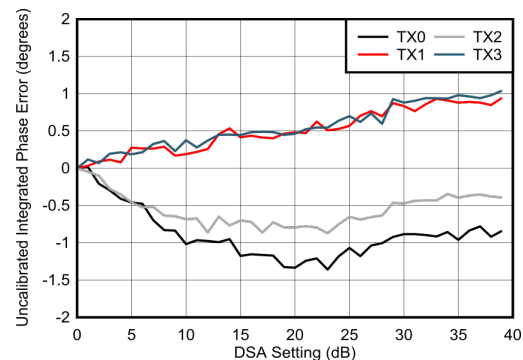
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-541. Uncalibrated Integrated Phase Error vs Channel at 7.1 GHz



Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-542. Uncalibrated Integrated Phase Error vs Temperature at 7.1 GHz



Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

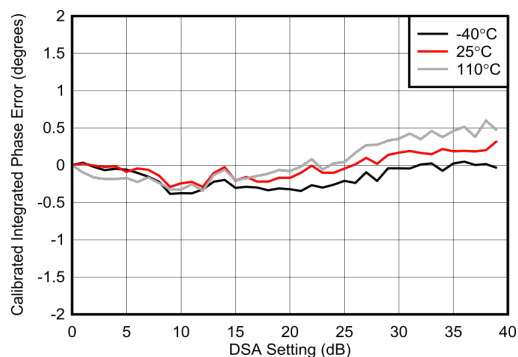
Figure 7-543. Calibrated Integrated Phase Error vs Channel at 7.1 GHz

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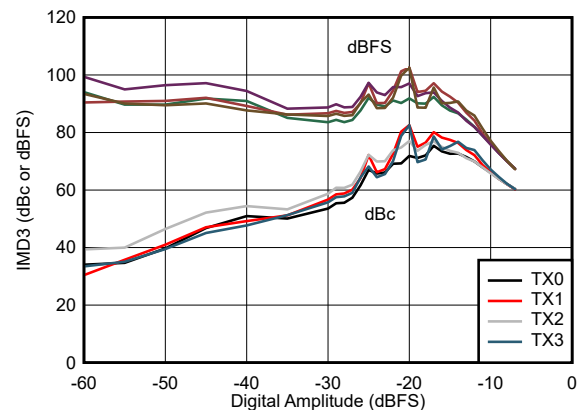
7.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



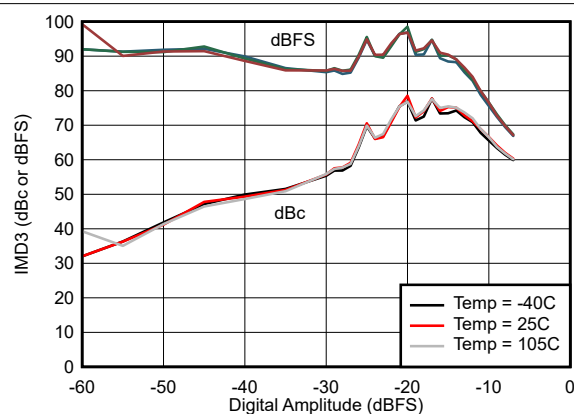
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-544. Calibrated Integrated Phase Error vs Temperature at 7.1 GHz



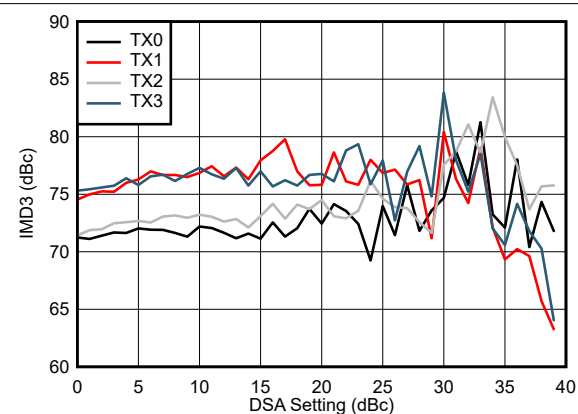
Tone spacing = 50MHz

Figure 7-545. IMD3 vs Digital Amplitude and Channel at 7.1 GHz



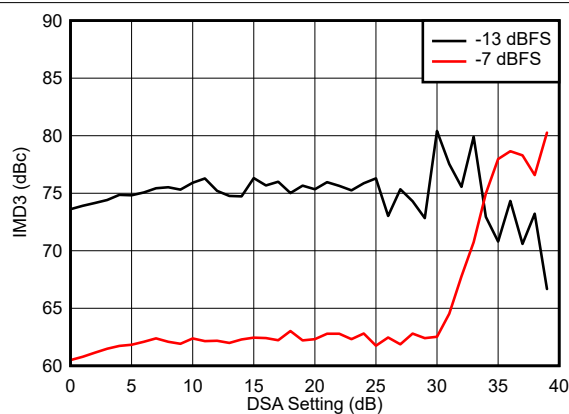
Tone spacing = 50MHz

Figure 7-546. IMD3 vs Digital Amplitude and Temperature at 7.1 GHz



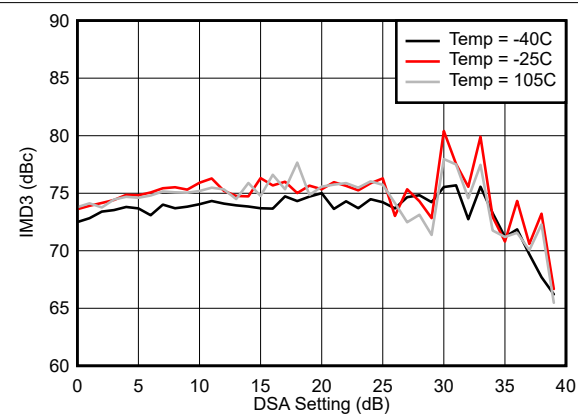
Tone spacing = 50MHz

Figure 7-547. IMD3 vs DSA Setting and Channel at 7.1 GHz



Tone spacing = 50MHz

Figure 7-548. IMD3 vs DSA Setting and Digital Amplitude at 7.1 GHz



Tone spacing = 50MHz

Figure 7-549. IMD3 vs DSA Setting and Temperature at 7.1 GHz

7.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.

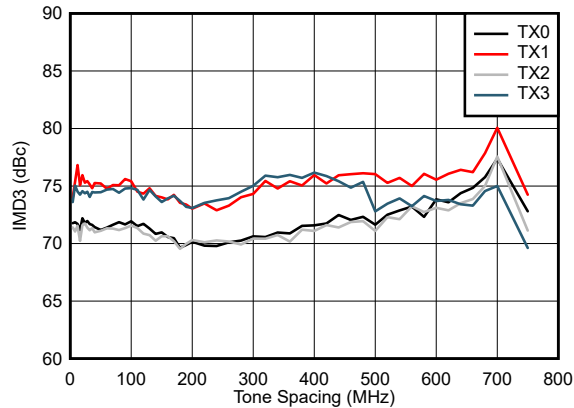


Figure 7-550. IMD3 vs Tone Spacing and Channel at 7.1 GHz

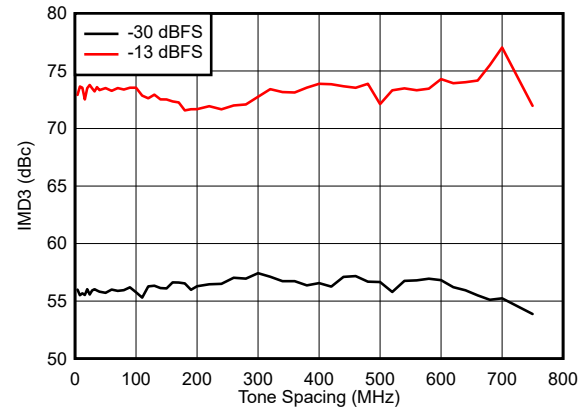


Figure 7-551. IMD3 vs Tone Spacing and Digital Amplitude at 7.1 GHz

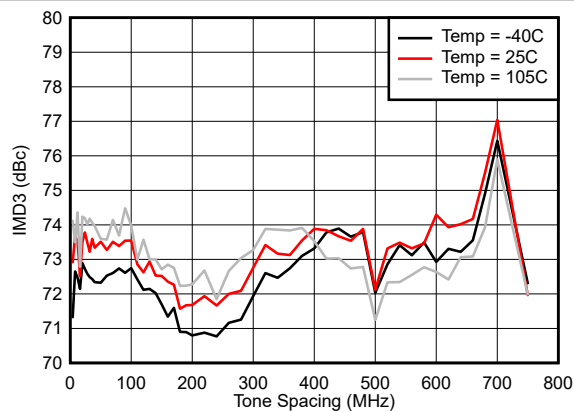
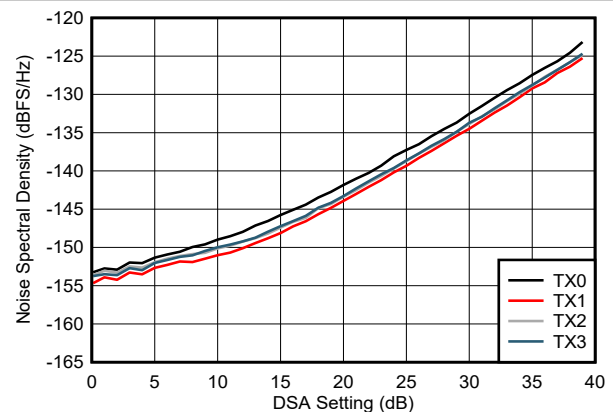
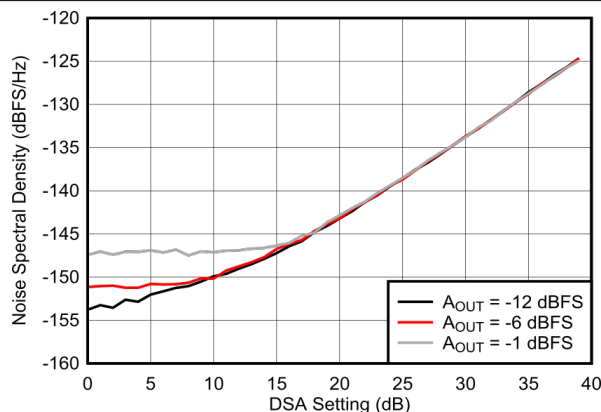


Figure 7-552. IMD3 vs Tone Spacing and Temperature at 7.1 GHz



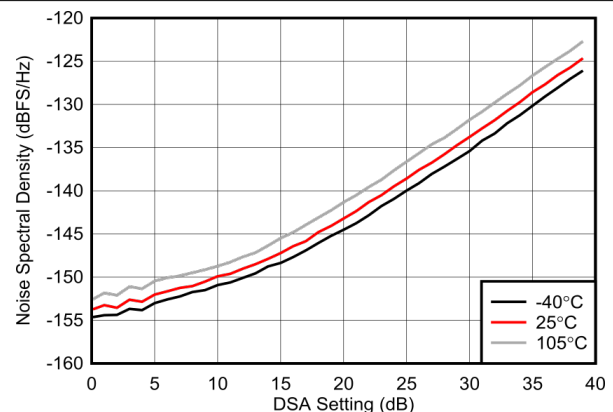
Tone at -12dBFS, 50MHz offset from tone

Figure 7-553. NSD vs DSA Setting and Channel at 7.1 GHz



50MHz offset from tone

Figure 7-554. NSD vs DSA Setting and Amplitude at 7.1 GHz



Tone at -12dBFS, 50MHz offset from tone

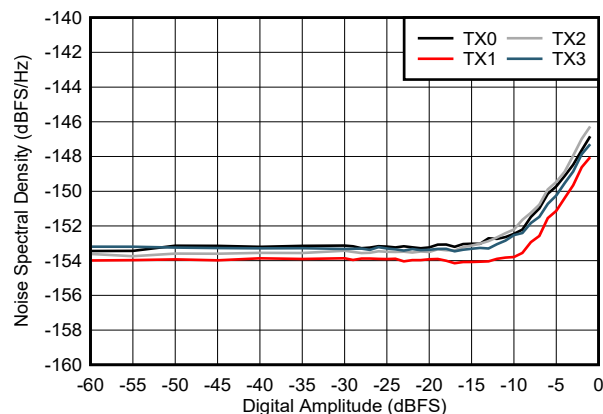
Figure 7-555. NSD vs DSA Setting and Temperature at 7.1 GHz

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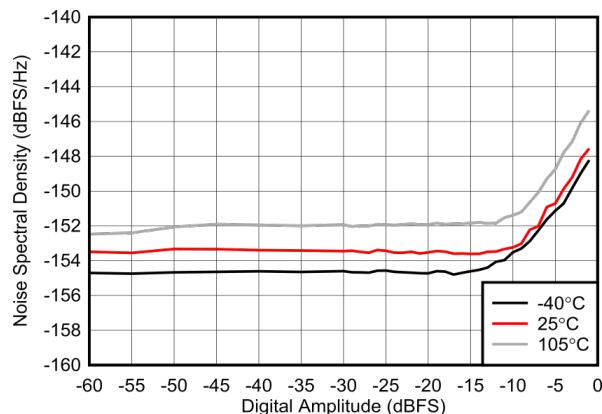
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7.12.13 TX Typical Characteristics at 7.1GHz (continued)

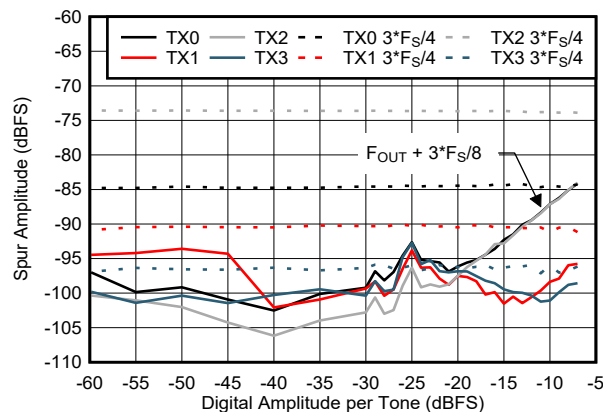
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



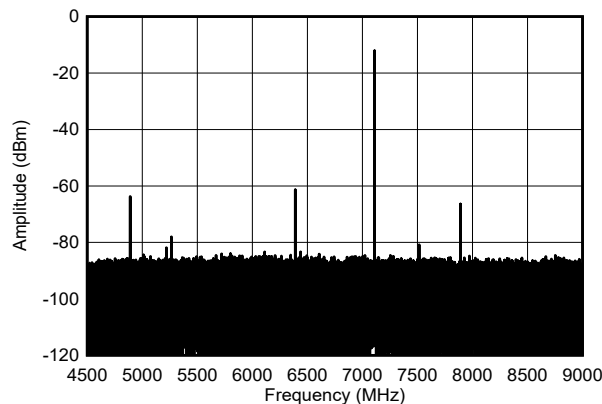
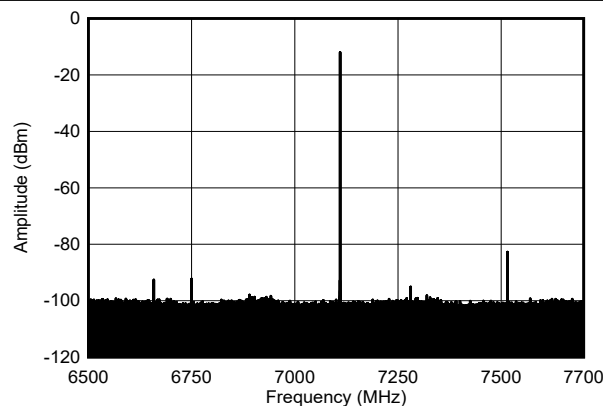
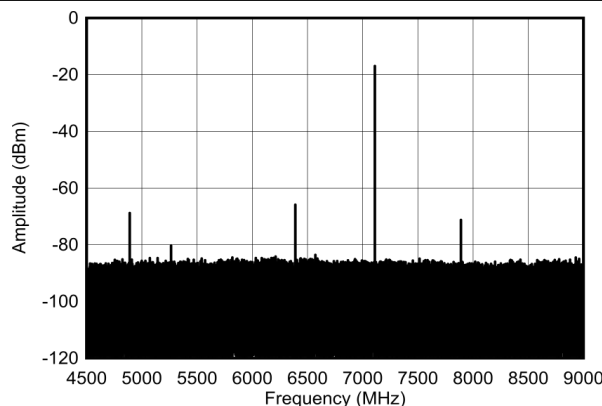
50MHz offset from tone

Figure 7-556. NSD vs Digital Amplitude and Channel at 7.1 GHz

50MHz offset from tone

Figure 7-557. NSD vs Digital Amplitude and Temperature at 7.1 GHz

Inband = 7100MHz \pm 600MHz, excluding IMD3 components,
3*Fs/4 spur not included and shown separately

Figure 7-558. Two Tone Inband SFDR vs Digital Amplitude at 7.1 GHz**Figure 7-559. Single Tone Output Spectrum at 7.1GHz, -1dBFS (Nyquist)****Figure 7-560. Single Tone Output Spectrum at 7.1GHz, -1dBFS (Inband)****Figure 7-561. Single Tone Output Spectrum at 7.1GHz, -6dBFS (Nyquist)**

7.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.

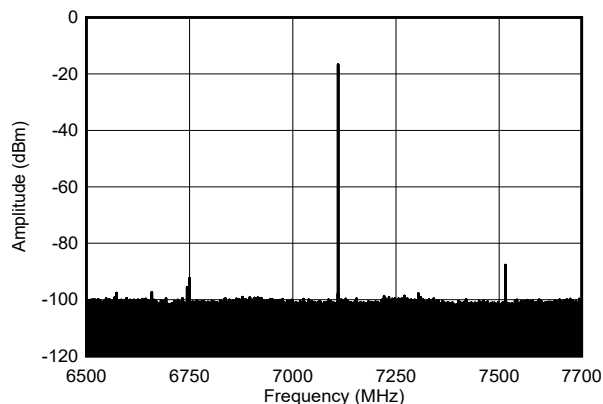


Figure 7-562. Single Tone Output Spectrum at 7.1GHz, -6dBFS (Inband)

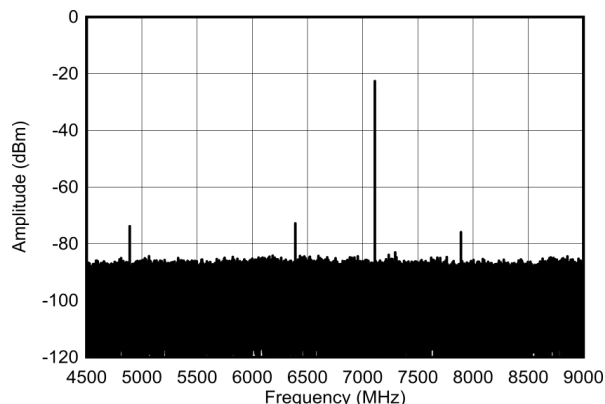


Figure 7-563. Single Tone Output Spectrum at 7.1GHz, -12dBFS (Nyquist)

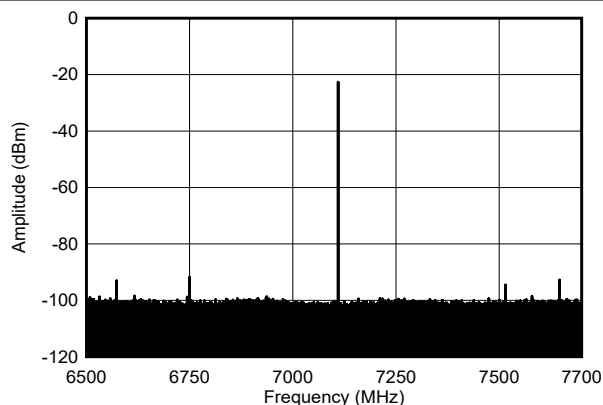
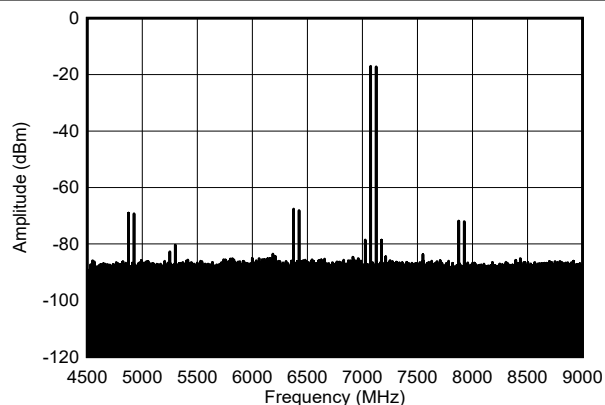
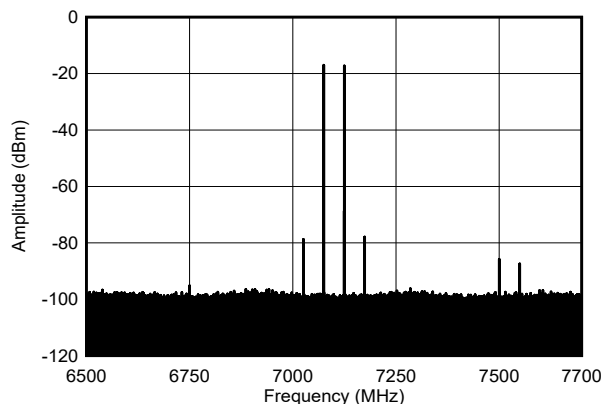


Figure 7-564. Single Tone Output Spectrum at 7.1GHz, -12dBFS (Inband)



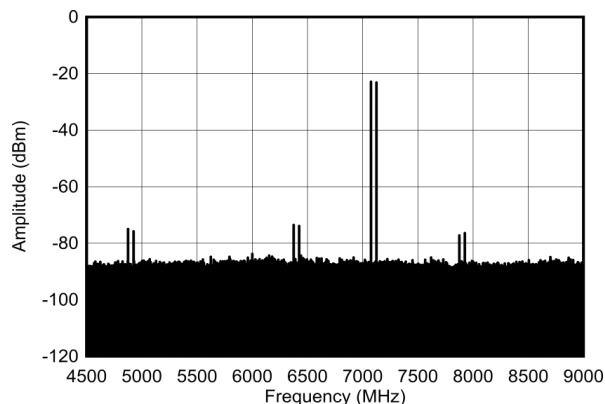
50MHz Tone Spacing

Figure 7-565. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (Nyquist)



50MHz Tone Spacing

Figure 7-566. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (Inband)



50MHz Tone Spacing

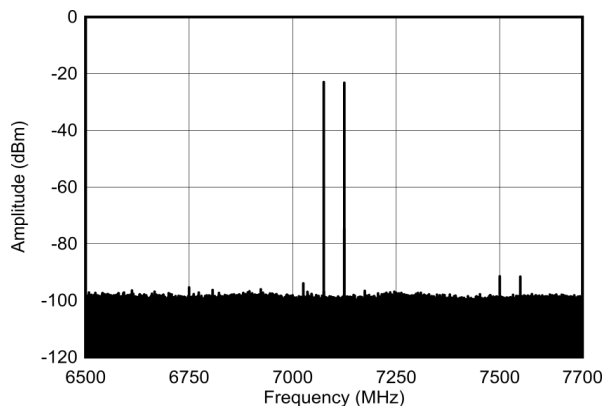
Figure 7-567. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (Nyquist)

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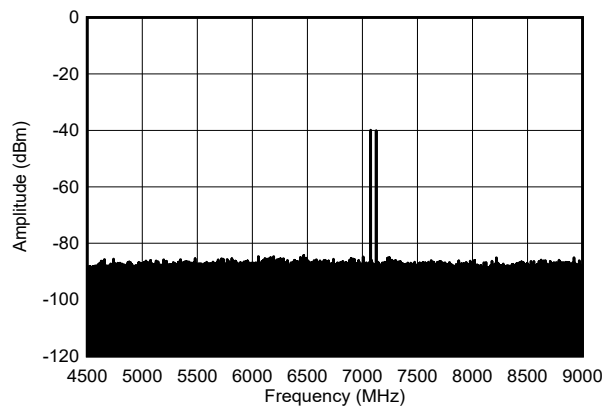
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7.12.13 TX Typical Characteristics at 7.1GHz (continued)

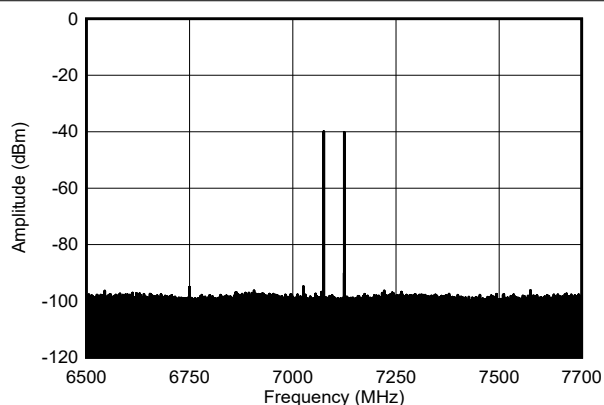
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$, non-interleave mode, $A_{\text{OUT}} = -1\text{ dBFS}$, 1st Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, Dither = 1, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



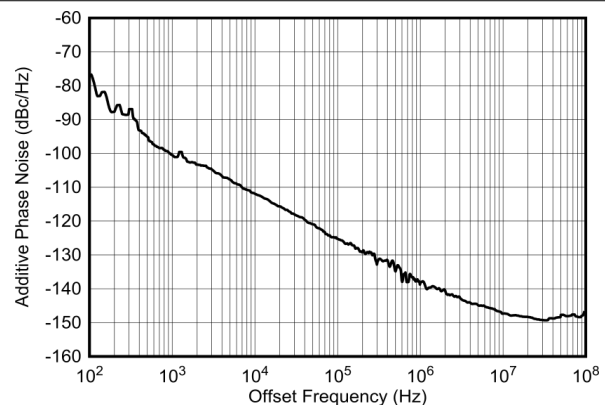
50MHz Tone Spacing

Figure 7-568. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (Inband)

50MHz Tone Spacing

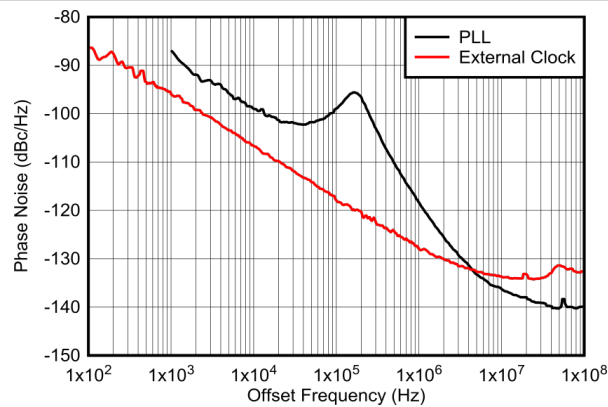
Figure 7-569. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (Nyquist)

50MHz Tone Spacing

Figure 7-570. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (Inband)**Figure 7-571. External Clock Additive Phase Noise at 7.1 GHz**

7.12.14 PLL and Clock Typical Characteristics

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Unless otherwise noted, $f_{\text{REF}} = 491.52 \text{ MHz}$, Phase noise measured at TX output



measured at TX output, normalized to 12GHz by $20 \cdot \log_{10}(12\text{GHz}/f_{\text{OUT}})$

Figure 7-572. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz

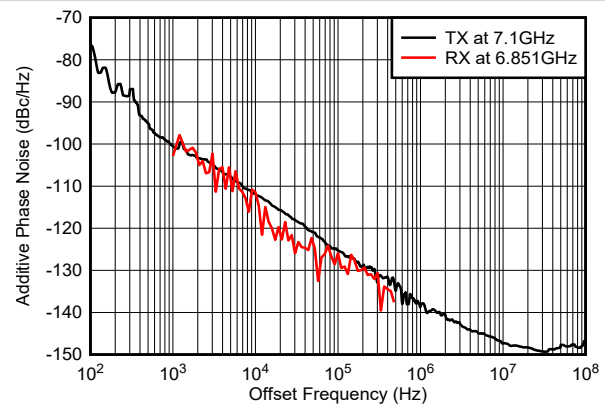
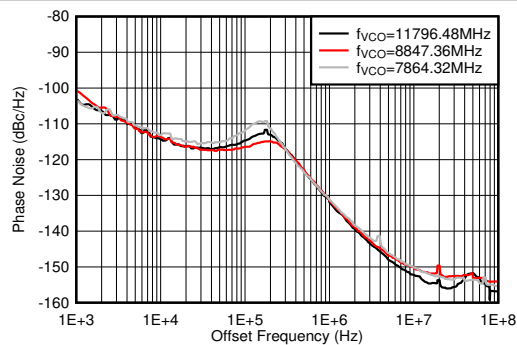
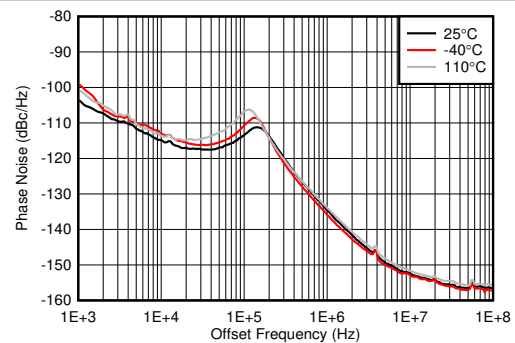


Figure 7-573. TX vs RX Additive Phase Noise at 7GHz



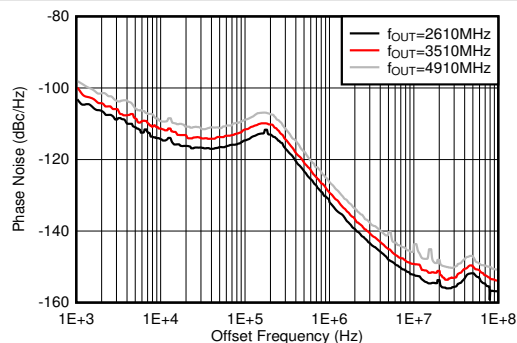
PLL enabled, $f_{\text{REF}} = 491.52\text{MSPS}$, measured at 2TXOUT

Figure 7-574. Phase Noise vs Offset Frequency and f_{VCO} at $f_{\text{OUT}} = 2610 \text{ MHz}$



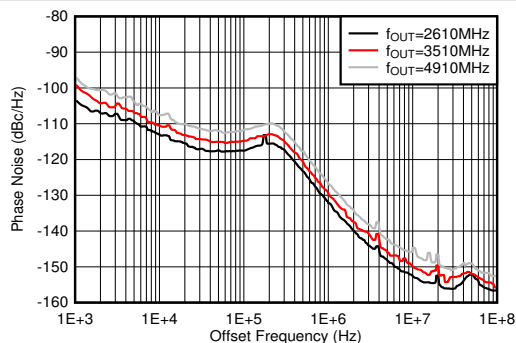
PLL enabled, $f_{\text{VCO}} = 11796.48 \text{ MHz}$, $f_{\text{REF}} = 491.52\text{MSPS}$, measured at 2TXOUT

Figure 7-575. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at $f_{\text{OUT}} = 1910 \text{ MHz}$



PLL enabled, $f_{\text{VCO}} = 11796.48 \text{ MHz}$, $f_{\text{REF}} = 491.52\text{MSPS}$, measured at 2TXOUT

Figure 7-576. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C

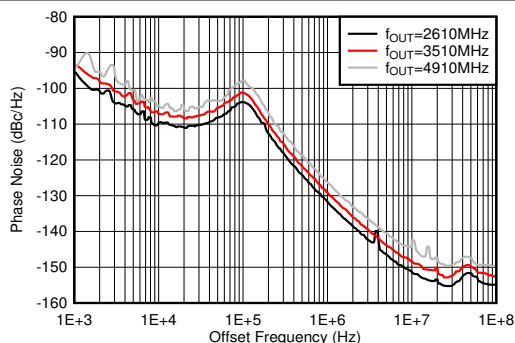


PLL enabled, $f_{\text{VCO}} = 11796.48 \text{ MHz}$, $f_{\text{REF}} = 491.52\text{MSPS}$, measured at 2TXOUT

Figure 7-577. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at -40°C

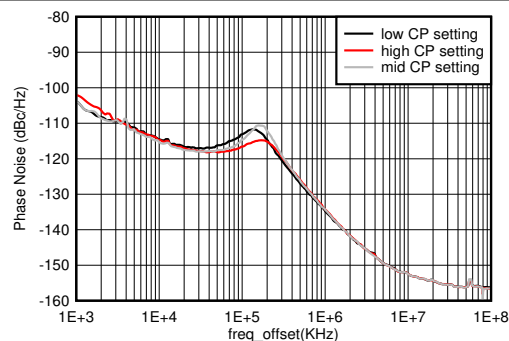
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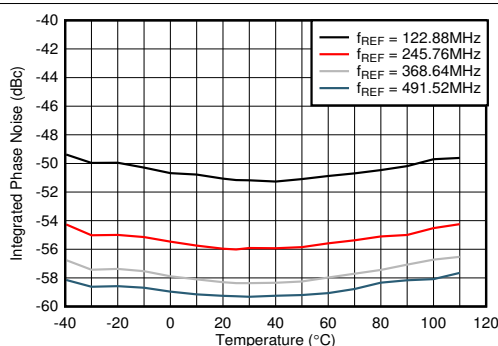
PLL enabled, $f_{VCO} = 11796.48$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-578. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



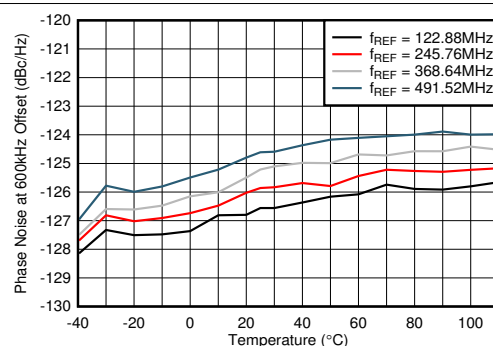
PLL enabled, $f_{VCO} = 11796.48$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-579. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at $f_{OUT} = 2.6$ GHz



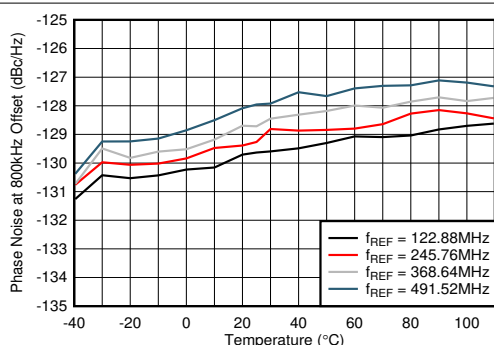
PLL enabled, $f_{VCO} = 11796.48$ MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 7-580. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



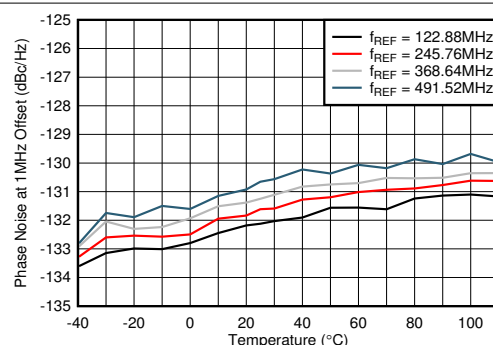
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at 2TXOUT

Figure 7-581. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



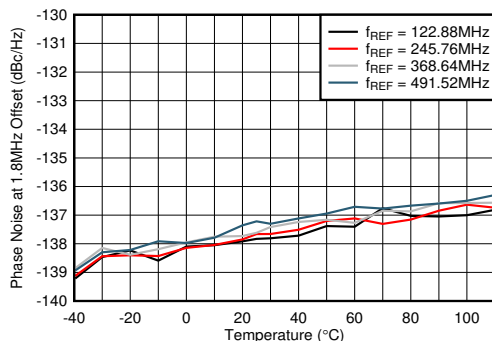
A. PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at 2TXOUT

Figure 7-582. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



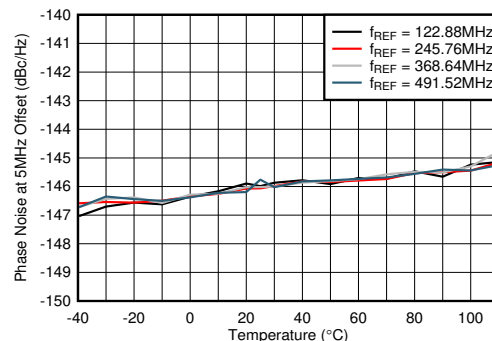
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at 2TXOUT

Figure 7-583. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



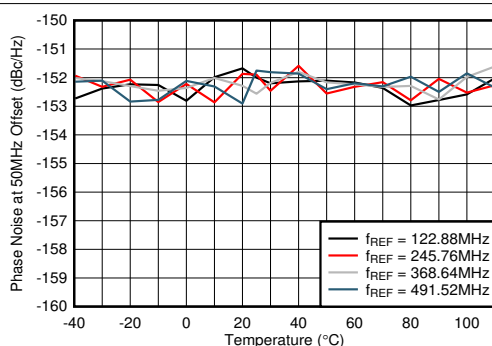
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at 2TXOUT

Figure 7-584. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



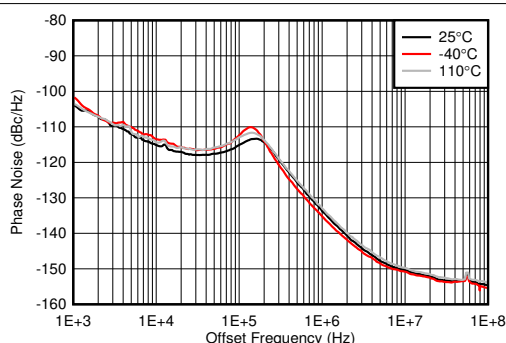
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at 2TXOUT

Figure 7-585. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



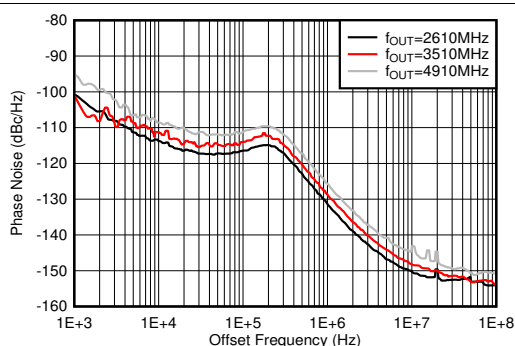
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at 2TXOUT

Figure 7-586. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



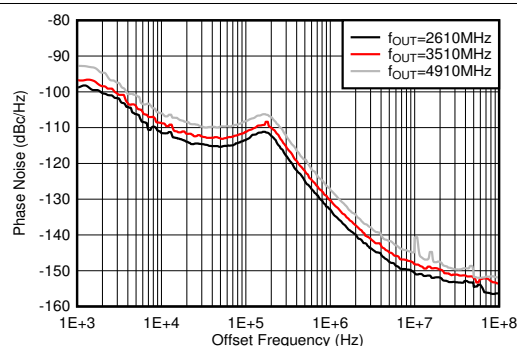
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-587. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz



PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-588. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C

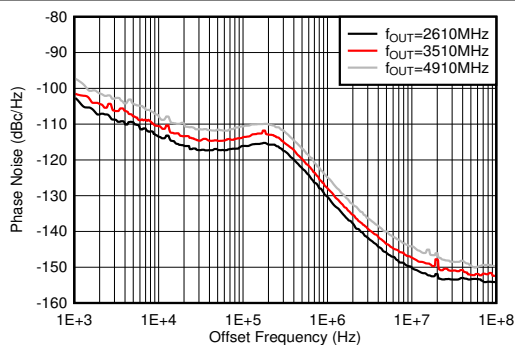


PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-589. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at -40°C

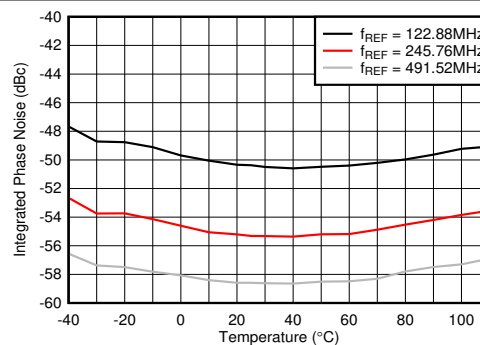
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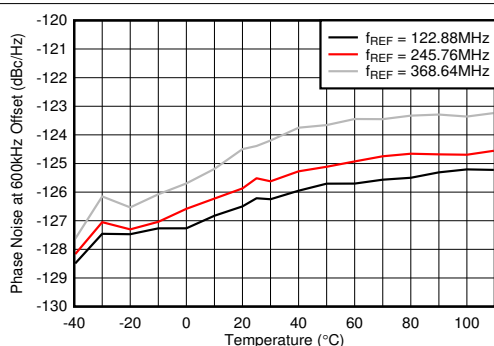
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-590. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



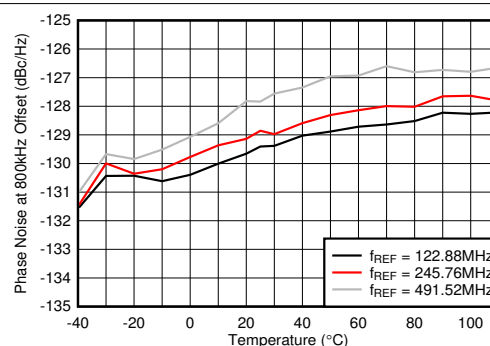
PLL enabled, $f_{VCO} = 9830.4$ MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

Figure 7-591. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



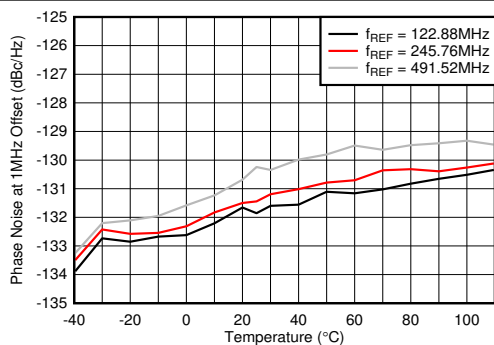
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at 2TXOUT

Figure 7-592. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



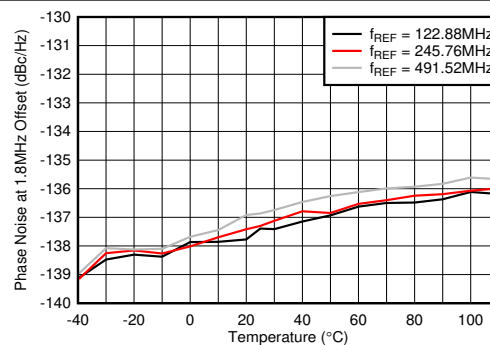
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at 2TXOUT

Figure 7-593. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



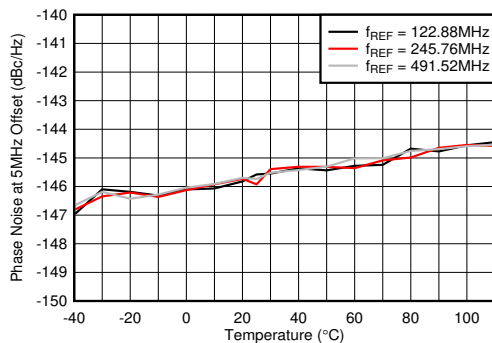
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at 2TXOUT

Figure 7-594. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



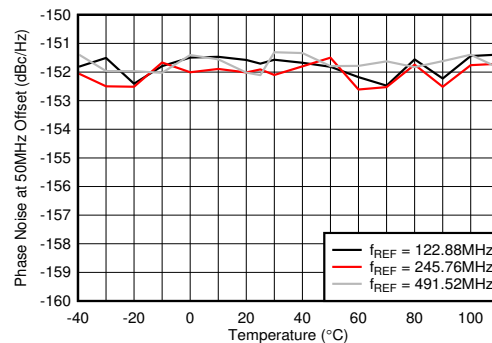
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at 2TXOUT

Figure 7-595. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



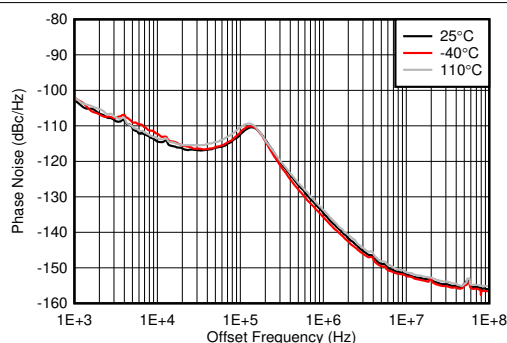
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at 2TXOUT

Figure 7-596. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



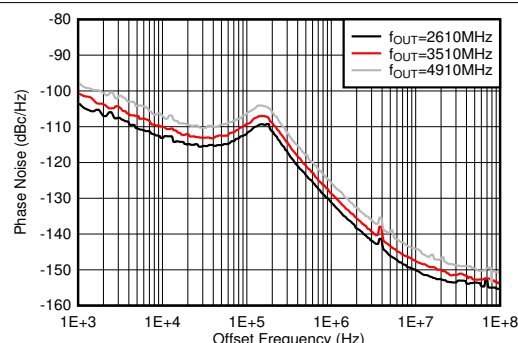
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at 2TXOUT

Figure 7-597. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



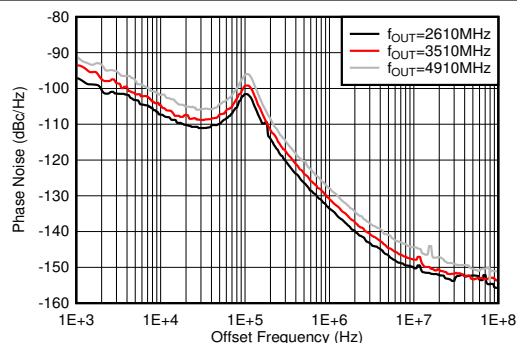
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-598. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz



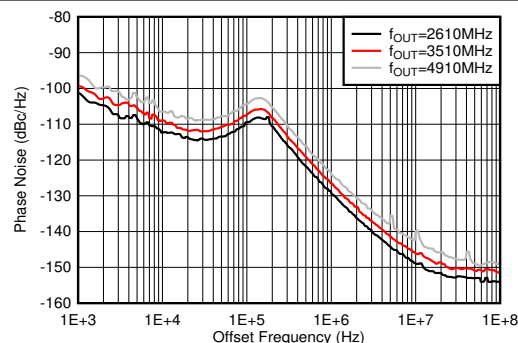
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-599. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-600. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at -40°C

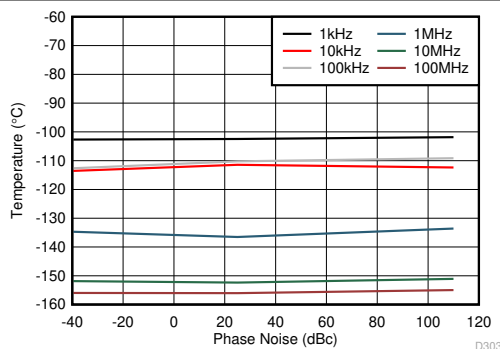


PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at 2TXOUT

Figure 7-601. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C

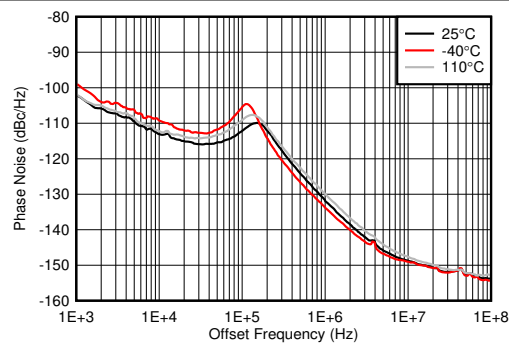
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PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS,
minimum LPF BW, measured at 2TXOUT

Figure 7-602. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at $f_{OUT} = 2.6$ GHz



PLL enabled, $f_{VCO} = 7864.32$ MHz, $f_{REF} = 491.52$ MSPS,
measured at 2TXOUT

Figure 7-603. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz

8 Detailed Description

8.1 Overview

The AFE7900 is a high performance multi-channel transceiver, integrating 4 RF sampling DAC transmitter paths, four RF sampling ADC receiver paths and two RF sampling ADC feedback or auxiliary receiver paths.

Each receiver (RX) path includes a DSA (Digital Step Attenuator), followed by a 3-GSPS non-interleaved RF sampling ADC. Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous AGC control, and a RF overload detector for device reliability protection. The RX ADC is followed by a flexible dual or single band DDC (digital down converter) to reduce the sample rate to only the bands of interest. The FB ADC is followed by a single wide BW DDC.

Each transmitter (TX) includes a dual or single band DUC (digital up converter), followed by a 12-GSPS RF sampling DAC driving a wideband RF amplifier (DSA). The DAC has zero order hold output to emphasize the 1st Nyquist output and a mixed mode output to emphasize the 2nd Nyquist zone.

In single DUC and DDC mode, each DUC and DDC path integrates 16 independent NCOs that allows fast switching between RF frequencies, while maintaining the phase of each NCO when not in use. In dual DUC and DDC mode, each path integrates two NCOs that allows fast switching between two RF frequencies, while maintaining the phase of each NCO when not in use.

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8.2 Functional Block Diagram

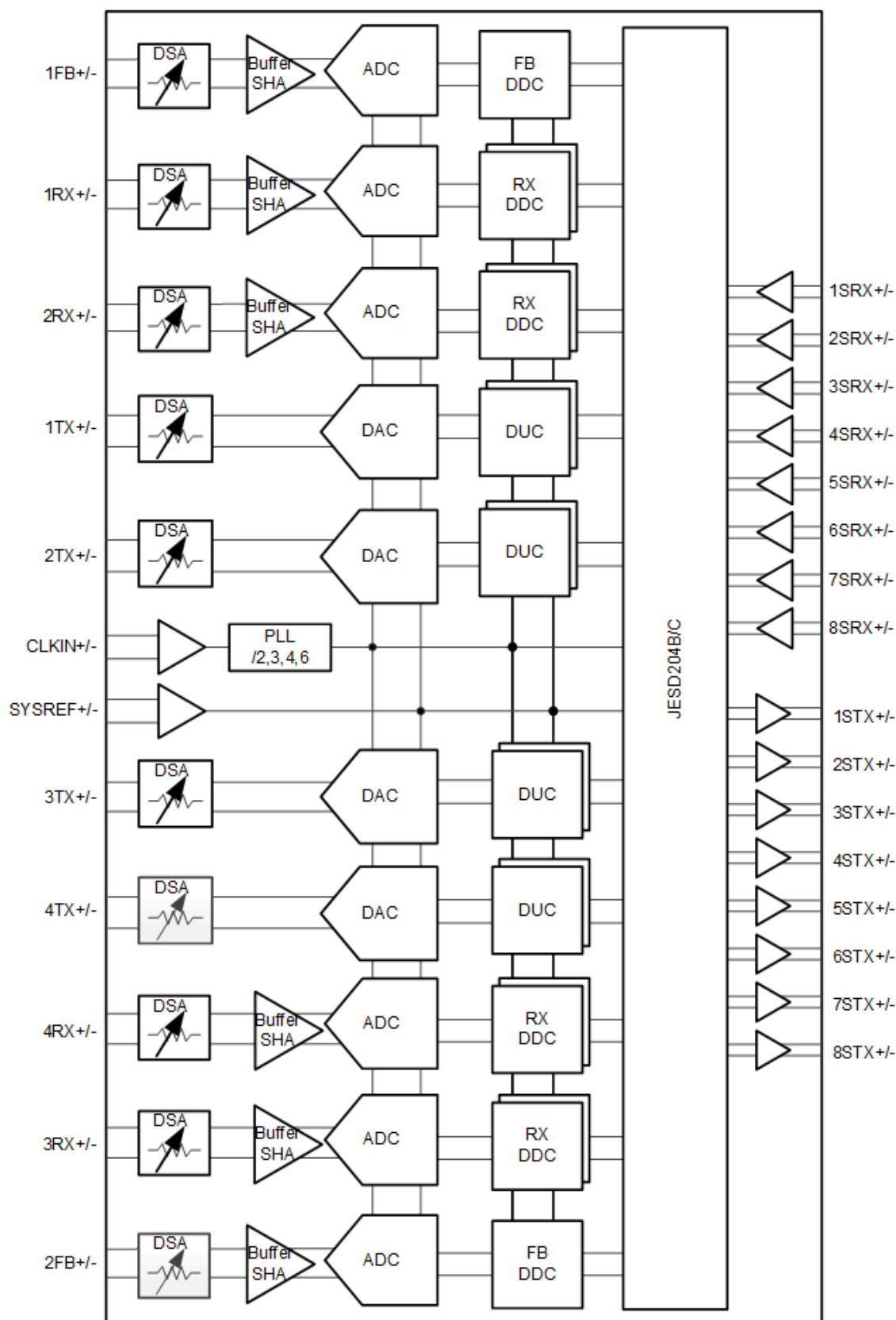


Figure 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Operation Modes

The AFE7900 can be configured in the following operating modes:

- **Power-On-Reset Mode:** this is the status of the device at power up and after any device $\overline{\text{RESET}}$ event.
- **Active Mode:** all clocks are running, all PLL are locked, all circuits are properly biased, JESD links are established, and digital functions are turned on.
- **Standby Mode:** defined for the transmitters, receivers, and feedback chains. In this mode, the chain is set to minimum power dissipation, while maintaining a fast wake-up time to active mode (typically less than 2 μs), by selectively powering down blocks of the chain. The JESD links are maintained in this mode. This mode is configured through the SPI and then activated through the allocated enable GPIO pins.
- **Sleep Mode:** in this status the device power dissipation is further reduced compared to the Standby Mode, but the wake-up time to Active Mode is slower. The JESD links are shut down in this mode and will need to be re-established when coming out of sleep mode. The Sleep Mode can be configured through the SPI and it is activated through the Sleep pin. In the default configuration, all blocks are off, but the PLL, the internal power management bias and internal controller.

8.3.2 Receiver (RX) Chain

The AFE7900 receiver block diagram with dual DDCs is shown in [Figure 8-2](#) and a single DDC in [Figure 8-3](#). Peak power detectors, a DSA, and a 3-GSPS non-interleaved ADC form the analog portion of the RX chain. The digital section of the receive chain includes digital peak and RMS power detectors, an autonomous AGC, complex mixers to down convert the wanted signal to baseband, decimation filters to reduce the sample rate to the target output rate, a digital compensation block to provide constant input-to-output gain and an output format block.

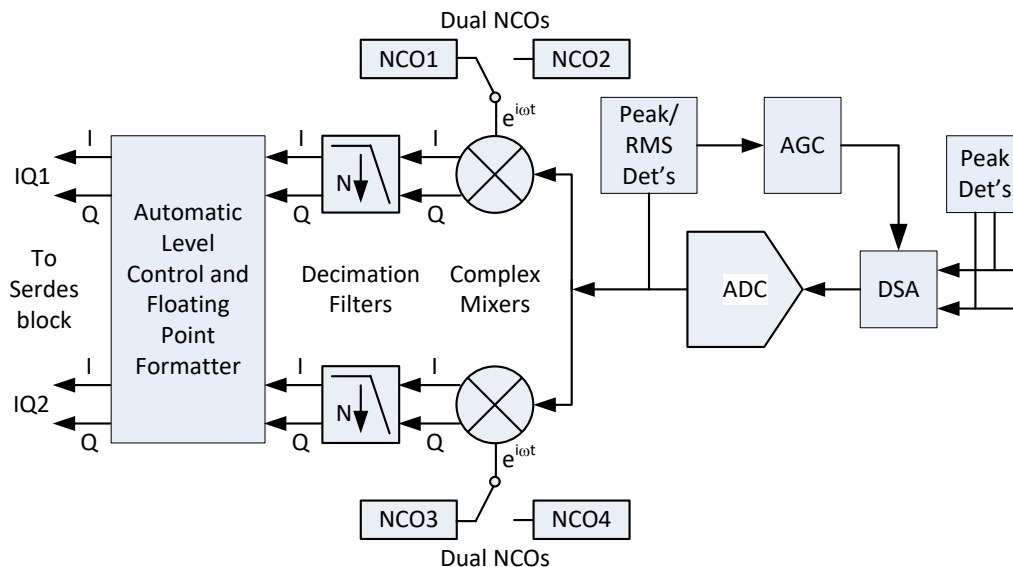
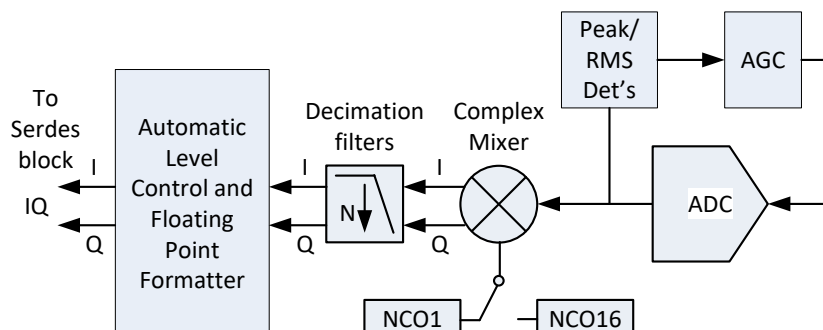


Figure 8-2. RX Chain Block Diagram in Dual DDC Mode

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**Figure 8-3. RX Chain Block Diagram in Single DDC Mode****8.3.2.1 RX Chain DSA**

The input stage of the receiver chain is a programmable Digital Step Attenuator (DSA), whose goal is to extend the effective dynamic range of the RX chain by attenuating the large signals before reaching the ADC. The attenuation setting of the DSA can be controlled in several ways through the Serial Programming Interface (SPI), GPIO pins, or an internal Automatic Gain Controller (AGC). At power up the default method to change the DSA setting is the direct access to the dedicated internal registers through the SPI. For a faster change of the DSA attenuation value, the AFE7900 has the option to use dedicated GPIO pins to directly control the DSA setting.

8.3.2.2 RX DSA Gain and Phase Correction

The RX DSA has a gain and phase correction block to reduce the error in gain and phase for each DSA setting. This is expected to be calibrated in the customer factory or at start-up through the DSA calibration macro.

8.3.2.3 External DSA Control

The device supports different modes of the direct DSA control access through the pins.

- Parallel 3 bits per RX chain. In this mode, 3 GPIO balls are allocated for each RX chain to implement 3 bits control of the DSA. The actual DSA attenuation setting is defined according to [Equation 1](#):

$$DSA_ATT_{act} = \min(ATT_{min} + B[2..0] \times ATT_{step}, ATT_{max}) \quad (1)$$

where

- $B[2..0]$ are the external controlling 3 bits (through parallel GPIO pins).
- ATT_{min} is a variable defining the minimum attenuation. It is programmable through the SPI and it can be set differently for each of the 4 receiver chains.
- ATT_{step} defines the step of the controlling word. It is programmable through the SPI and it can be set differently for each of the 4 receiver chains.
- ATT_{max} is the maximum attenuation, configurable through the SPI up to 25 dB. It is possible to define two different ATT_{max} values, one for RX1/RX2 and one for RX3/RX4.
- Shared Parallel 5 or 6 bits with DSA select and latch. In this mode the 0 to 25 dB range of the DSA can be controlled by 5 or 6 parallel bits with 1 dB steps or 6 parallel bits with 0.5-dB steps. For every two receivers, there are allocated 5 pins for the parallel word control, a separate select and latch pins allow to load the DSA setting into the selected DSA.

When the AFE7900 internal AGC is enabled the RX chain DSA attenuation setting is directly controlled by the internal AGC block.

All the above modes can be configured through the SPI.

8.3.2.4 RX Peak and Power Detectors

[Figure 8-4](#) shows the locations of the analog and digital detectors in the RX chain.

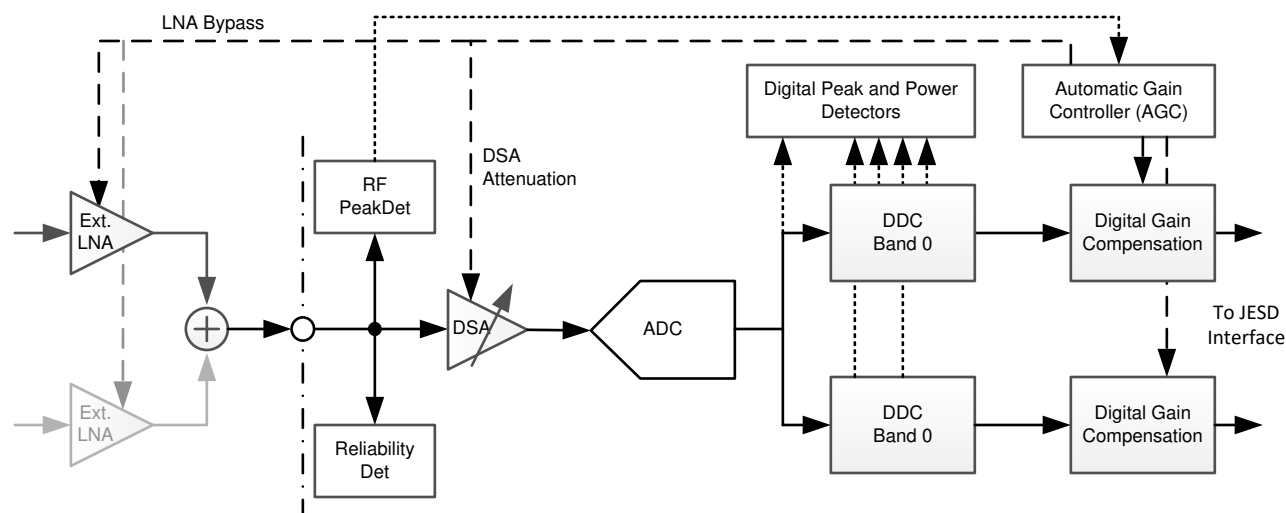


Figure 8-4. RX Chain: AGC and Detectors

8.3.2.4.1 RF/Analog Peak Detectors

Located at the RF input of each receiver chain, the RF/analog peak detector thresholds are scaled based on the actual DSA attenuation setting, and can be equivalent to the DSA output. Only an attack detector is available. Each one has programmable thresholds, configurable in 1-dB steps from –10 dBFS to +1 dBFS. The number of threshold crossings is counted over a block period, programmable from approximately 10 ns to 40 ms. The number of crossings is then compared to a programmable threshold, which then can generate a trigger.

In internal AGC mode, the detectors can be used to control the DSA gain and/or LNA bypass. In external AGC mode, the detectors outputs can be made available at dedicate GPIO pins.

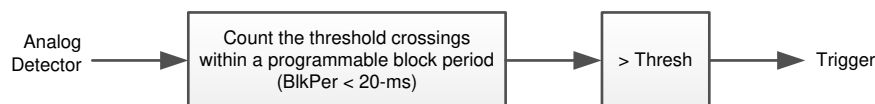


Figure 8-5. RF/Analog Peak Detector Block Diagram

8.3.2.4.2 Reliability RF Peak Detector

The AFE7900 integrates at the RF input pins of the receiver chain a dedicated peak detector that monitors the input levels to ensure that the levels do not exceed the maximum usable full scale power. Both attack and decay are built-in (in digital) to the same analog reliability detector. When the maximum full scale is exceeded, the DSA is set to maximum attenuation, the difference in gain is compensated in digital, and a flag available in the status register or through a dedicated pin is enabled.

The reset of the alarm can be done in 3 different modes:

- Decay detector indicating that signal level is lower than reliability levels.
- Decay detector indicating that signal level is lower than reliability levels along with an SPI bit set by the user.
- Automatically clear it after a programmable time.

The reliability detector mechanism is same in both internal and external AGC Mode.

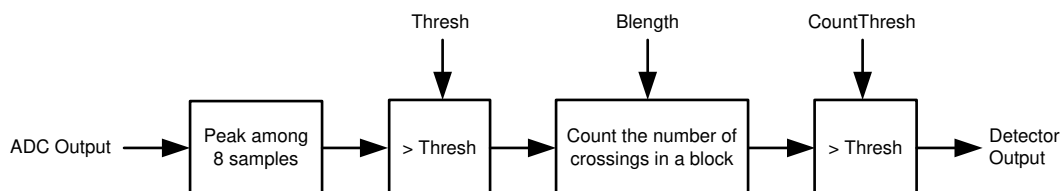
8.3.2.4.3 ADC Digital Peak and Power Detector

At ADC output, there are multiple digital peak and power detectors. In a typical use case the peak detector is used to maintain the level at the ADC input below the programmed back-off.

Two independent thresholds for attack (big and small step) and decay (big and small step) can be configured. All four detectors are identical. The number of threshold crossings is counted over a programmable block period and compared to configurable target value to determine that the detector has triggered. In internal AGC mode, the detectors can be used to control the DSA gain and/or LNA bypass. In external AGC mode, each peak detector output can be made available at pins.

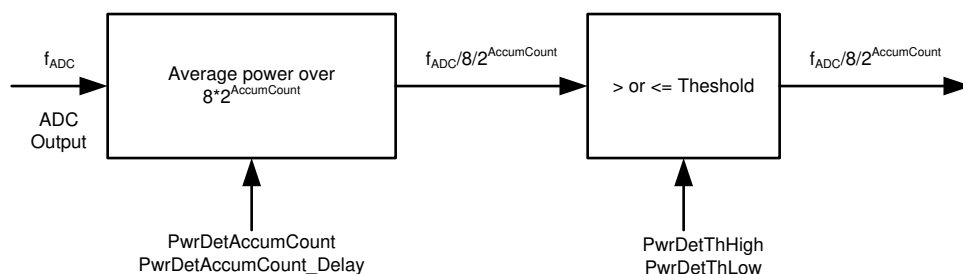
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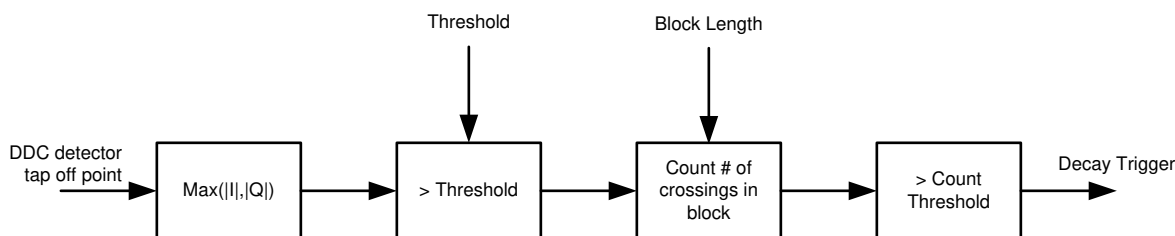
**Figure 8-6. ADC Output Digital Peak Detector Block Diagram****Table 8-1. Digital Detectors Parameters**

PARAMETER	DESCRIPTION	TYPE	RANGE
Thresh	Level comparison threshold	Linear 12-bit resolution	0 to 4095 Threshold in dBFs = $20 \times \text{Log}(\text{Thresh}/4095)$
Blength	Time interval where to count number of crossings	Integer	Integer multiples of $f_{\text{ADC}}/8$, up to 20 ms.
CountThresh	Number of crossing threshold	Integer	1 to Blength

The digital power detectors share the same tap off points as the digital peak detectors and have both attack and decay thresholds. Power is calculated as the square of the ADC output value. The integration time is between 10 ns and 10 ms, and the threshold can be configured between 0 and –30 dBFS with 0.2-dB steps (see [Figure 8-7](#)).

**Figure 8-7. ADC Output Digital Power Detector Processing****8.3.2.4.4 DDC Digital Peak Detectors**

The digital downconverter (DDC) offers various tap off points for digital peak detectors. In dual DDC modes, each DDC can have separate detectors. The block diagram of the detector is shown in [Figure 8-8](#). The Max of the absolute value of I and Q is compared to a programmable threshold. The number of crossings within a time block of programmable length is counted, and this is compared to a threshold for the final detector output.

**Figure 8-8. DDC Digital Peak Detector Block Diagram**

It is expected that the tap off point either at the DDC output or before the final decimation stage would be used. [Table 8-2](#) shows the bandwidth of the tap off point before the final DDC decimation stage for different sample rates and decimation factors.

Table 8-2. DDC Detector Tap Off Point Before Final Stage

f_{ADC} (MSPS)	DECIMATION FACTOR	AGC BW (MHz)
3000	8	+/- 200

Table 8-2. DDC Detector Tap Off Point Before Final Stage (continued)

f_{ADC} (MSPS)	DECIMATION FACTOR	AGC BW (MHz)
2500	10	+/- 200
3000	12	+/- 200
3000	16	+/- 150
2500	20	+/- 100
3000	24	+/- 100
3000	32	+/- 75
2500	40	+/- 50
3000	48	+/- 50

8.3.2.5 Internal Automatic Gain Control (AGC)

The AFE7900 receiver chain integrates all the blocks (multiple analog and digital detectors and an AGC controller) to enable an autonomous Automatic Gain Control. The AGC, detectors and gain control options are shown in [Figure 8-4](#). Four different analog peak detectors are located in the RF portion of the RX chain. At the ADC output, there are four digital peak detectors and one power detector. There are also peak detectors in the digital down converters (DDCs), which are then band-specific for dual band devices and configurations.

In internal AGC mode, the output of each detector goes to the internal AGC controller that sets the RX DSA attenuation setting based on the programmed configuration, which includes comparison thresholds, integration time for attack and decay, and so forth. In this mode, the device has also the option to control an external gain step (like a LNA bypass control, for example) through dedicated GPIO pins. The integrated Digital Gain block can be used to implement the Digital Gain Compensation (DGC) function, which compensates for the RF gain change in digital so that the overall gain from analog input to JESD output is constant.

8.3.2.5.1 Timing Control of the AGC

The AGC has options for controlling how the AGC behaves during switching between IDLE, RX, and FB modes during TDD operation. For FDD, it is expected that the AGC would run continuously. The AGC start can also be delayed by the programmable value.

There are several options to specify the condition of the AGC during FB and IDLE modes and at the start of the RX mode. The AGC can be programmed to continue with the same gain as at the end of the previous RX mode. Alternatively, the AGC gain restarts with the default gain and LNA bypass state.

The maximum and minimum DSA setting can also be programmed. The DSA attenuation will not exceed this range. After the AGC changes the gain, the detector block accumulation will restart. The restart time can be delayed by a programmable value. This will prevent transitory effects of the gain change from affecting the next block accumulation.

The AGC can be frozen at the current gain settings and stop updating through SPI programming or the dedicated GPIO pins.

It is also possible to determine if the AGC DSA or LNA bypass setting has changed since the last inquiry through SPI programming and readback the DSA and LNA bypass actual values:

- TDD Mode – Carry over the RX gain from previous RX time slot.
 - Also has an option to start with a default gain setting for every RX time slot.
 - Decay Detectors can carry over the state from one RX time slot to the next RX time slot.
 - Attack Detectors are always reset during RX OFF
- Internal AGC Freeze either through register or pin – Freezes the state of the Detectors and the gain information
- Gain Swap Mode – treated similar as TDD Mode by the AGC Control algorithm
 - The gain will “be frozen during Gain Swap and continue after Gain Swap is removed” or “restart with default setting after Gain Swap is removed”

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- Analog Gain settings during “Gain Swap” can be configured for DSA and the LNA’s of both the bands

8.3.2.5.2 Temperature Compensation for External LNA Gain

The External LNA gain for one or both bands can be pre-configured through SPI registers as a function of temperature. There are 32 gains and phases as a function of temperature range for each band LNA. The device temperature can be used as an indicator of the external LNA temperature. Optionally, the external LNA gain can be dynamically programmed through SPI registers

8.3.2.5.3 AGC Flow

The AGC flow is shown in [Figure 8-9](#). The flow starts with the reliability detectors, then attack detectors, and finally the decay detectors.

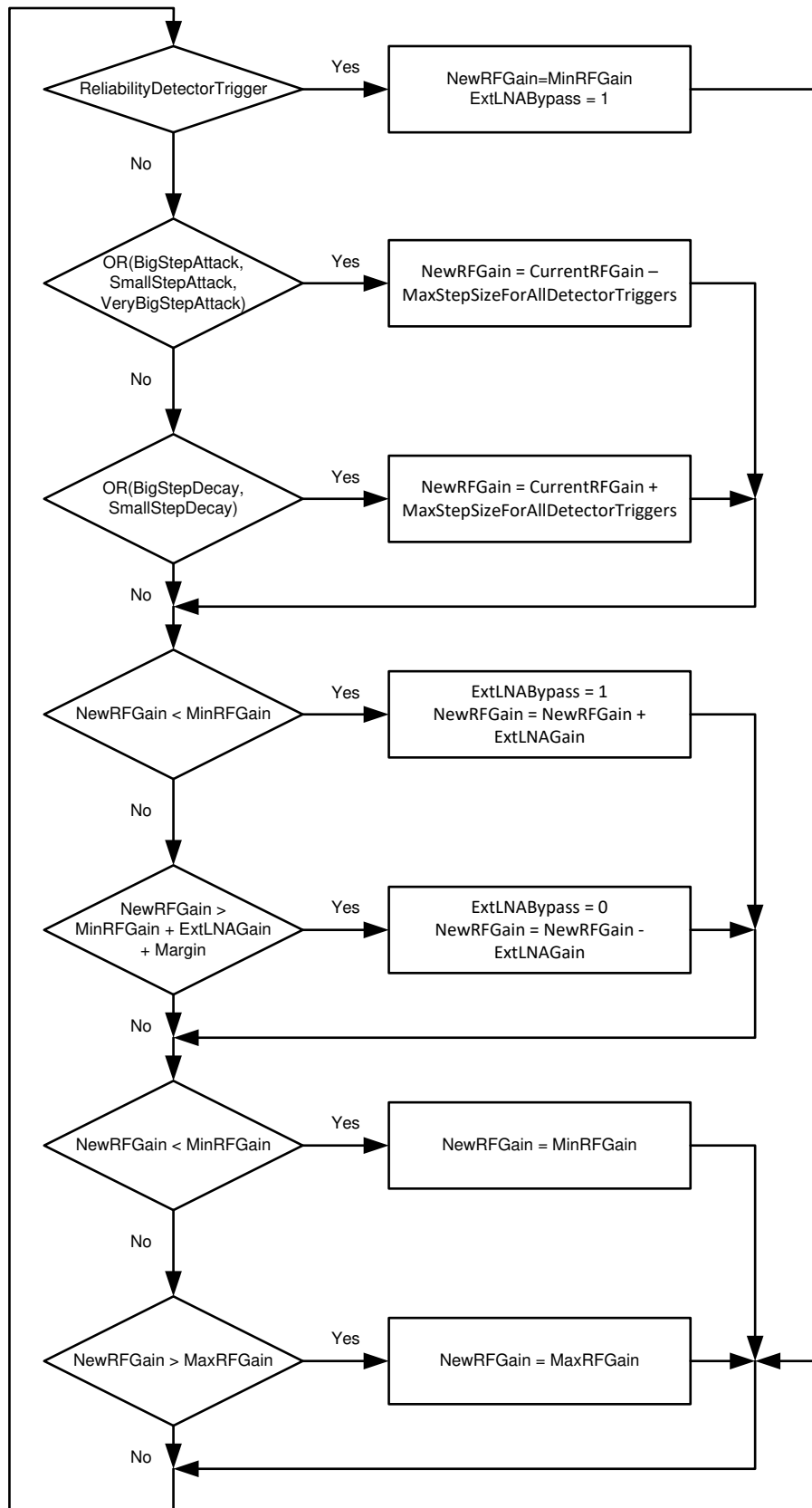


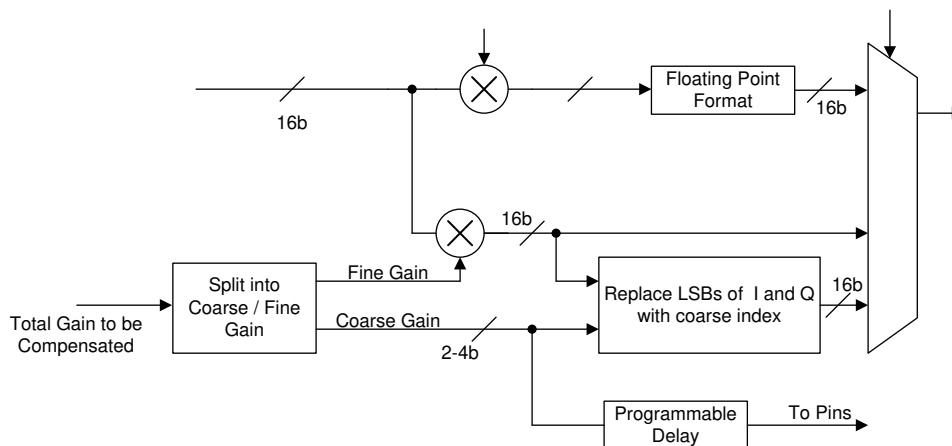
Figure 8-9. AGC Flow

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8.3.2.5.4 Digital Gain Compensation (DGC) for Internal AGC

The AFE7900 has a digital gain compensation (DGC), also known as the automatic level control (ALC) block that provides constant gain from the device input (or LNA input when using the LNA bypass control) to the DGC output when using the internal AGC. As shown in Figure 8-10, the DGC block also has several methods to increase the range of the output data. In the first mode a floating point format is used to represent the output in 16 bits (Ex: 2 bits exponent, 1 bit sign, 13 bit mantissa). In the second mode, the gain to be applied to the signal is split into coarse and fine gains. The third mode is not to do any gain compensation, represent the data in 15 bits, and use an LSB to encode the 5-bit gain value (in dB) onto an LSB using a specified frame structure. In this case, any change in gain can be communicated only at the next frame (Ex: Frame Length = 20 bits) and cannot be on a sample-by-sample basis.

**Figure 8-10. Digital Gain Compensation Modes****8.3.2.5.4.1 Floating Point Format**

The device includes a floating point format for the RX output to account for the higher signal range provided when using the RX DSA. TI recommends to use 16-bit resolution, which is only available for JESD204B/C formats with 16 or more bits. Using a 12-bit JESD204B/C format is possible, but since 2 or 3 bits are used as an exponent, the floating point format with 12-bit JESD204B/C output resolution provides only 9 or 10 bits of significant resolution, which will result in a significant degradation in output SNR. The floating point format is defined as follows (similar to IEEE Standard 754-2008):

- S = sign, $S \in \{0, 1\}$
- E = exponent, $0 \leq E \leq 2^w - 1$, where w = width of the exponent field
- T = significand, $0 \leq T \leq 2^t - 1$, where t = width of the significant field = $16 - w - 1$
- $p = t + 1$ = precision of the floating point number in bits

Option 1:

- For $E = 0$, the sample value $v = (-1)^S \times T$ (that is, $ABS(v) < 2^t$)
- For $E > 0$, sample value $v = (-1)^S \times (2^t + T) \times 2^{(E-1)}$ (that is, $ABS(v) \geq 2^t$).

Option 2:

- For all values of E , sample value $v = (-1)^S \times T \times 2^E$.

The selection of option 1 or 2 is in register field `FLOAT_PT_MODE`. Allowed values for the exponent width (w) are 2 or 3, selected in field `FLOAT_PT_FORMAT`. The 16-bit word is formatted as in Table 8-3.

By default the gain compensation is justified at the maximum compensation so that the full-scale range is supported at the DGC output. It automatically computes this based on the gain range that must be supported by the DGC. This is indicated by the `TOTAL_GAIN_RANGE` register in DGC. The justification is rounded off on the higher side to power of 2 (multiples of 6.02 dB).

The conversion to floating point is as follows:

1. First, define Signal = DDC output bits × DGC gain (linear). The DDC output is 16 bits, and DGC = digital gain correction, which applies a gain equal to the total attenuation (DSA + external).
2. For optimum scaling, calculate the max possible value of signal, round up to nearest power of 2, and justify this to the maximum floating point value. So for example, 25 dB corresponds to $10^{(25/20)} = 17.78$. This is rounded up to 32 linear (30.1 dB). This is a programmable value in the device.
3. Then for each data point, calculate signal and convert to floating point.

The conversion back to linear is straight forward, but needs to take into account the justification. For $w = 3$, the formula is $(-1^{\text{float}(15)}) \times \text{float}(11:0) \times 2^{\text{float}(14:12)} \times 2^{\text{J}-4}$, where $J = 2^{\text{ceiling}(\text{gain_range}/20/\text{LOG}_{10}(2))}$ is the justification. The value of 4 comes from the difference is the significant resolution and DDC output resolution.

Table 8-3. Floating Point Format

	MSB															LSB
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$w = 2$	S	E1	E0	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
$w = 3$	S	E2	E1	E0	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

8.3.2.5.4.2 Coarse/Fine Gain Mode

Another DGC Mode is the Coarse/Fine Gain Mode. The gain to be imparted to the signal is split into coarse and fine gains. Coarse step can be 2, 3, 4, 6, or 8 dB. The number of coarse bits is 2, 3, or 4. Fine gain is imparted to the data whereas the coarse index is encoded either through the LSBs of the data or through output GPIO pins. An offset for the fine gain in the range of 0 to 5 dB in 1-dB steps can be programmed, and TI recommends to set the offset to $\text{mod}(6 - (\text{CoarseStep} - 1), 6)$.

8.3.2.5.4.2.1 Coarse Gain Over LSB Encoding

If it is encoded through LSBs of the data, either the LSBs of both I and Q are used to encode the coarse gain, or the coarse gain is encoded completely in both I and Q. For example, if the coarse index is 2 bits either 1 LSB from I and Q are used or alternatively 2 LSBs of both I and Q are used for encoding the coarse gain on both I and Q. Similarly, a coarse index of 4 bits uses 2 LSBs of I and Q. TI recommends that this mode is used only with 16-bit or higher JESD formatting to prevent significant SNR loss due to a higher quantization noise with lower resolution. The modes supported are tabulated below in [Table 8-4](#).

Table 8-4. Modes to Encode Coarse Index on LSBs of I and Q

MODE #	DESCRIPTION
1	2-bit Coarse Index, 1 LSB of I and Q
2	3-bit Coarse Index, 2 LSB of I and Q
3	4-bit Coarse Index, 2 LSBs of I and Q
4	2-bit Coarse Index, 2 LSBs of I (and repeated on Q)
5	3-bit Coarse Index, 3 LSBs of I (and repeated on Q)

When the Coarse Index is transmitted over I and Q, the LSBs of the coarse index are transmitted on I and the MSBs on Q by default. The I and Q LSBs can be swapped or inverted in order.

8.3.2.5.4.2.2 Coarse/Fine Gain Mode With Coarse Index Sent Over Pins

In this mode, the coarse index is sent over pins and hence all 16 bits can be used for data. A maximum of 3 pins are supported. For a 3-pin example, the mapping can be changed from [0 7] to [7 0], which is the equivalent to doing a subtraction from 7.

The output through the pins can be delayed to better match the latency of the fine data through the JESD204B/C interface. The delay is a 12-bit number in units of $f_{\text{ADC}}/8$ clock cycles.

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8.3.2.6 RX Chain Digital Block

The output of the RX ADC goes to the DDC blocks, consisting of a complex mixer followed by decimation block to reduce the sample rate of the output data. The output of the DDC goes to an digital gain compensation (DGC) block to optionally maintain a constant gain from RX analog input to digital output.

8.3.2.6.1 RX Digital Mux

The device supports a mode where the output data of one ADC can be routed internally to the digital blocks of both DDC blocks in each 2 RX on the same side of the device (channels 1RX and 2RX are a group and channels 3RX and 4RX are a group). The unused ADC channel can be powered down. This allows up to 4 DDCs (or 2 DDCs in the wider bandwidth modes) to be used for two ADCs.

8.3.2.6.2 RX Delay Block

A programmable delay can be configured in integer multiples of the ADC clock period up to 31 clocks through 5 register bits. There may be an offset in delay between the 0 delay setting when enabled and when the delay is disabled.

8.3.2.6.3 RX Digital Mixers and NCOs

The digital mixer includes two NCOs in dual DDC mode and 16 NCOs in single DDC mode, whose frequency can be set independently. The mixers can switch between the NCOs and each NCO is able to maintain its phase accumulation at all times. The switch between the NCOs can be controlled through the SPI or dedicated GPIO pins. The NCOs have two options for setting the frequency. First, they can have a 32-bit resolution with the frequency specified as the $N \times \text{sample rate} \times 1/2^{32}$. Optionally, the NCOs can provide an exact 1-kHz raster for an input reference clock frequency of $N \times 61.44 \text{ MHz}$, where N is a integer. The NCOs and mixer provide a SFDR of 100 dB.

8.3.2.6.4 RX Decimation Block

The RX decimation block decimates the ADC data to the output sample rate. The decimation block is highly flexible, matching the interface rates to the possible ADC sample rates. Boxes with a number are valid modes, boxes without a number are not valid modes. The rates are listed in [Table 8-5](#). The non-grey boxes have 2 DDCs, while the grey boxes have 1 DDC only. Above 750MSPS, the feedback paths are not available to be used in parallel with the receiver paths.

Table 8-5. RX Decimation Rates

		Feedback Available?	ADC SAMPLE RATE (MSPS)					
			1250	1500	2000	2250	2500	3000
Output Rate (MSPS)	62.5	Yes	20	24	32		40	48
	93.75	Yes		16		24		32
	125	Yes	10	12	16		20	24
	187.5	Yes		8		12		16
	250	Yes	5	6	8		10	12
	375	Yes		4		6		8
	500	Yes			4		5	6
	750	Yes						4
	1000	No			2		2.5	3
	1500	No						2

The digital decimation filters provide over 85 dB (90 dB for the final 2x decimation) of image rejection of the in-band signal. Passband is defined as 81.4% of the baseband sample rate and in-band peak-to-peak ripple is less than 0.2 dB. The decimation filter responses for decimation from 3000 MSPS are shown in [Figure 8-11](#) through [Figure 8-38](#).

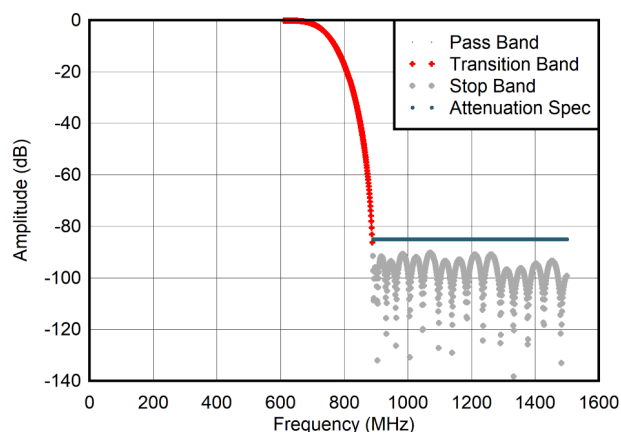


Figure 8-11. RX Filter Response for Decimation by 2 (Nyquist)

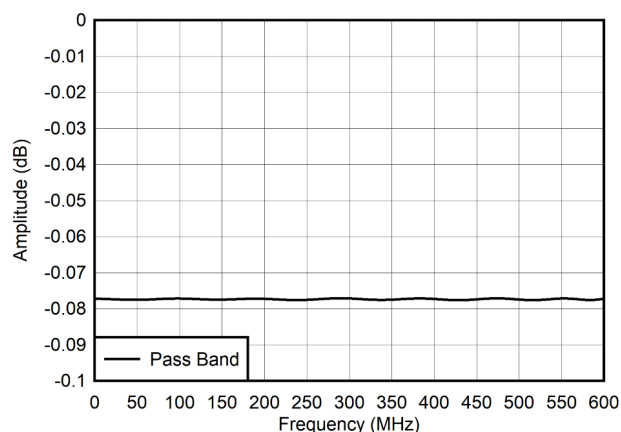


Figure 8-12. RX Filter Response for Decimation by 2 (Passband)

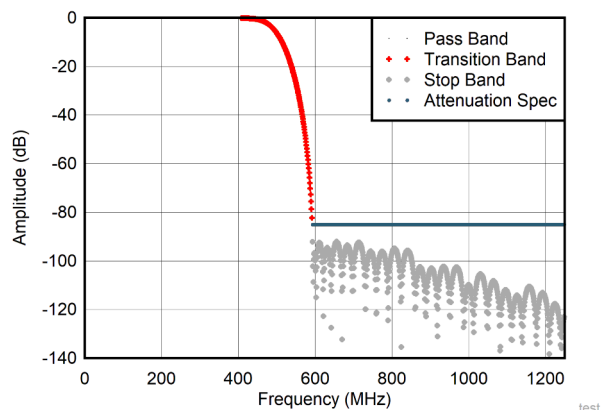


Figure 8-13. RX Filter Response for Decimation by 2.5 (Nyquist)

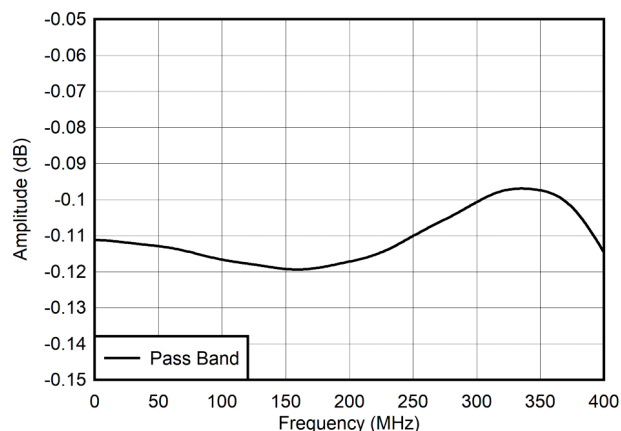


Figure 8-14. RX Filter Response for Decimation by 2.5 (Passband)

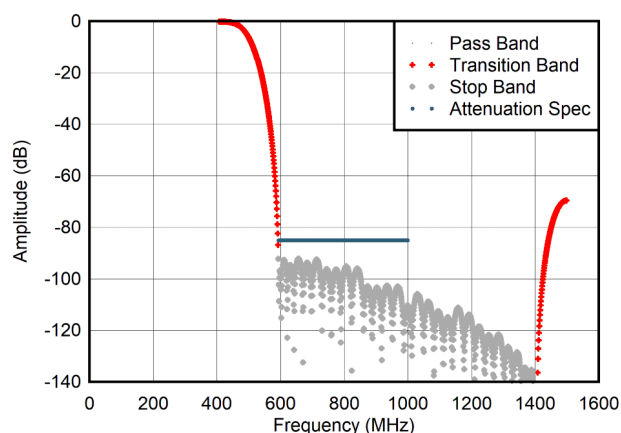


Figure 8-15. RX Filter Response for Decimation by 3 (Nyquist)

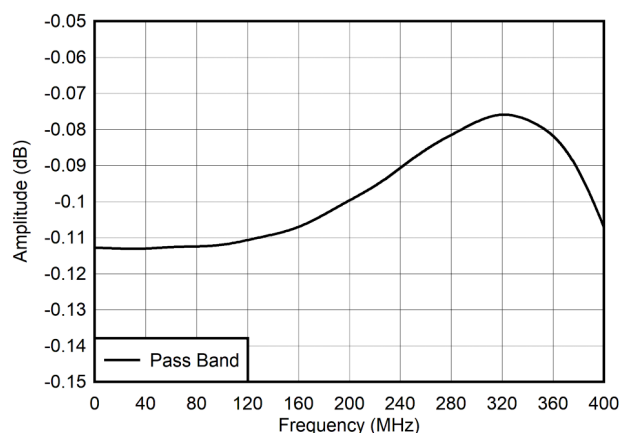


Figure 8-16. RX Filter Response for Decimation by 3 (Passband)

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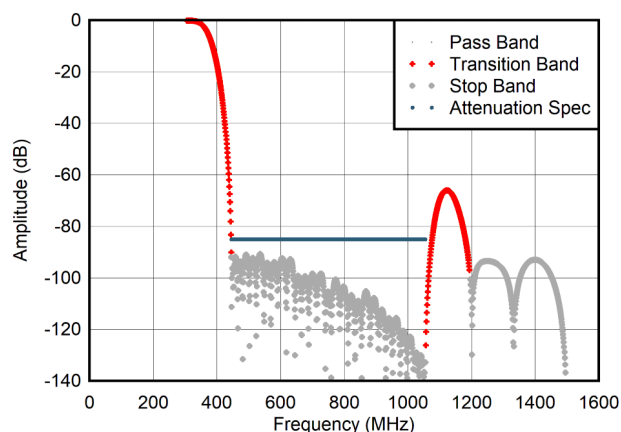


Figure 8-17. RX Filter Response for Decimation by 4 (Nyquist)

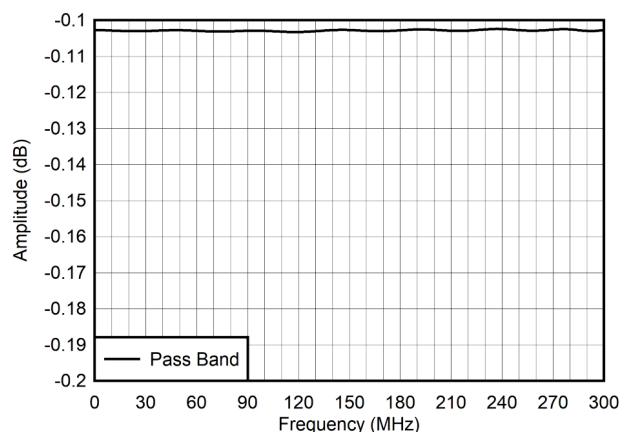


Figure 8-18. RX Filter Response for Decimation by 4 (Passband)

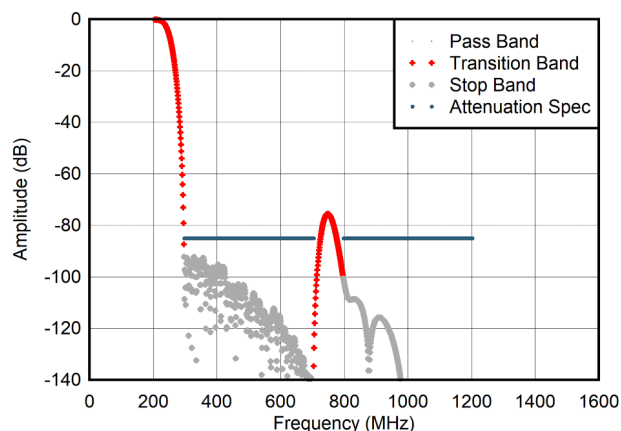


Figure 8-19. RX Filter Response for Decimation by 6 (Nyquist)

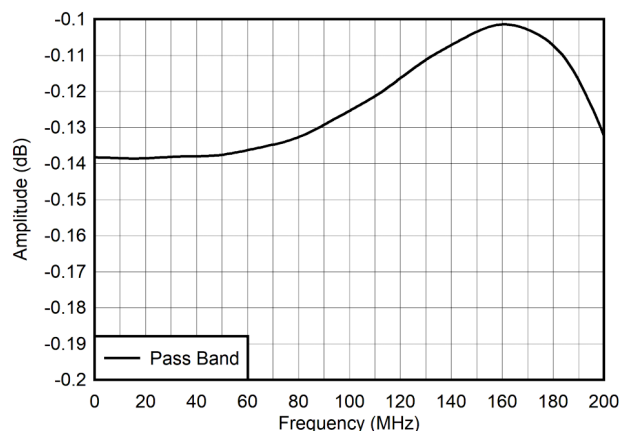


Figure 8-20. RX Filter Response for Decimation by 6 (Passband)

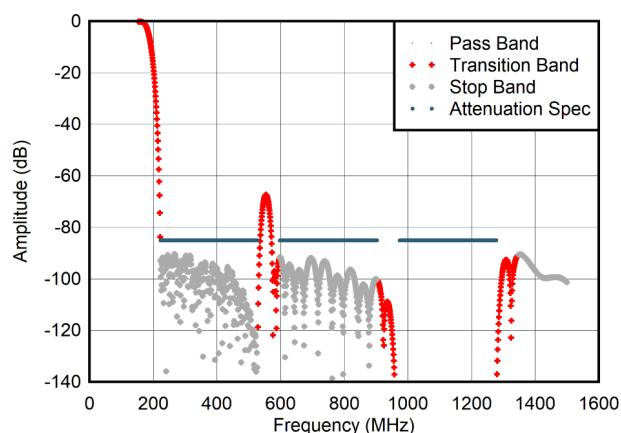


Figure 8-21. RX Filter Response for Decimation by 8 (Nyquist)

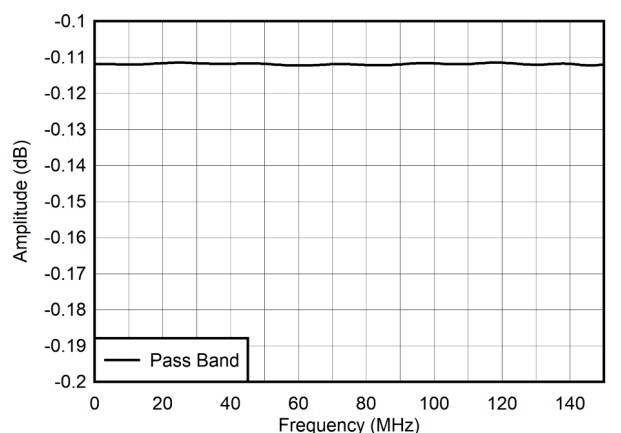


Figure 8-22. RX Filter Response for Decimation by 8 (Passband)

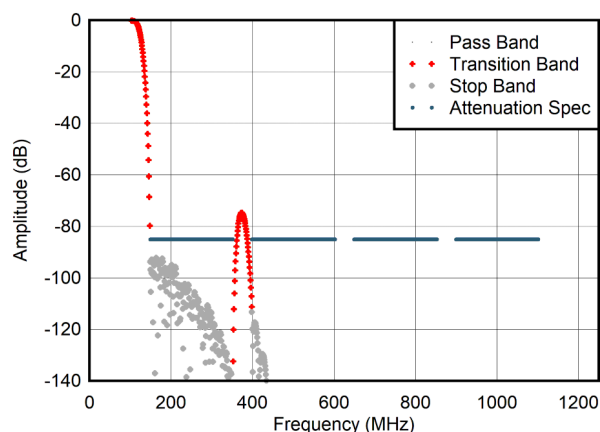


Figure 8-23. RX Filter Response for Decimation by 10 (Nyquist)

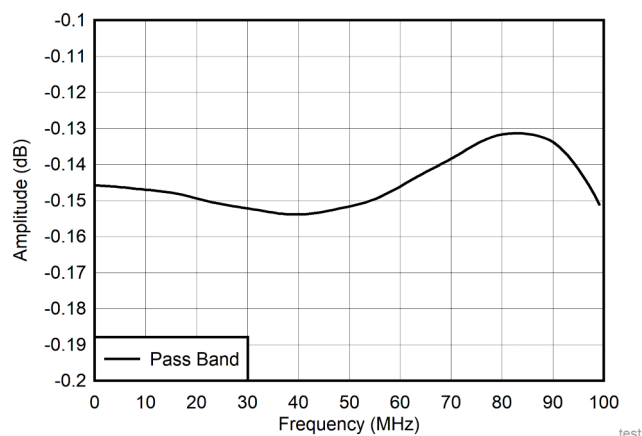


Figure 8-24. RX Filter Response for Decimation by 10 (Passband)

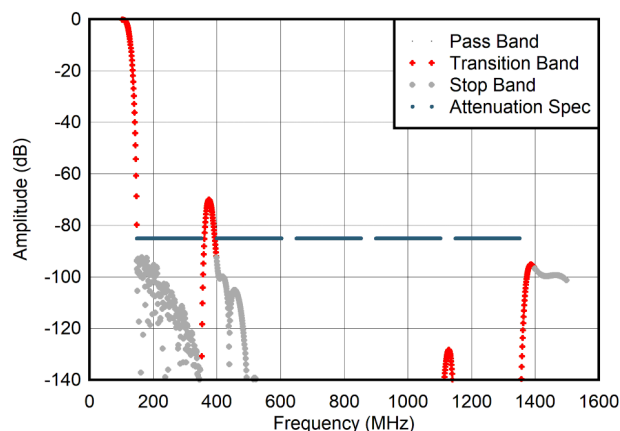


Figure 8-25. RX Filter Response for Decimation by 12 (Nyquist)

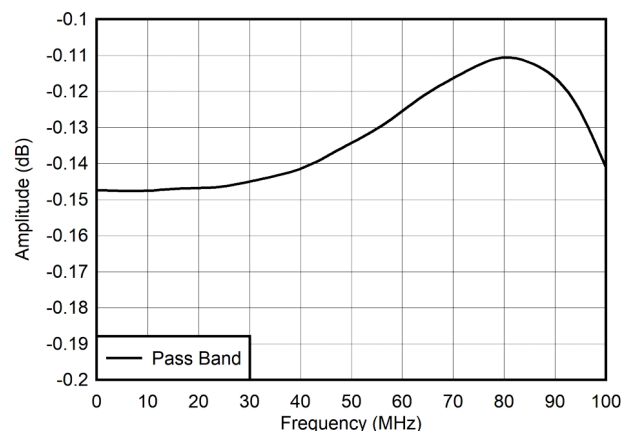


Figure 8-26. RX Filter Response for Decimation by 12 (Passband)

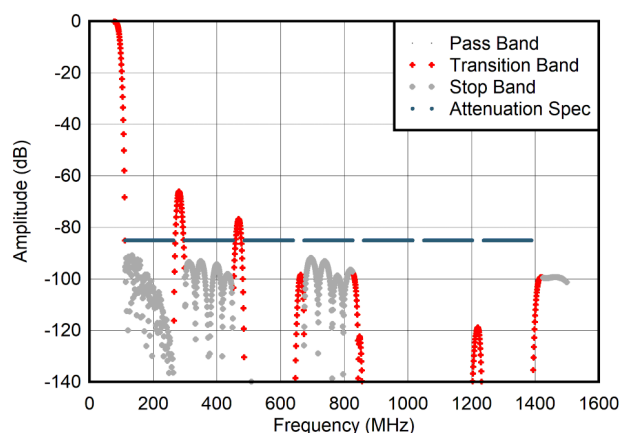


Figure 8-27. RX Filter Response for Decimation by 16 (Nyquist)

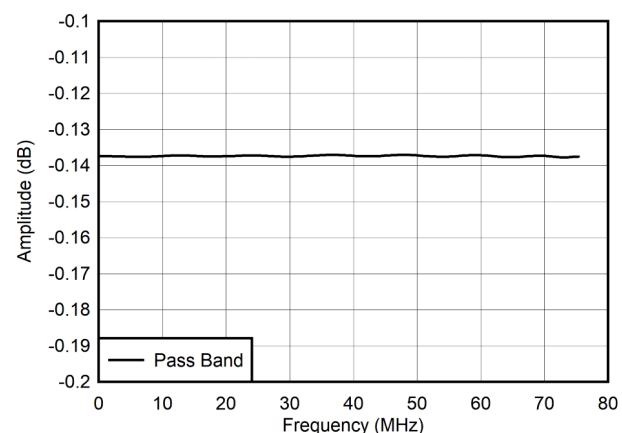


Figure 8-28. RX Filter Response for Decimation by 16 (Passband)

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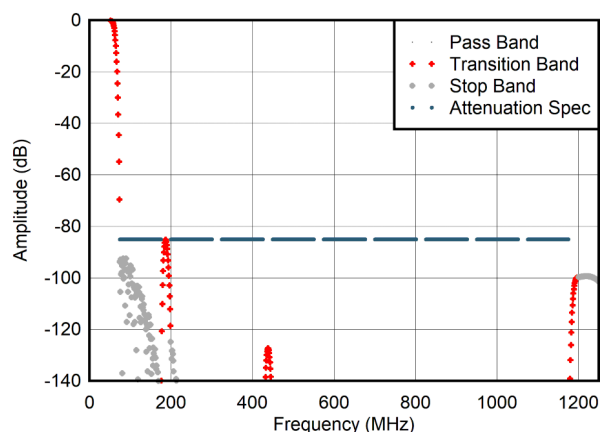


Figure 8-29. RX Filter Response for Decimation by 20 (Nyquist)

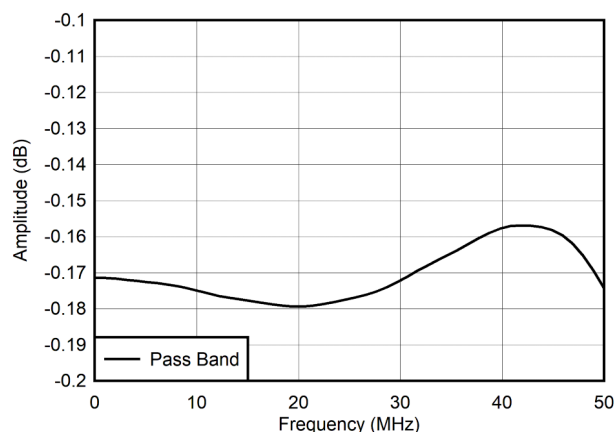


Figure 8-30. RX Filter Response for Decimation by 20 (Passband)

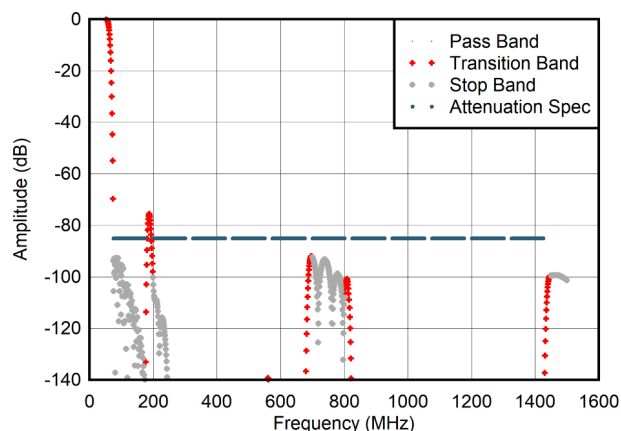


Figure 8-31. RX Filter Response for Decimation by 24 (Nyquist)

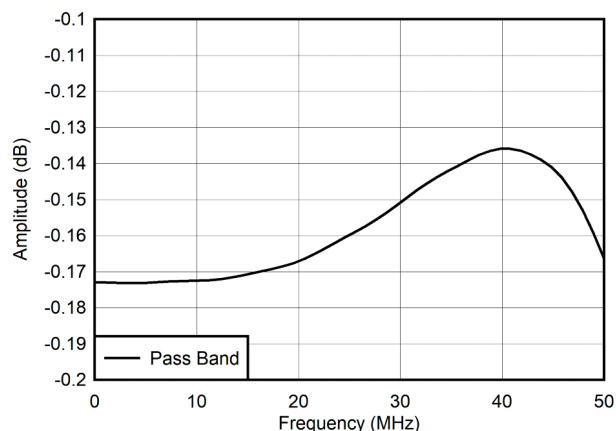


Figure 8-32. RX Filter Response for Decimation by 24 (Passband)

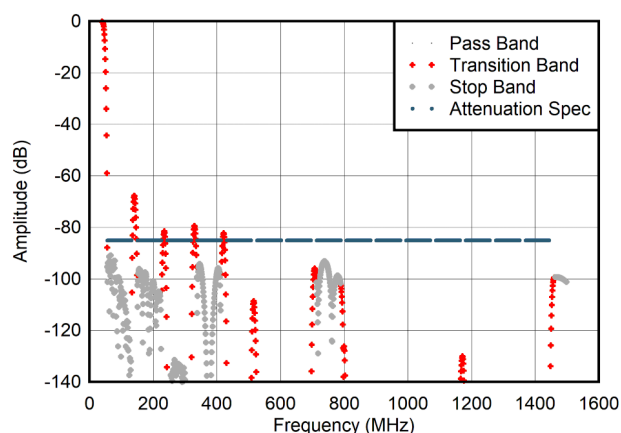


Figure 8-33. RX Filter Response for Decimation by 32 (Nyquist)

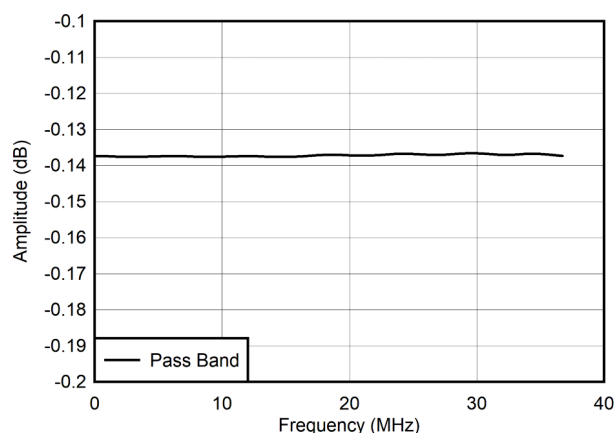
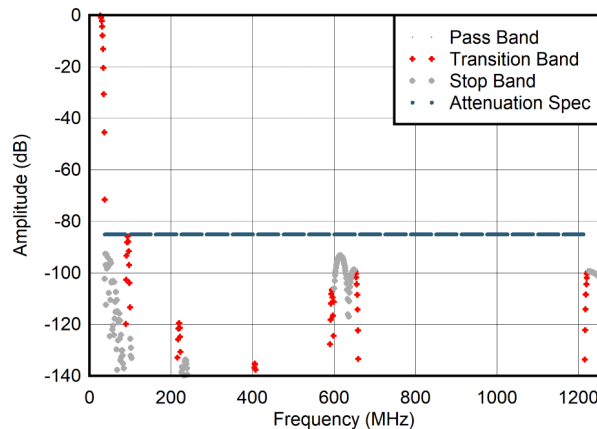
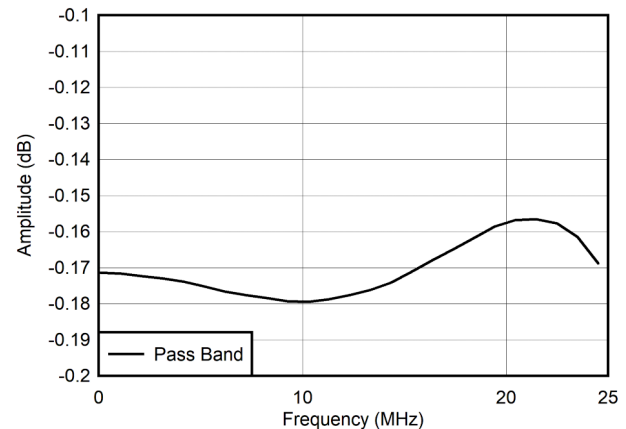
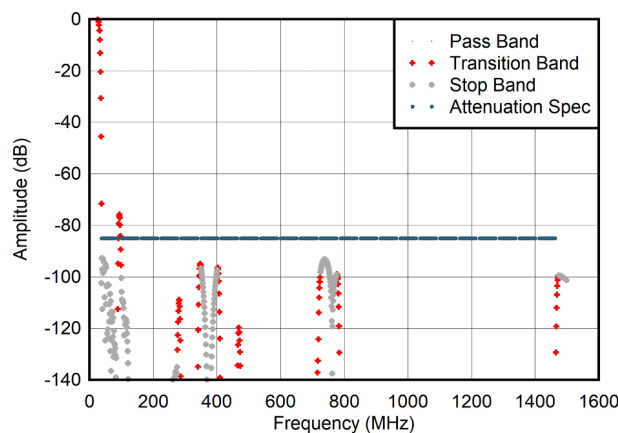
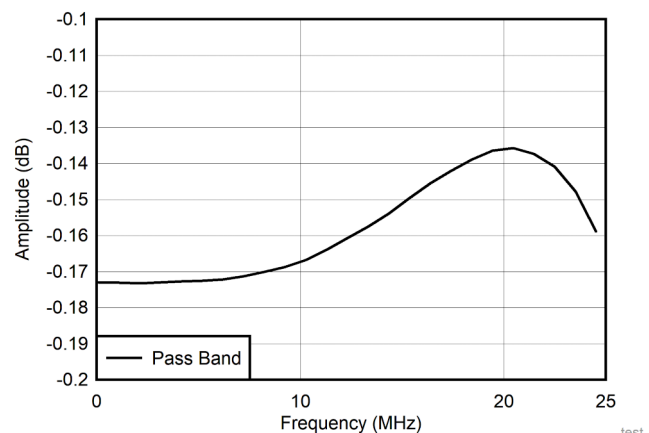
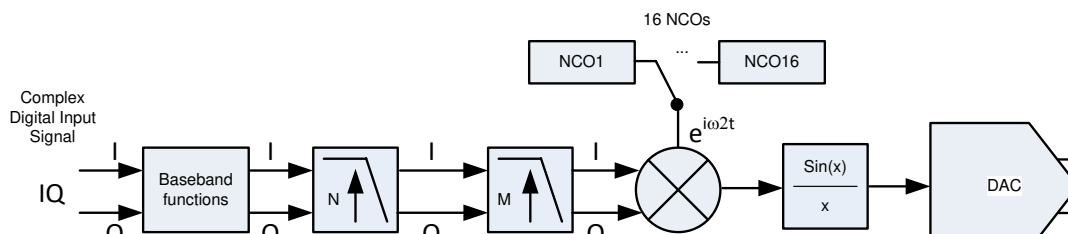


Figure 8-34. RX Filter Response for Decimation by 32 (Passband)


Figure 8-35. RX Filter Response for Decimation by 40 (Nyquist)

Figure 8-36. RX Filter Response for Decimation by 40 (Passband)

Figure 8-37. RX Filter Response for Decimation by 48 (Nyquist)

Figure 8-38. RX Filter Response for Decimation by 48 (Passband)

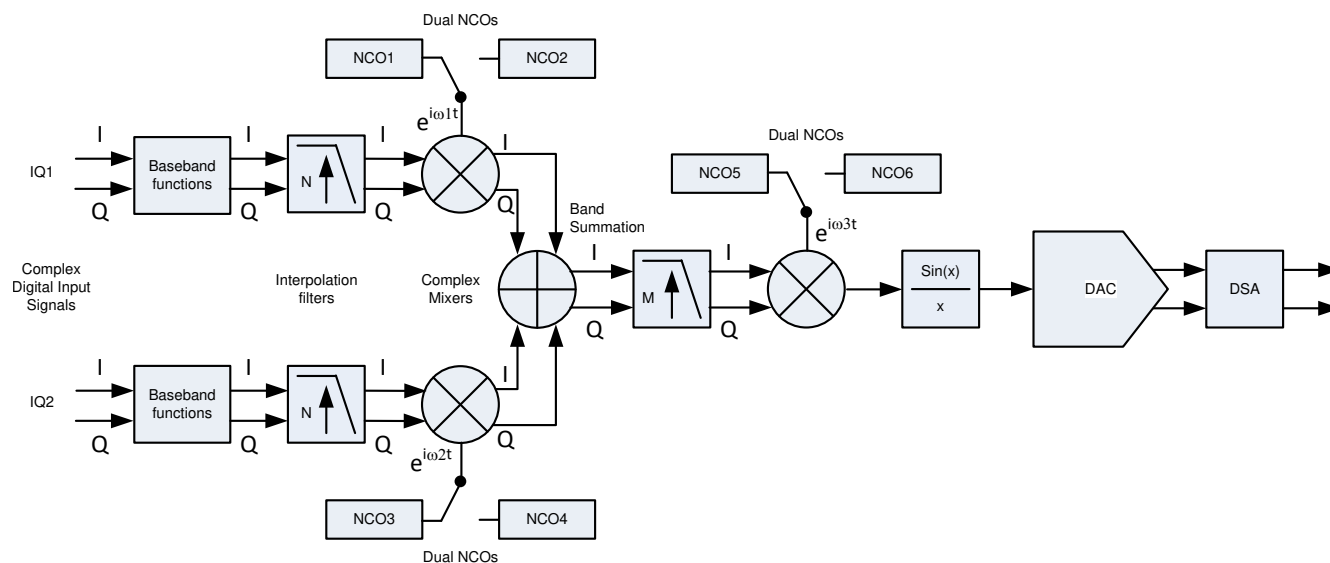
8.3.3 Transmitter (TX) Chain

The AFE7900 integrates 4 transmitters based on RF sampling DACs. The TX chain block diagrams are shown in [Figure 8-39](#) for a single DUC and [Figure 8-40](#) for dual DUC mode. The DAC output operates up to 12 GSPS and is followed by a wideband RF amplifier (TX DSA). The digital section of the TX includes dual or single DUCs to increase the input sample rate to the DAC sample rate. The digital block also include gain control and a PA protection block.


Figure 8-39. TX Chain Block Diagram With Single DUC

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**Figure 8-40. TX Chain Block Diagram With Dual DUCs****8.3.3.1 TX Chain Digital Block**

The input to the TX chain is one or two complex signals from the JESD block. At the input sample rate are baseband functions and a signal measurement circuit for the PA protection block. This is followed by the digital upconverter and the $\text{Sin}(x)/x$ filter.

8.3.3.1.1 Baseband Processing Functions

The baseband processor provides the following functions:

- Digital Gain
- TX DSA Gain and Phase Correction
- TX Frequency Response Correction
- TX Power Meter

8.3.3.1.1.1 Digital Gain

The digital gain block has a range of [+3 to -20 dB] in steps of 0.125 dB (a setting of 0 corresponds to maximum gain). A value of 24 corresponds to 0dB gain, i.e. a full scale input signal being fullscale at the DAC. When combined with an analog (DSA) gain change, the analog setting should be written first and then the digital gain setting so both will be simultaneously updated without a glitch.

The digital gain can also be programmed separately through a different register.

8.3.3.1.1.2 TX DSA Gain and Phase Correction

The TX DSA gain and phase correction block is used to reduce the error in gain and phase for each DSA setting. This is expected to be calibrated in the customer factory or at start-up through the DSA calibration macro.

8.3.3.1.1.3 TX Frequency Response Correction

The TX has a correction filter that can provide a gain slope as a function of frequency to correct the DAC output frequency response across the band.

8.3.3.1.1.4 TX Power Meter

There are RMS power meters at each of the IQ input streams. The power meter measures the RMS power in a programmable window of samples 2^n samples, with $n = [5, 16]$. The power meter is accurate to 0.3 dB for signal levels between 0 and -40 dBFS. The power meter is read through the SPI interface.

8.3.3.1.2 TX PA Protection

The AFE7900 incorporates an optional power amplifier protection (PAP) block to monitor when the input signal is too large (like when an interface error occurs and reduces the digital signal power for the DAC, for example).

The PAP block achieves the functionality of reducing the input signal that crosses the threshold through three main sub-blocks. These are PAP detectors, a PAP gain state machine, and a PAP gain module. The locations of the PAP blocks in the TX digital signal chain are shown in Figure 8-41. One PAP state machine is dedicated for each TX1, TX2, TX3, and TX4 chains.

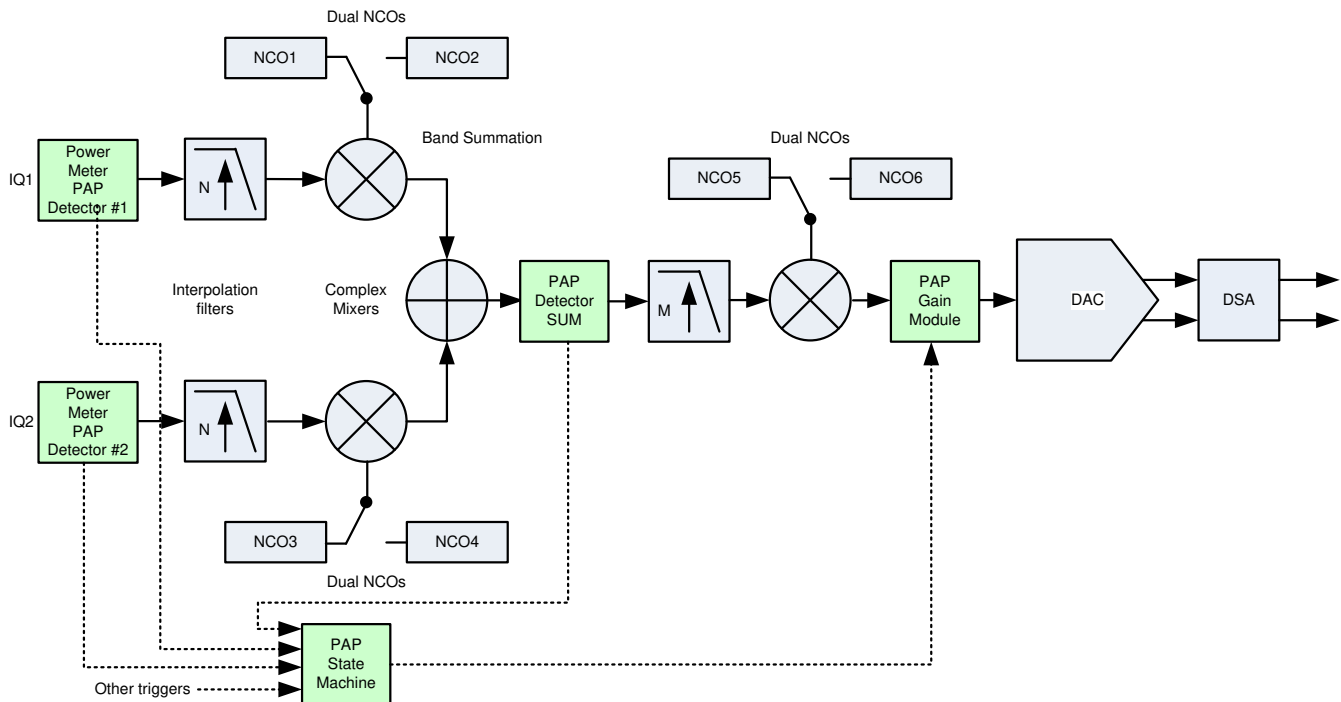


Figure 8-41. PAP Blocks in the TX Signal Chain

8.3.3.1.2.1 PAP Triggers

The PAP protection state machine can be triggered by alarms from the SerDes and JESD blocks, PLLs, power measurements on the TX signal, PAP triggers from other TX chains, TX over range signal, or a SPI register (see Figure 8-42). Each trigger can be enabled separately.

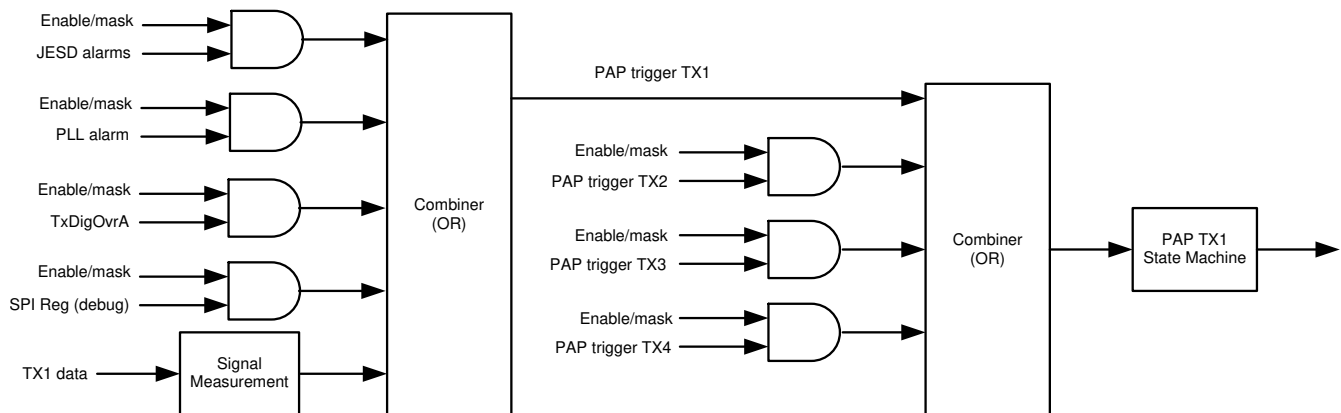


Figure 8-42. PAP Triggers for TX1

8.3.3.1.2.1.1 SerDes and JESD Triggers

The SerDes and JESD blocks have four different type of alarms, of which some are per lane and some others are common for all the lanes:

- FIFO errors – 1 per lane.
- Loss of Signal (LOS) errors – 1 per lane.

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- Link errors – 1 per lane.
- SerDes PLL unlock error – common for all lanes.

Based on the JESD LMFS configuration, an error on a lane will require the corresponding TX chains to be shut down. For example, if 8 lanes are supporting 4 IQ TX chains, then even if only lane 1 (for TX1_I) has an error, both lane 1 and 2 (TX1_I and TX2_Q) will need alarms. So depending on the LMFS configuration, the JESD alarm to TX1 needs to be configured for example as:

- Lane1 error OR Lane2 error OR SerDes PLL error = TX1 JESD alarm
- Lane3 error OR Lane4 error OR SerDes PLL error = TX2 JESD alarm
- Lane5 error OR Lane6 error OR SerDes PLL error □ TX3 JESD alarm
- Lane7 error OR Lane8 error OR SerDes PLL error □ TX4 JESD alarm

Lane 1 error itself is the OR of all the per lane errors like FIFO error, LOS error and Link error. If 4 lanes support 4 IQ TX chains, then

- Lane1 error OR SerDes PLL error = TX1 JESD alarm
- Lane2 error OR SerDes PLL error = TX2 JESD alarm
- Lane3 error OR SerDes PLL error = TX3 JESD alarm
- Lane4 error OR SerDes PLL error = TX4 JESD alarm.

8.3.3.1.2.2 PLL Alarm Trigger

The unlock alarm from the device clock PLL is available to trigger the PAP state machine.

8.3.3.1.2.3 Average Power Trigger

The average power-based protection is based on power measurement in a moving window, and the module is dedicated for each TX chain. The window length is programmable to 32, 64, 96, or 128 samples. The average power measurement computes the envelop of the signal by taking abs of the complex signal I + jQ followed by average power measurement as shown in [Figure 8-43](#).

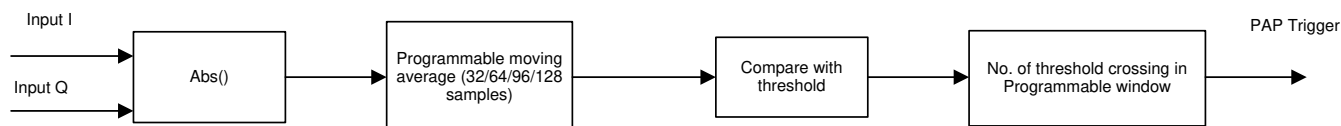


Figure 8-43. Average Power Based PA Protection on Abs of the Input Signal

The programmable window length and the threshold are both programmable in the range 1 to $2^{12} - 1$.

8.3.3.1.2.4 High Pass Filter Trigger

The high pass filter (HPF) based PA protection trigger provides another option in determining abnormal signals in the TX chain. The HPF taps are $[-1 \ 1 \ 6 \ -6 \ -1 \ 1]/16$ and the frequency response across the Nyquist zone is shown in [Figure 8-44](#).

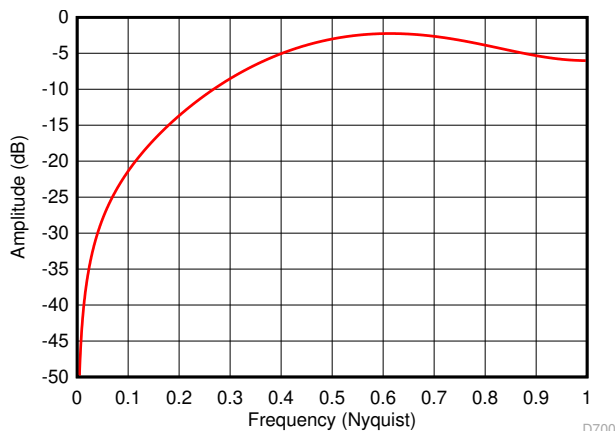


Figure 8-44. HPF Frequency Response

This HPF trigger has one detection mode:

- High pass filter on $\text{abs}(I+jQ)$ and output is used to determine threshold crossing.

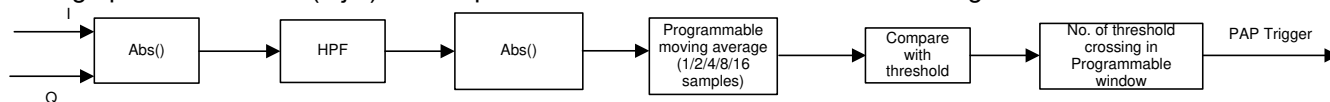


Figure 8-45. Programmable Filter Detector – Mode 3

The moving average power is compared with a threshold and the number of crossings in a programmable time window is computed. The time window is programmable from $1 - 2^4$ samples. If the number of crossings is higher than a threshold number of crossing then the PAP is triggered. The programmable window of length: $1 - 2^{12} - 1$ samples and the threshold is also 1 to $2^{12} - 1$.

8.3.3.1.2.5 PAP Gain State Machine

In a trigger event, the digital signal is scaled down before the DAC so that the abnormal samples do not reach the PA. The ramp down signal is multiplied to signal data path at the output of the interpolation filter. The PAP state machine is shown in [Figure 8-46](#):

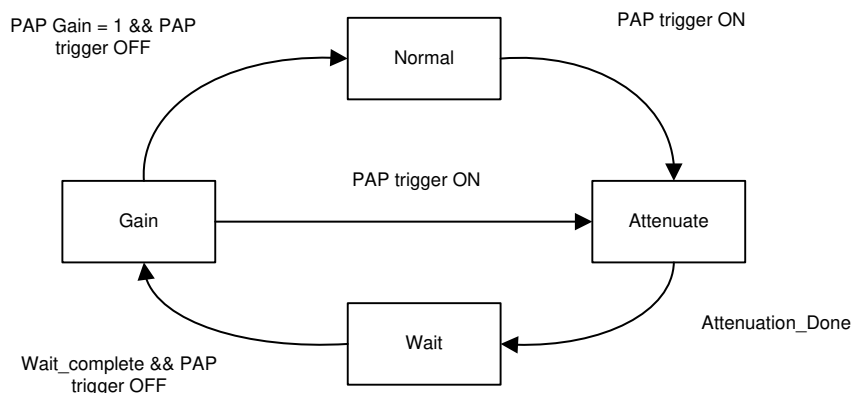


Figure 8-46. PAP State Machine

Once the PAP trigger ON is generated, the state machine moves to “Attenuate” state, where the attenuation of the signal is started. In the “Attenuate” state, the ramp down of the signal is done in one of two programmable modes:

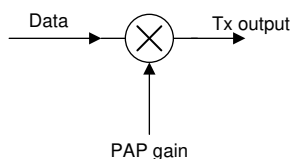
- Linear ramp down: The start gain, gain step and time duration in a particular gain step for ramp down are all programmable.
- Cosine Ramp down: Attenuation of the form $(1 + \cos\theta)/2$ with θ going from 0 to π . The starting phase and time duration in a particular phase value are all programmable.

In addition to the ramp down, there are three programmable modes in the datapath:

- Regular Operation of Datapath: The signal datapath is working in the normal mode and is multiplied by the ramp down signal. In this mode, the PA protection is achieved by ramp down as even the offending sample with attenuation is passed to the PA.
- Holding the last good sample: The signal datapath holds the sample value at the interpolator filter the time instant at which the PA protection trigger occurs. The offending sample does not pass through the data chain. The PA protection trigger to the PAP state machine can be delayed to ensure the last good sample before the offending sample is held. The held datapath output is then multiplied by the ramp down. Once the ramp down signal reaches the end gain (or phase value) a Done signal is generated by the ramp down module. This Done signal is used to remove the holding of the samples. After the Done signal, the regular datapath operation begins though the output of the datapath is multiplied by the ramp down signal.
- Programmable Value to datapath: Instead of holding the last good sample, a programmable value in I and Q is forced into the datapath once the PAP state machine is triggered. The forcing of the programmable value to the datapath is removed once the Done signal is generated by the ramp down module. After the Done signal, the regular datapath operation begins though the output of the datapath is multiplied by the ramp down signal.

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**Figure 8-47. Multiplication of Signal Datapath to Ramp Down Signal**

After attenuation is done, the PAP state machine moves into the Wait state, before checking the status of the PAP trigger. A programmable 16-bit counter is used in the Wait state.

After the wait time ends, the state machine moves to gain state only if the PAP trigger is OFF. If the PAP trigger is ON then the state machine continues to remain in Wait state. If the PAP trigger becomes OFF then the state machine moves to Gain state. The signal measurement PAP triggers (Average Power and Programmable Filter Triggers) continuously monitor the incoming signal and become OFF when the measurements does not exceed the threshold anymore. All other PAP triggers require the intervention of the Host to perform the necessary steps to remove the source of the error and then clear the Triggers.

Once again in the Gain state, the signal is multiplied by the ramp-up signal. The ramp-up is generated by the two modes:

- Linear ramp-up: Programmable ramp-up end and step. The end, step and time duration for the ramp-up are all different from the ramp-down values.
- Cosine ramp-up: the end phase and phase step are programmable and different from the cosine ramp down values.

If a PAP ON trigger occurs during the Gain state ramp-up then the state machine moves to Attenuate state. The starting gain in the Attenuate state is equal to the value at which the Gain state stopped.

8.3.3.2 Interpolation Block

The TX interpolation block interpolates the input data to the DAC sample rate and up converts the signals to the chosen frequencies. The interpolation block is highly flexible, matching the interface rates to the possible DAC sample rates. The rates are listed in the tables below. Boxes with a number are valid modes, boxes without a number are not valid modes. The non-grey boxes have the option for two DUCs, while the grey boxes have 1 DUC available. The digital up-conversion is implemented with a two-stage architecture: front stage (interpolate by N in [Figure 8-41](#)) and back stage (interpolate by M in [Figure 8-41](#)). The front mixer stage sets the I/Q streams to the desired frequency spacing, after which the I/Q streams are summed together in the band summation block. The interpolation FIRs are also split into the front-FIR stage and back-FIR stage.

The output data rate after the multi-band summation block is also listed in [Table 8-6](#). The resulted multi-band signal is further interpolated and up-converted to the desired output RF frequency.

Table 8-6. Interpolation Factors Between Input and DAC Sample Rates

		DAC SAMPLE RATE (MSPS)							
		4500	5000	6000	7500	8000	9000	10000	12000
Input Rate (MSPS)	125	36	40	48	60	64	72	80	96
	187.5	24		32	40		48		64
	250	18	20	24	30	32	36	40	48
	375	12		16	20		24		32
	500	9	10	12	15	16	18	20	24
	750	6		8	10		12		16
	1000	4.5		6	7.5	8	9	10	12
	1500	3		4			6		8
	2000 (2TX only)			3		4			6
	3000 (2TX only)						3		4
Dual DUC Combining Rates (MSPS)	Half Rate	1105.92	1250	1500	1250	1000	1500	1250	1500
	Full Rate	2211.84	2500	3000	2500	2000	3000	2500	3000

Table 8-6. Interpolation Factors Between Input and DAC Sample Rates (continued)

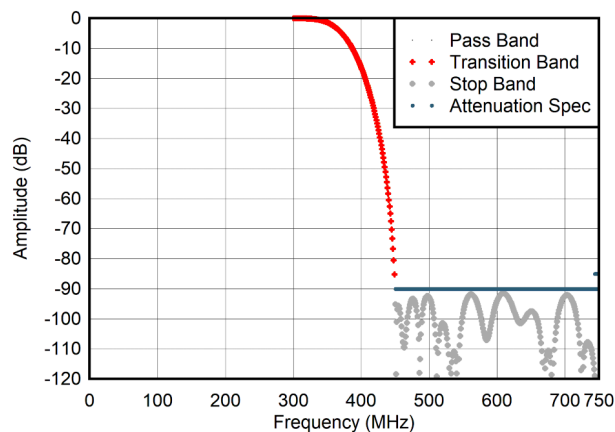
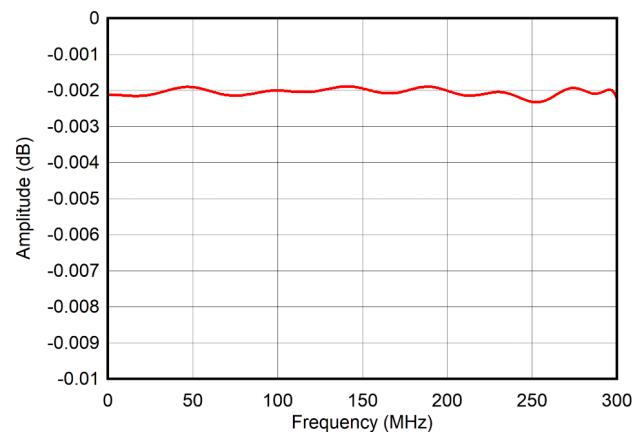
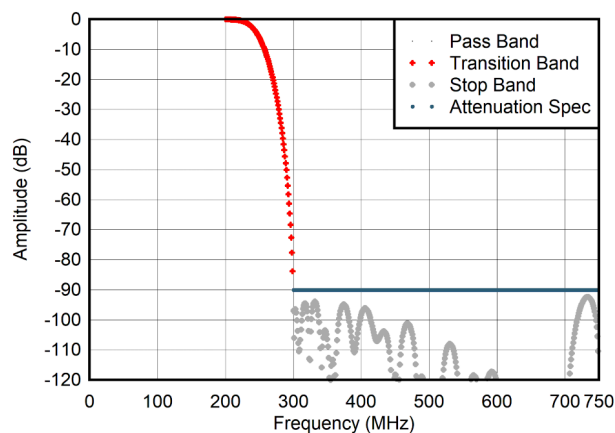
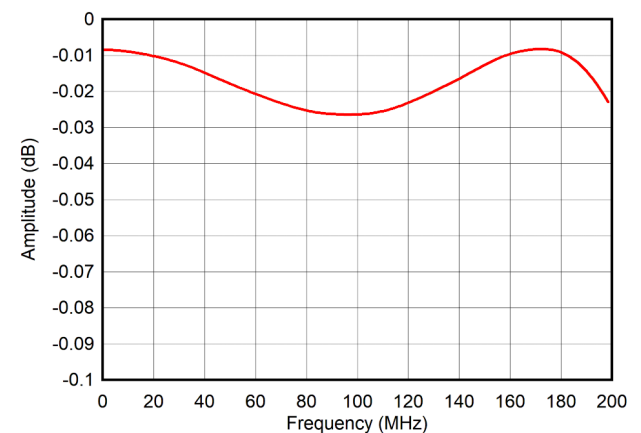
		DAC SAMPLE RATE (MSPS)							
		4500	5000	6000	7500	8000	9000	10000	12000
M (2nd Stage) Interpolation	Half Rate	4	4	4	6	8	6	8	8
	Full Rate	2	2	2	3	4	3	4	4

8.3.3.3 Front Stage Interpolation Block

The front stage digital interpolation filters provide over 90 dB of image rejection of the in-band signal. Passband is defined as 80% of the baseband sample rate and in-band peak-to-peak ripple is for common interpolation factors below 0.1 dB, and is always better than 0.2 dB.

For signals with lower amplitudes at the edge of the passband (like with digital pre-distortion, for example), the bandwidth can also be extended.

The front stage interpolation filter responses are shown in [Figure 8-48](#) through [Figure 8-65](#). Interpolation by 2, 3, 4, 6, 8, and 12 are shown for half rate DUC combining mode at 1500 MSPS. The same responses for interpolation by 4, 6, 8, and 12 are valid for full rate DUC combining mode at 3000 MSPS by multiplying the x-axis by 2. Interpolation by 5, 10 are shown for half rate DUC combining mode at 1250 MSPS. The same responses are valid for full rate DUC combining mode at 2500 MSPS by simply multiplying the x-axis by 2. Interpolation by 20 is shown for the full rate DUC combining mode at 2500 MSPS as this is the only valid mode.

**Figure 8-48. TX Front Stage Filter Response for Interpolate by 2 (Nyquist)****Figure 8-49. TX Front Stage Filter Response for Interpolate by 2 (Passband)****Figure 8-50. TX Front Stage Filter Response for Interpolate by 3 (Nyquist)****Figure 8-51. TX Front Stage Filter Response for Interpolate by 3 (Passband)**

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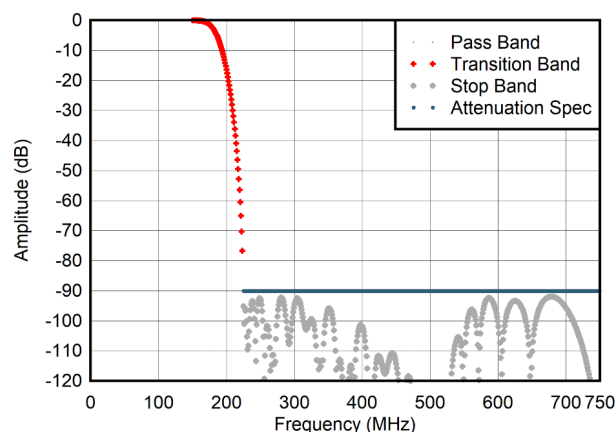


Figure 8-52. TX Front Stage Filter Response for Interpolate by 4 (Nyquist)

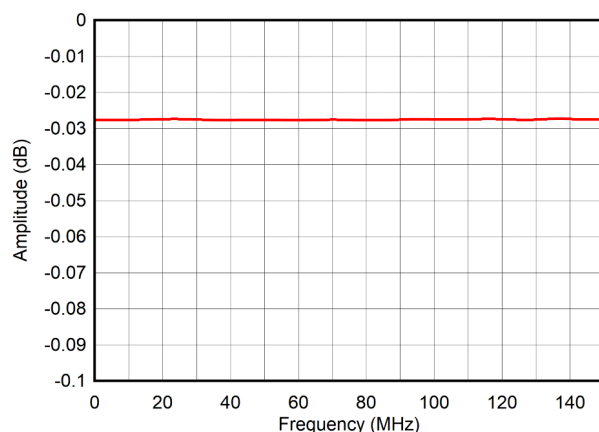


Figure 8-53. TX Front Stage Filter Response for Interpolate by 4 (Passband)

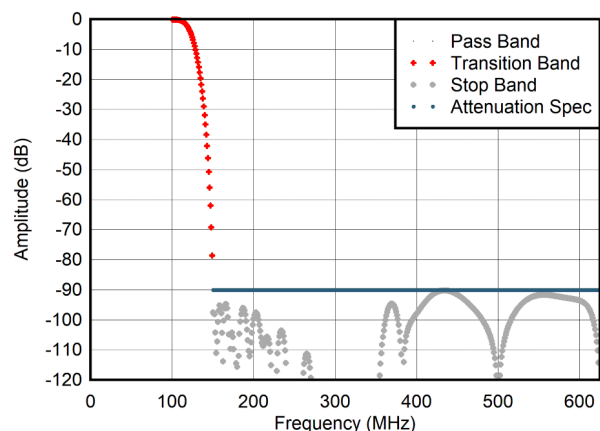


Figure 8-54. TX Front Stage Filter Response for Interpolate by 5 (Nyquist)

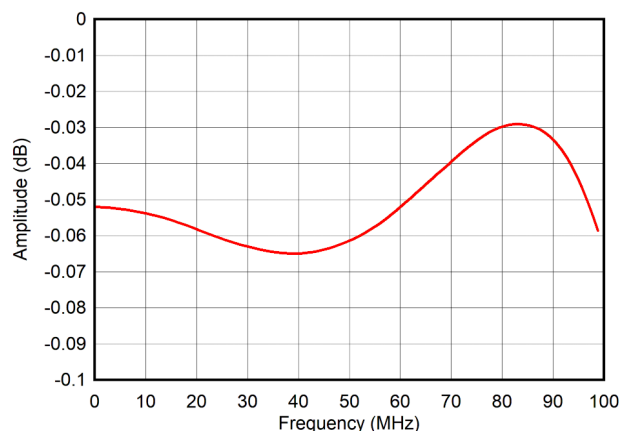


Figure 8-55. TX Front Stage Filter Response for Interpolate by 5 (Passband)

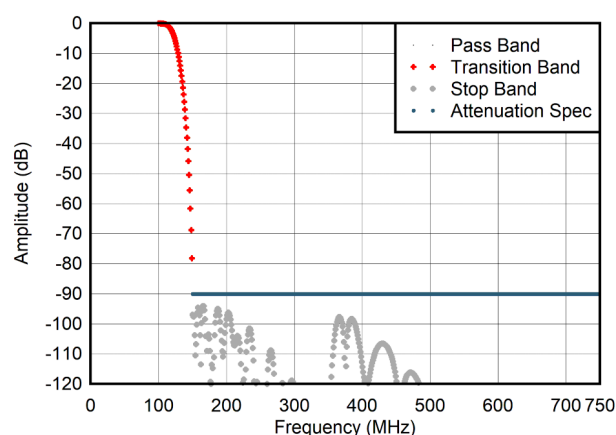


Figure 8-56. TX Front Stage Filter Response for Interpolate by 6 (Nyquist)

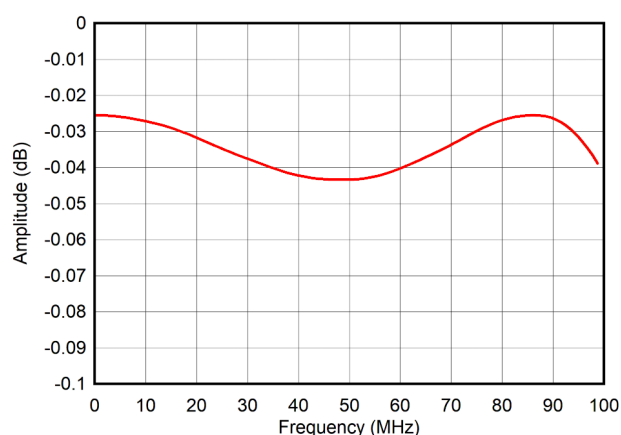


Figure 8-57. TX Front Stage Filter Response for Interpolate by 6 (Passband)

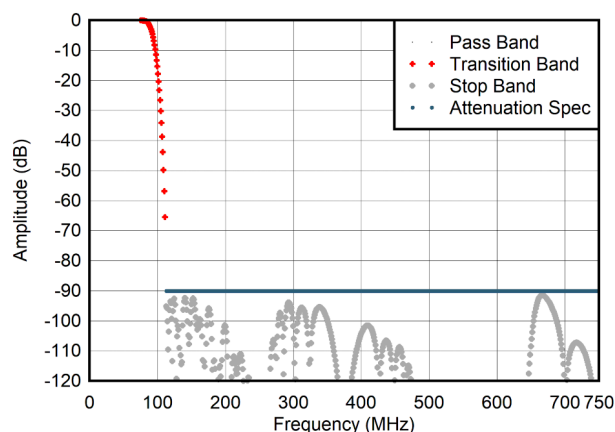


Figure 8-58. TX Front Stage Filter Response for Interpolate by 8 (Nyquist)

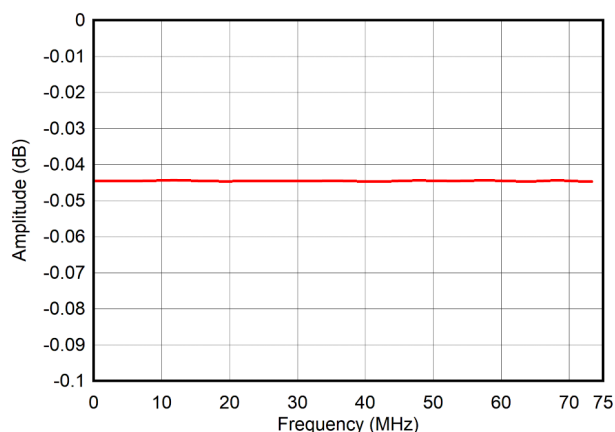


Figure 8-59. TX Front Stage Filter Response for Interpolate by 8 (Passband)

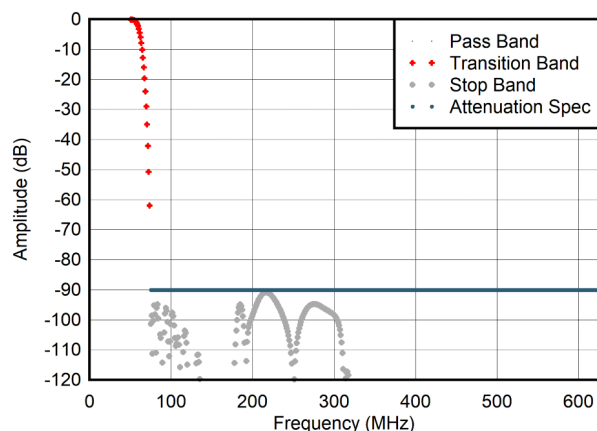


Figure 8-60. TX Front Stage Filter Response for Interpolate by 10 (Nyquist)

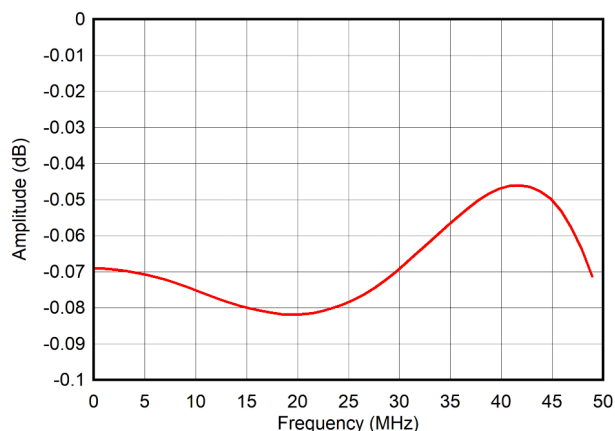


Figure 8-61. TX Front Stage Filter Response for Interpolate by 10 (Passband)

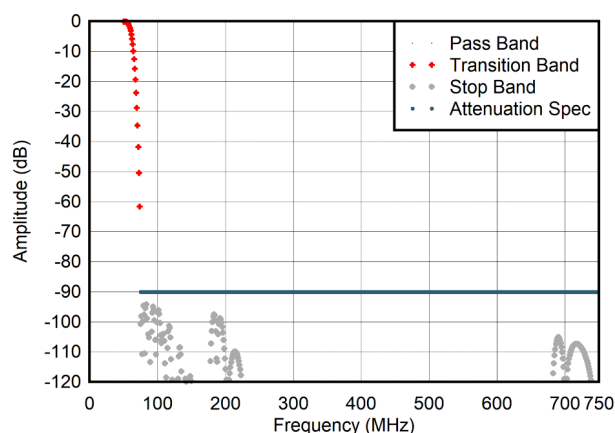


Figure 8-62. TX Front Stage Filter Response for Interpolate by 12 (Nyquist)

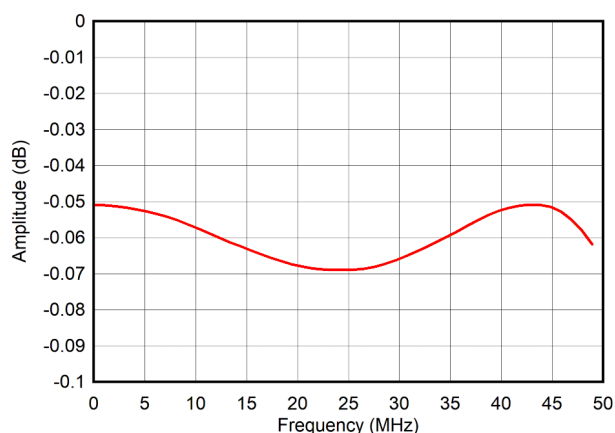


Figure 8-63. TX Front Stage Filter Response for Interpolate by 12 (Passband)

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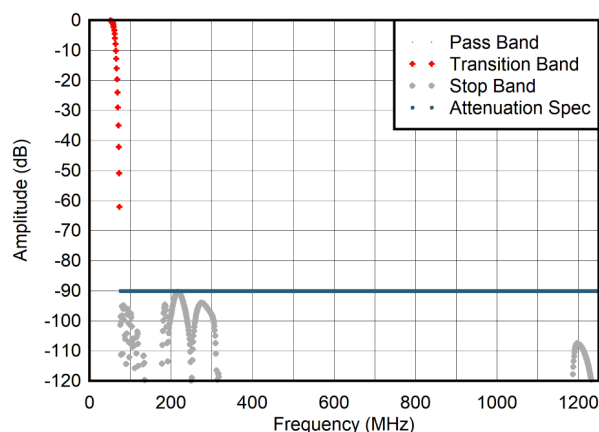


Figure 8-64. TX Front Stage Filter Response for Interpolate by 20 (Nyquist)

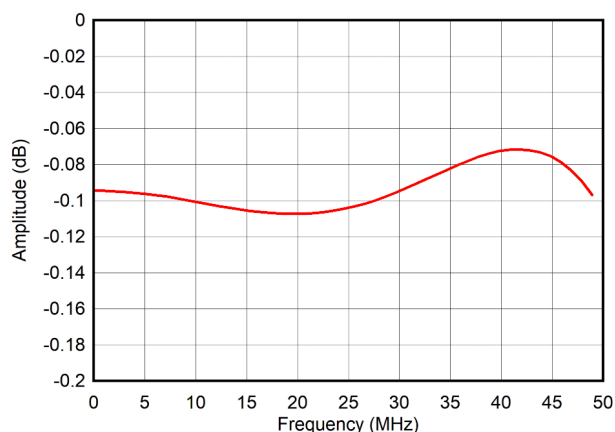


Figure 8-65. TX Front Stage Filter Response for Interpolate by 20 (Passband)

8.3.3.4 Back Stage Interpolation Block

The back stage digital interpolation filters provide over 90 dB of image rejection of the in-band signal. Passband is defined as 80% of the baseband sample rate and in-band peak-to-peak ripple is for common interpolation factors below 0.1 dB, and is always better than 0.2 dB.

For signals with lower amplitudes at the edge of the passband (like with digital pre-distortion, for example), the bandwidth can also be extended.

The back stage interpolation filter responses are shown in Figure 8-66 through Figure 8-75. Interpolation by 2 and 3 are shown for full rate DUC combining mode with an input rate of 3000 MSPS. Interpolation by 4 is shown for are shown for half rate DUC combining mode with an input rate of 1500 MSPS. The interpolation by 4 response is also value for full rate DUC combining mode with an input rate of 3000 MSPS by multiplying the x-axis by 2. The interpolation by 6 and 8 responses are shown for a half rate DUC combining mode of 1500 MSPS.

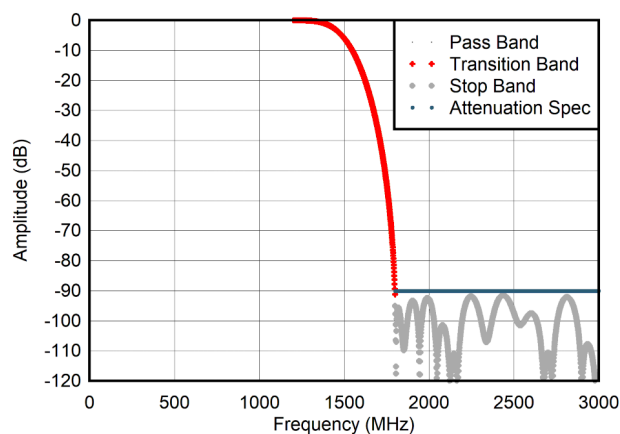


Figure 8-66. TX Back Stage Filter Response for Interpolate by 2 (Nyquist)

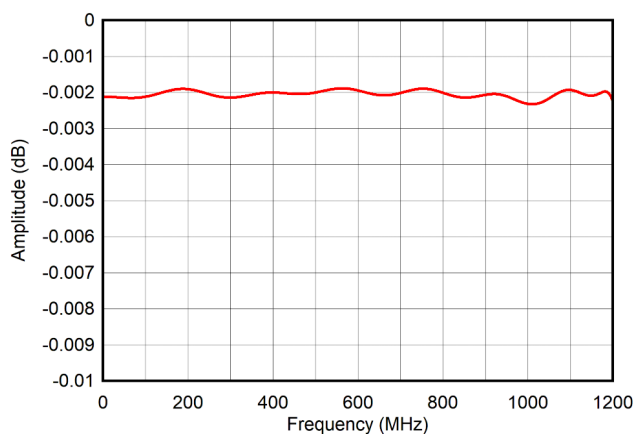


Figure 8-67. TX Back Stage Filter Response for Interpolate by 2 (Passband)

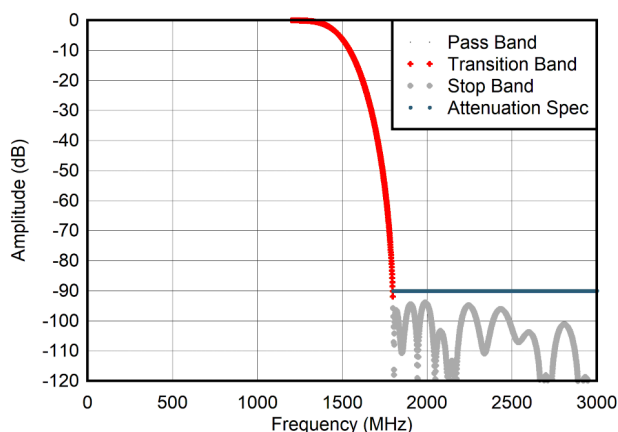


Figure 8-68. TX Back Stage Filter Response for Interpolate by 3 (Nyquist)

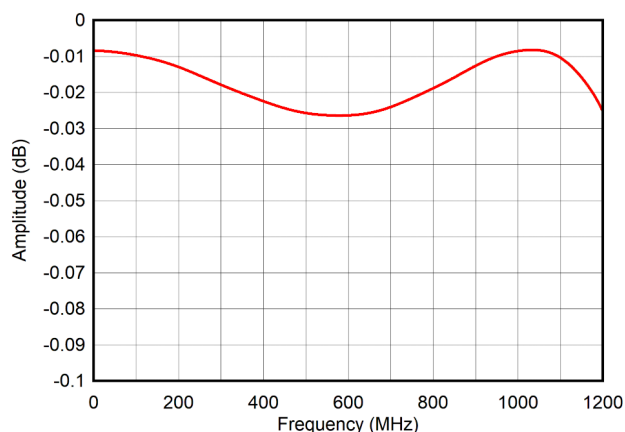


Figure 8-69. TX Back Stage Filter Response for Interpolate by 3 (Passband)

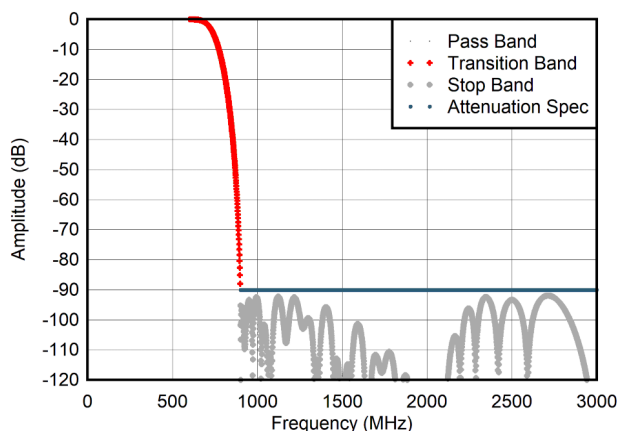


Figure 8-70. TX Back Stage Filter Response for Interpolate by 4 (Nyquist)

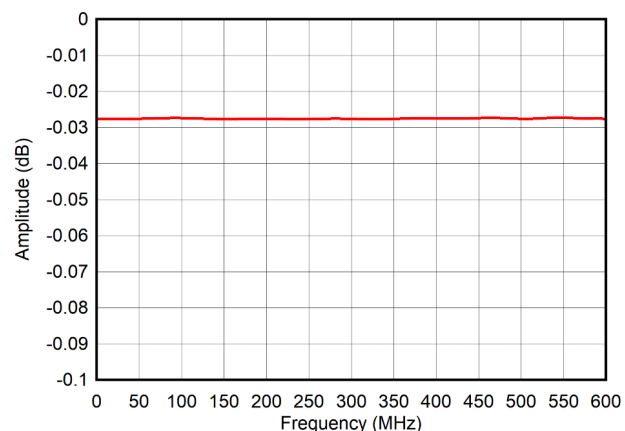


Figure 8-71. TX Back Stage Filter Response for Interpolate by 4 (Passband)

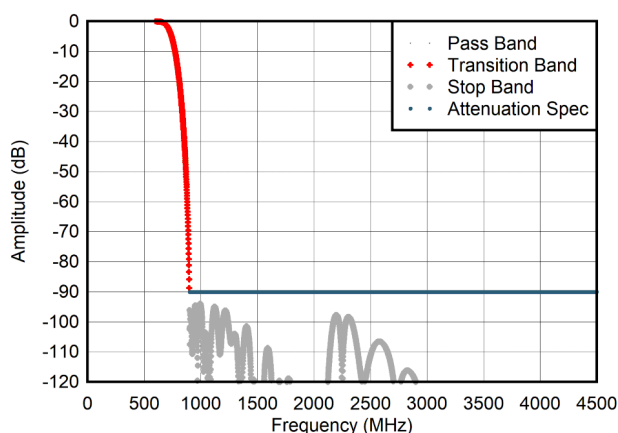


Figure 8-72. TX Back Stage Filter Response for Interpolate by 6 (Nyquist)

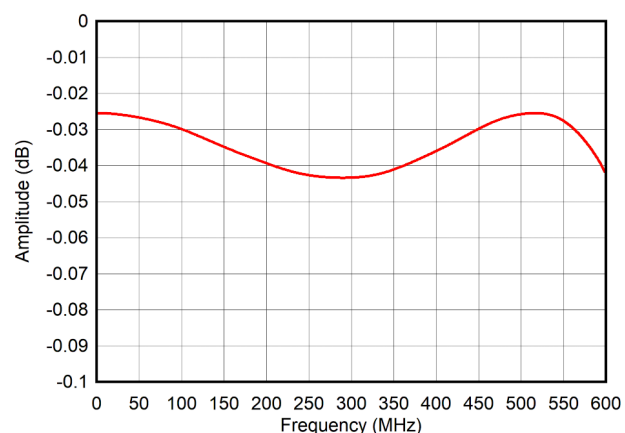


Figure 8-73. TX Back Stage Filter Response for Interpolate by 6 (Passband)

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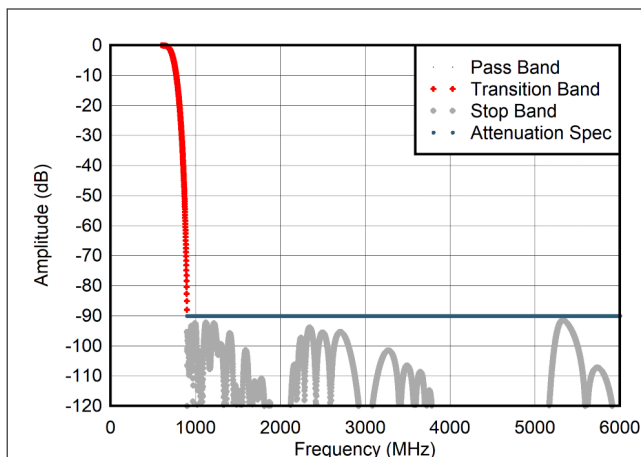


Figure 8-74. TX Back Stage Filter Response for Interpolate by 8 (Nyquist)

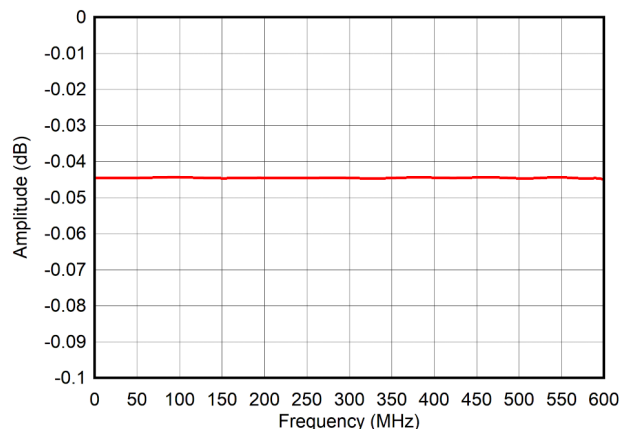


Figure 8-75. TX Back Stage Filter Response for Interpolate by 8 (Passband)

8.3.3.5 Digital Mixer and NCOs

The front and back mixers includes two NCOs each, whose frequency can be set independently. The front stage mixers can switch between two NCOs, each able to maintain the NCO phase at all times. The switch between the two NCOs can be controlled through the SPI or dedicated GPIO pin. The back stage digital mixer includes 16 NCOs whose frequency can be set independently. The mixers can switch between the NCOs and each NCO is able to maintain its phase accumulation at all times. The switch between the NCOs can be controlled through the SPI or dedicated GPIO pins. The NCOs have two options for setting the frequency. First, they can have a 32-bit resolution with the frequency specified as the $N \times \text{sample rate} \times 1/2^{32}$. Optionally, the NCOs can provide an exact 1-kHz raster for an input reference clock frequency of $N \times 61.44 \text{ MHz}$, where N is a integer. The NCOs and mixer provide a SFDR of 100 dB.

8.3.3.6 Inverse Sinc Filter

The device has an inverse Sinc filter that runs at the DAC update rate (f_{DAC}) that can be used to flatten the frequency response of the sample-and-hold output. There are two different filters - one for a zero order hold output used in 1st Nyquist zone and another for the mixed mode output used in the 2nd Nyquist zone. The DAC sample-and-hold output sets the output current and holds it constant for one DAC clock cycle until the next sample, resulting in the well known $\sin(x)/x$ or Sinc(x) frequency response (Figure 8-76, red line). The inverse sinc filter response (Figure 8-76, black line) has the opposite frequency response from 0 to $0.4 \times f_{\text{DAC}}$, resulting in the combined response (Figure 8-76, grey line). Similar curves are shown in Figure 8-77 for the 2nd Nyquist zone mode.

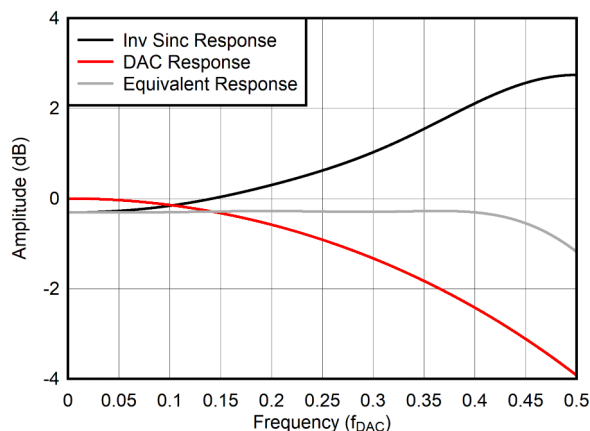


Figure 8-76. DAC, Inverse Sinc Filter and Composite Response for 1st Nyquist zone

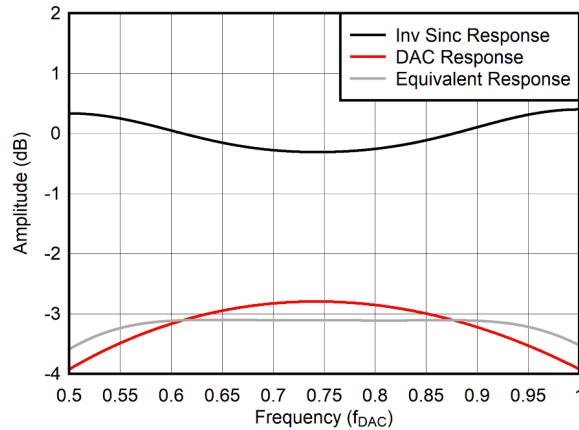


Figure 8-77. DAC, Inverse Sinc Filter and Composite Response for 2nd Nyquist zone

The inverse sinc filters have a gain > 1 at some frequencies. Therefore, the signal input to the inverse sinc filter must be reduced from full scale to prevent saturation in the filter. The amount of back-off required depends on the signal frequency, and is set such that at the signal frequencies the combination of the input signal and filter response is less than 1 (0 dB). For example, if the signal input to inverse sinc filter is at $0.25 \times f_{DAC}$, the response of the 1st Nyquist inverse sinc filter is 0.6 dB, and the signal must be backed off from full scale by 0.6 dB to avoid saturation. The advantage of the inverse sinc filter having a positive gain at all frequencies is that the user is then able to optimize the back-off of the signal based on its frequency.

8.3.3.7 Delay Block

A programmable delay can be configured in integer multiples of the DAC clock period up to 31 clocks through a dedicated 5-bit SPI register. There may be an offset in delay between the 0 delay setting when enabled and when the delay is disabled.

8.3.3.8 TX RF Output Gain Control (TX DSA)

The output stage of each transmitter chain is a wideband differential RF amplifier with integrated gain control, which conceptually we will refer to as the TX DSA. The gain of the output stage is set through the SPI accessing the allocated register. AFE7900 supports also a mode where the TX new gain setting is applied only when a dedicated GPIO is enabled, which is configured through the SPI. Each transmitter chain has two internal registers (reg A and reg B) for the DSA setting. In default mode only one register is used and its value is directly applied to the DSA. It is possible to configure the device through SPI to support the use of both registers. In this case, the selection of the valid register is done through dedicated pins. Three GPIO configurations are supported: one, two and four pin options.

In the one pin configuration a single GPIO function is used. Select the use of Reg A or Reg B to set the DSA for all 4 transmitter chains (Low = Reg A; High = Reg B). The channels for the swap can be masked or unmasked through a SPI register.

In the two pins configuration, instead one GPIO function level controls the use of reg A (low) or Reg B value for the gain setting of TX1 and TX2; while the other two chains (TX3 and TX4) are controlled by a second GPIO function.

In the four pin configuration, each TX channel can be controlled separately by a GPIO function.

The device supports a smooth change of TX DSA from one value to another. The TX DSA (in analog) supports gain steps of 0.25, 0.5, and 0.75 dB which can be used during the transition (the steady-state step size is 1 dB). The wait time in each step is programmable (as a Macro argument) with the resolution of 0.125 μ s.

The device can also use the TX digital gain in steps of 0.125 dB to make it look like the gain transition happens with steps of 0.125 dB. In the dual band case, the attenuation in each band can potentially move in different directions using the separate digital gain for each band.

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8.3.3.9 Straight, Interleaved and Mixed Mode Outputs

The device TX can operate in either straight or interleaved mode. Interleaved mode uses a half rate clock to save power, but will have an image at $F_{DAC}/2 - F_{OUT}$. With TI factory trim, the spur will be below -50 dBc.

The device TX can also operate in a mixed mode, where the output is inverted after $1/2$ of the DAC clock cycle. the results in the 2nd and 3rd Nyquist images to be emphasized with higher output power.

8.3.4 Feedback (FB) Chain

The AFE7900 includes 2 Feedback (FB) chains based on direct RF sampling architecture whose block diagram is shown in [Figure 8-78](#). The FB chains are often used as observation path of the PA (power amplifier) output for an external linearization DPD engine, but can also be used as additional receivers. The FB ADCs are identical to the RX ADCs. When the RX DDCs are configured with an output data rate above 750MSPS, the FB chains are not available.

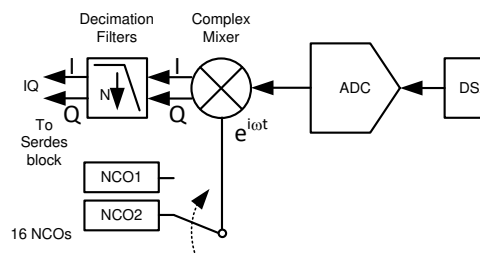


Figure 8-78. Feedback Path Block Diagram

8.3.4.1 Feedback Chain Analog Block

The FB path analog block includes an input DSA and a RF sampling ADC. The DSA attenuation is set through the SPI.

8.3.4.2 FB Chain Digital Block

The digital section of the AFE7900 feedback chain is shown in [Figure 8-78](#). The first function is a mixer to convert to a complex baseband signal. The mixer has four switchable NCOs, so for a multi-band application, the NCO phase for one band can be maintained when the other NCO for another band is being used. Following the mixer is a decimation stage.

8.3.4.3 Delay Block

A programmable delay can be configured in integer multiples of the ADC clock period up to 31 clocks through a dedicated 5-bit SPI register. There may be an offset in delay between the 0 delay setting when enabled and when the delay is disabled.

8.3.4.4 FB Peak Detector

The FB chain includes a peak detector at the ADC, whose output can be read through the SPI.

The digital peak detector first computes the peak value of the ADC over every 8 ADC samples. The overall peak among N such peaks is computed where N is the programmable block length. Block length (LSB is 8 full rate ADC CLKs) can be programmed with a 17 bit value. This peak value during the block is stored in an 8-bit SPI register. Peak over 8 samples is compared against a programmable threshold (8 bit value). The number of level crossings during the block length N is stored in a 17-bit SPI register. The values in the registers are continuously updated. To read the peak detector output, it is required to stop the SPI registers update through a specific register bit. After the reading of the peak detector registers has been completed, it is required to clear the bit that holds the update. When ADC is in half rate mode, the peak is computed over 4 samples and block length is defined in terms of every 4 ADC clocks (or 8 full rate ADC clocks).

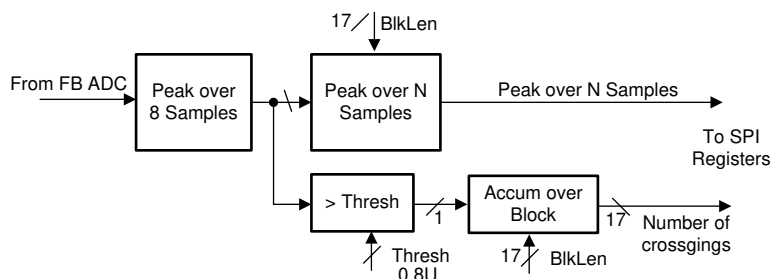


Figure 8-79. FB Peak Detector Block Diagram

8.3.4.5 FB Digital Mixer and NCOs

The FB path includes four NCOs, whose frequency can be set independently. The FB mixer can switch between four NCOs, each one running at different frequency, so the NCO phase is maintained at all times. The switch between the four NCOs can be controlled through the SPI or GPIO.

The NCOs have two options for setting the frequency. First, they can have a 32-bit resolution with the frequency specified as the $N \times \text{sample rate} \times 1/2^{32}$. Optionally, the NCOs can provide an exact 1-kHz raster for an input reference clock frequency of $N \times 61.44 \text{ MHz}$, where N is a integer. The NCOs and mixer provide a SFDR of 100 dB.

8.3.4.6 FB Decimation Block

The FB decimation block decimates the ADC sample rate data to the output rate. The decimation block is highly flexible, matching the interface rates to the possible ADC sample rates. Unlike the RX path, there is only one DDC per FB path. The rates are listed in the tables below. Boxes without numbers are not valid modes of operation.

For wide bandwidth modes such as decimate by 2 or 3, care should be taken to select the NCO so that the output bandwidth does not overlap an ADC Nyquist zone. For example, in decimate by 2 mode, the NCO frequency should be set to $(2 \times N - 1) \times f_{\text{ADC}}/4$ in the center of the Nyquist zone, where N is the Nyquist zone number. For decimate by 3, the NCO frequency should be set within approximately 250 MHz from the center of the Nyquist zone

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Table 8-7. Decimation Factors Between FB ADC and Output Sample Rates

		ADC SAMPLE (MSPS) RATE					
		1250	1500	2000	2211.84	2500	3000
Output Rate (MSPS)	125	10	12	16		20	24
	187.5		8		12		16
	250	5	6	8		10	12
	375		4		6		8
	500	2.5	3	4		5	6
	750		2		3		4
	1000			2		2.5	3
	1500						2

The digital decimation filters provide over 85 dB of image rejection of the in-band signal. Passband is defined as 81.4% of the baseband sample rate and in-band peak-to-peak ripple is less than 0.04 dB.

The decimation filter responses are shown in [Figure 8-80](#) through [Figure 8-103](#).

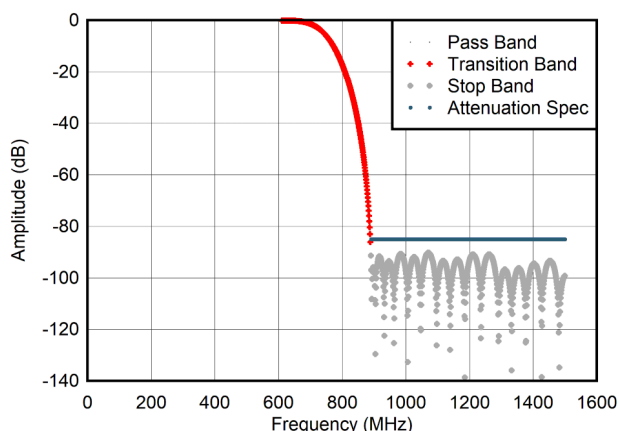


Figure 8-80. FB Filter Response for Decimation by 2 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

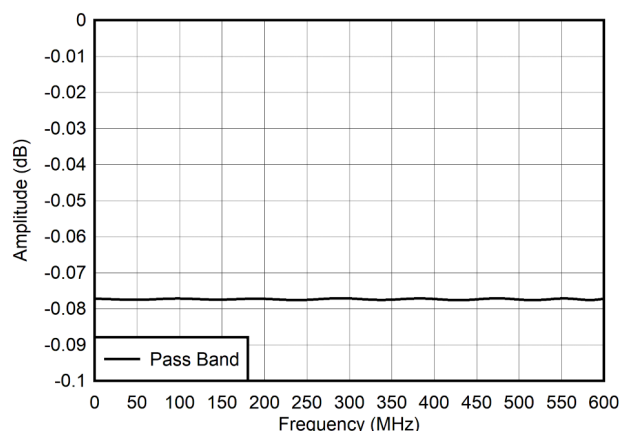


Figure 8-81. FB Filter Response for Decimation by 2 with $f_{ADC} = 3\text{GSPS}$ (Passband)

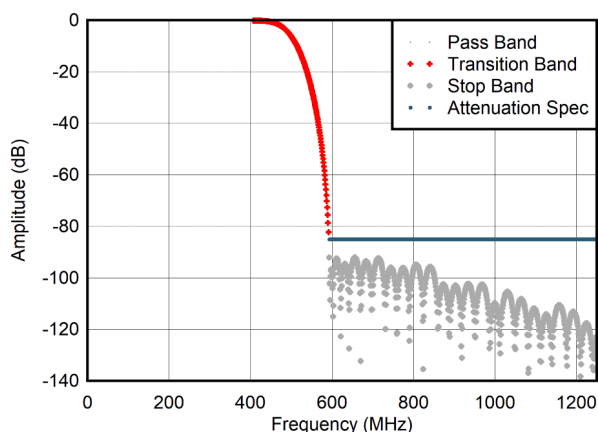


Figure 8-82. FB Filter Response for Decimation by 2.5 with $f_{ADC} = 2.5\text{GSPS}$ (Nyquist)

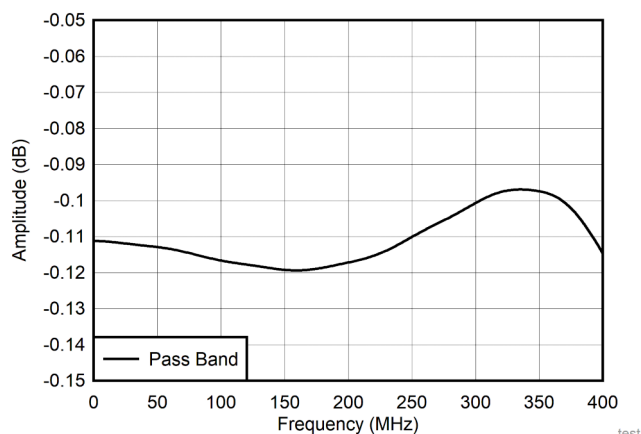


Figure 8-83. FB Filter Response for Decimation by 2.5 with $f_{ADC} = 2.5\text{GSPS}$ (Passband)

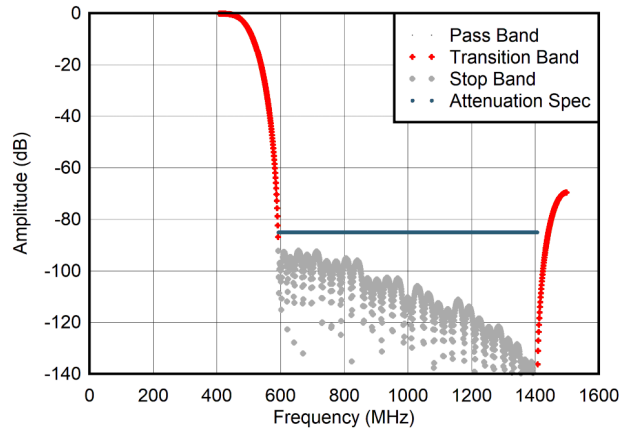


Figure 8-84. FB Filter Response for Decimation by 3 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

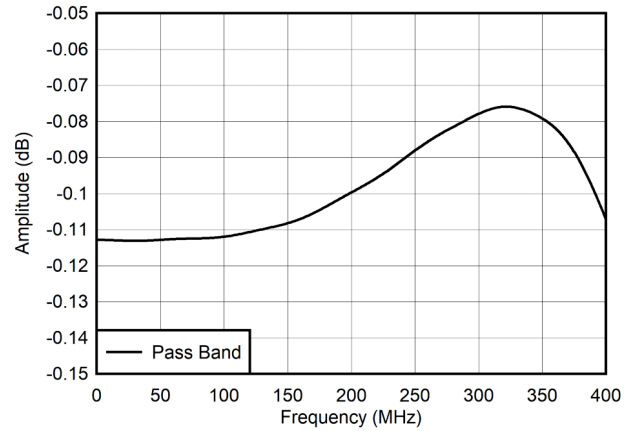


Figure 8-85. FB Filter Response for Decimation by 3 with $f_{ADC} = 3\text{GSPS}$ (Passband)

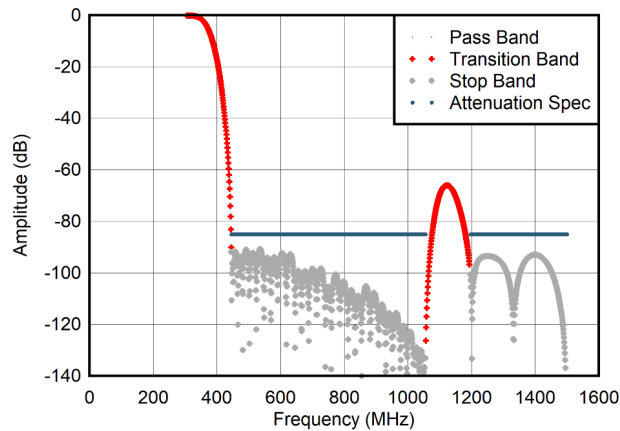


Figure 8-86. FB Filter Response for Decimation by 4 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

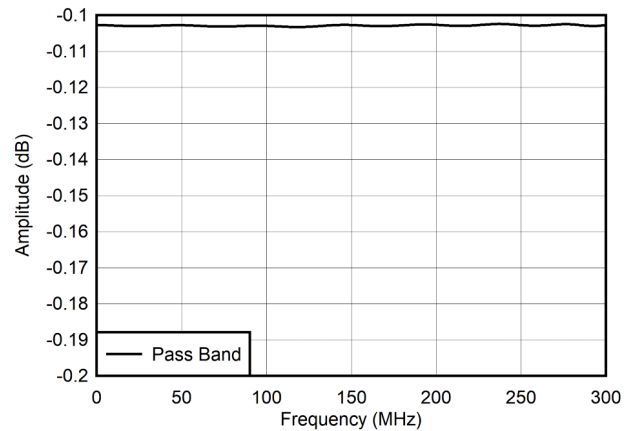


Figure 8-87. FB Filter Response for Decimation by 4 with $f_{ADC} = 3\text{GSPS}$ (Passband)

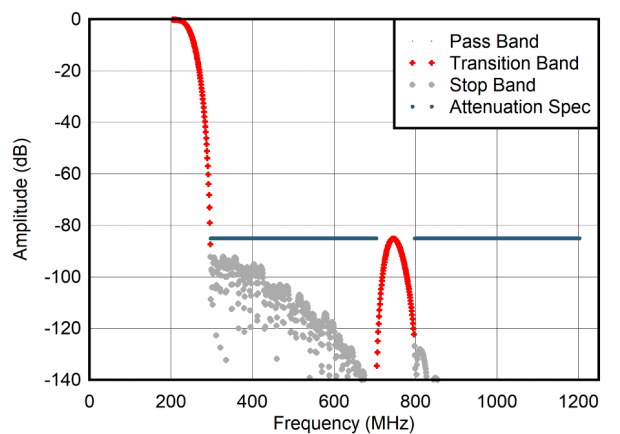


Figure 8-88. FB Filter Response for Decimation by 5 with $f_{ADC} = 2.5\text{GSPS}$ (Nyquist)

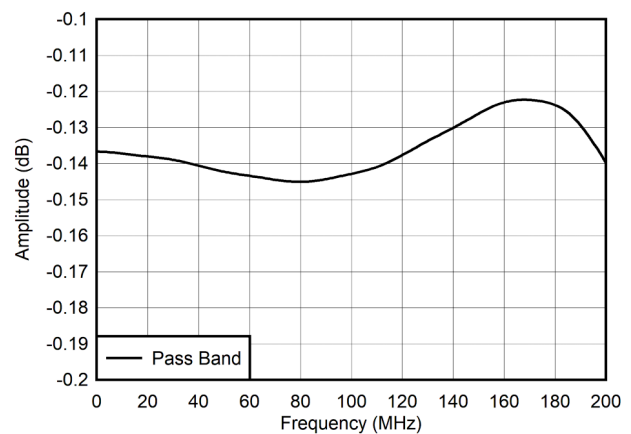


Figure 8-89. FB Filter Response for Decimation by 5 with $f_{ADC} = 2.5\text{GSPS}$ (Passband)

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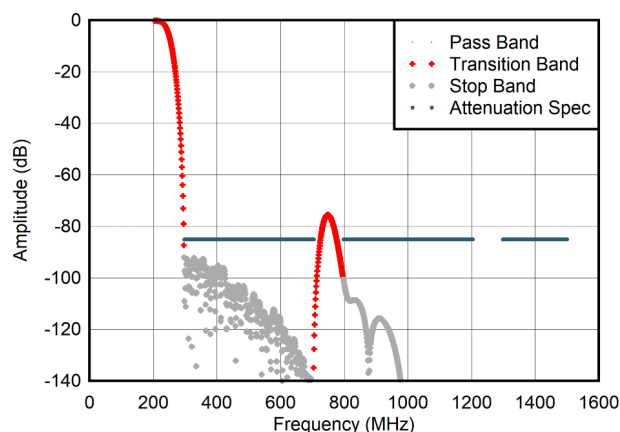


Figure 8-90. FB Filter Response for Decimation by 6 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

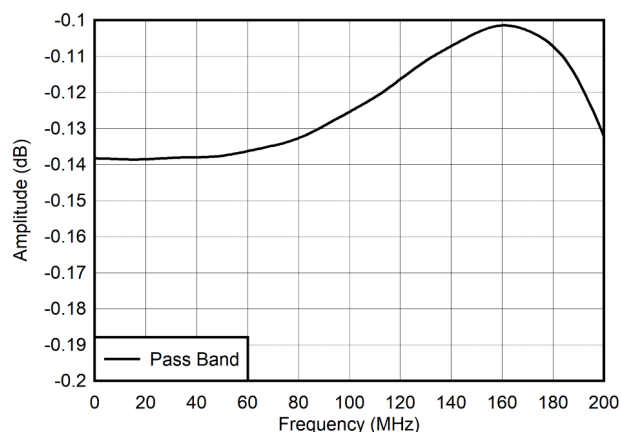


Figure 8-91. FB Filter Response for Decimation by 6 with $f_{ADC} = 3\text{GSPS}$ (Passband)

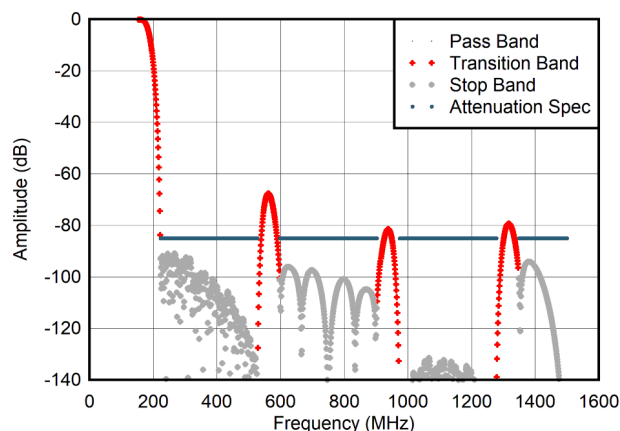


Figure 8-92. FB Filter Response for Decimation by 8 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

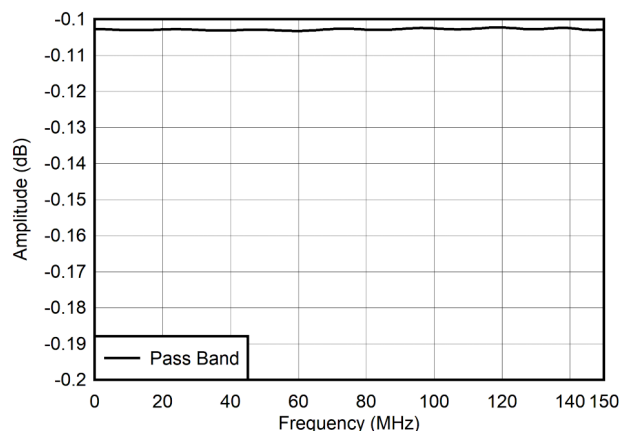


Figure 8-93. FB Filter Response for Decimation by 8 with $f_{ADC} = 3\text{GSPS}$ (Passband)

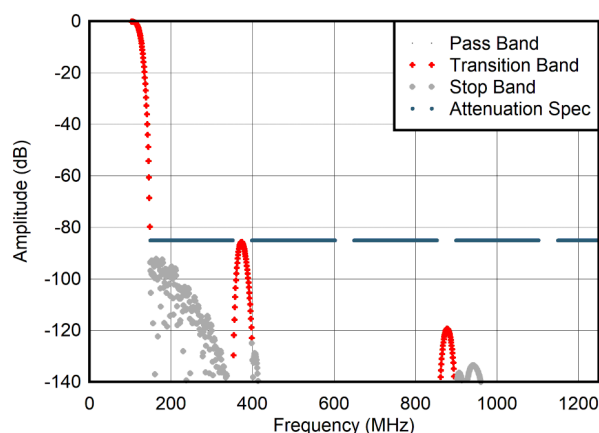


Figure 8-94. FB Filter Response for Decimation by 10 with $f_{ADC} = 2.5\text{GSPS}$ (Nyquist)

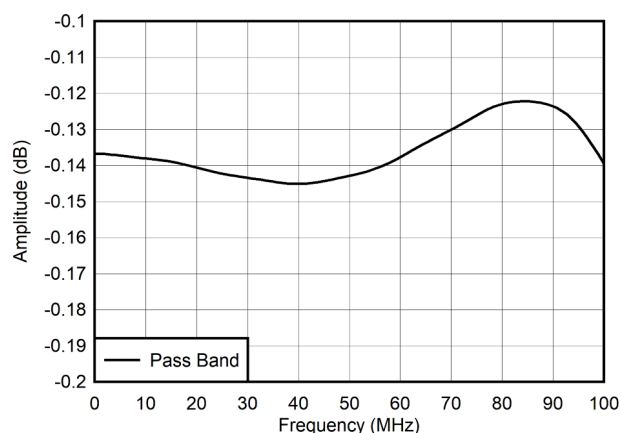


Figure 8-95. FB Filter Response for Decimation by 10 with $f_{ADC} = 2.5\text{GSPS}$ (Passband)

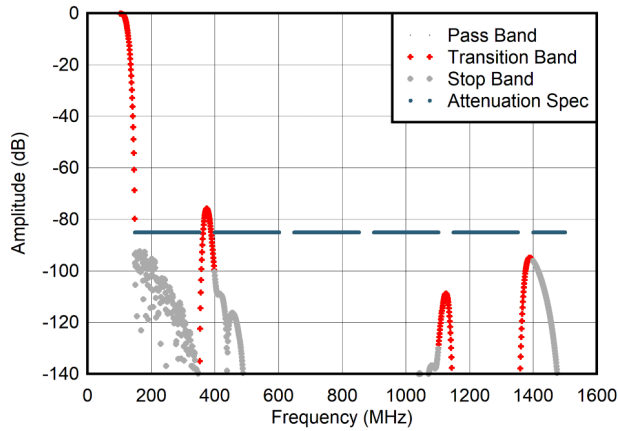


Figure 8-96. FB Filter Response for Decimation by 12 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

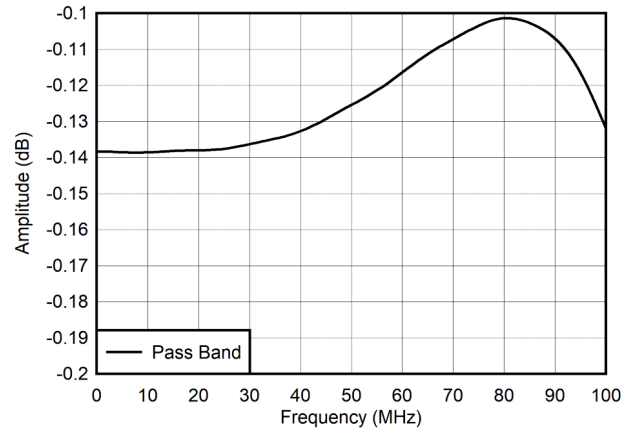


Figure 8-97. FB Filter Response for Decimation by 12 with $f_{ADC} = 3\text{GSPS}$ (Passband)

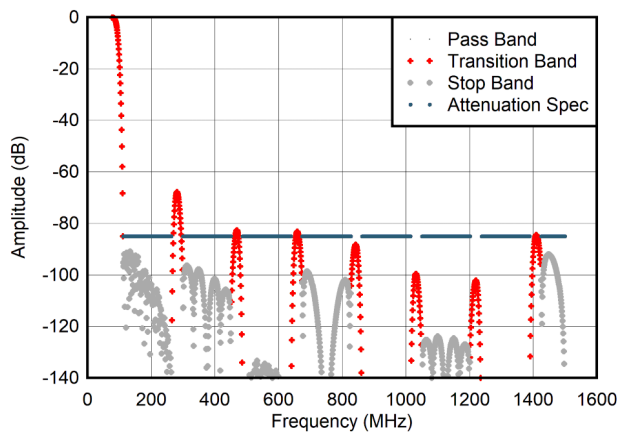


Figure 8-98. FB Filter Response for Decimation by 16 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

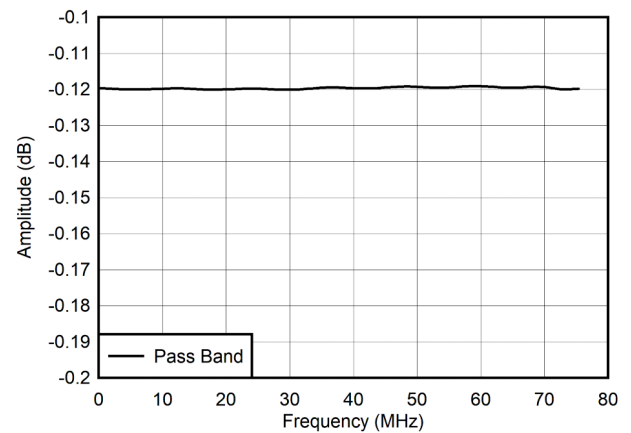


Figure 8-99. FB Filter Response for Decimation by 16 with $f_{ADC} = 3\text{GSPS}$ (Passband)

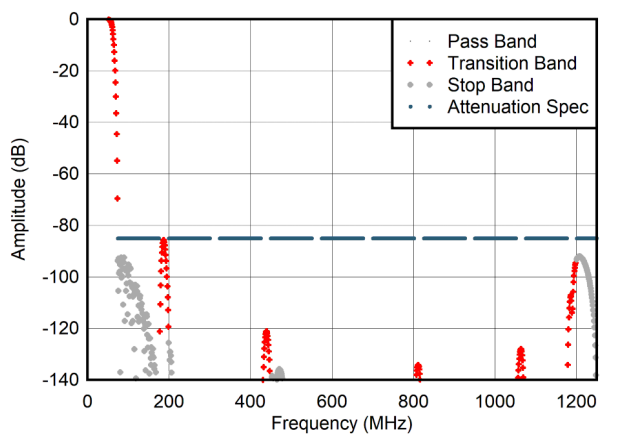


Figure 8-100. FB Filter Response for Decimation by 20 with $f_{ADC} = 2.5\text{GSPS}$ (Nyquist)

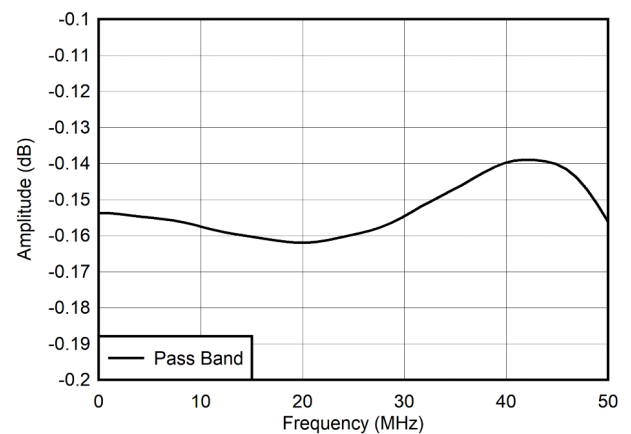


Figure 8-101. FB Filter Response for Decimation by 20 with $f_{ADC} = 2.5\text{GSPS}$ (Passband)

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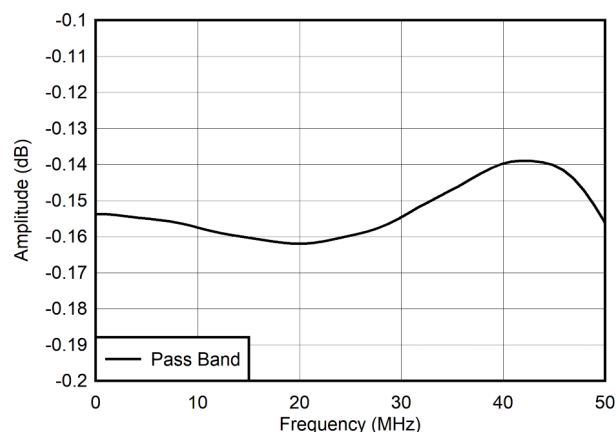


Figure 8-102. FB Filter Response for Decimation by 24 with $f_{ADC} = 3\text{GSPS}$ (Nyquist)

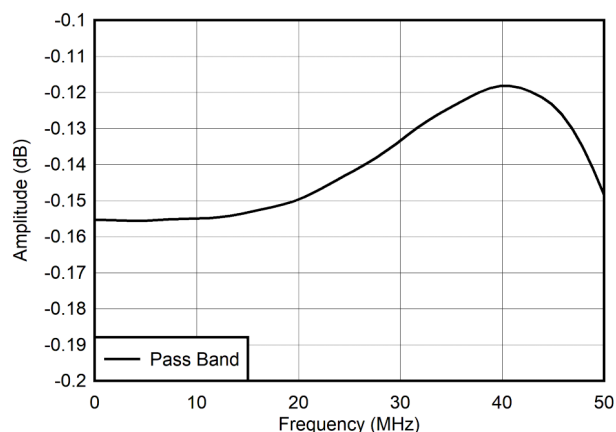


Figure 8-103. FB Filter Response for Decimation by 24 with $f_{ADC} = 3\text{GSPS}$ (Passband)

8.3.4.7 Digital Gain Control Block

A separate digital gain control is available in the digital block. The range of the gain control is -2.5 dB to 21 dB in 0.5 dB steps (0 corresponds to -2.5 dB); 47 corresponds to 21 dB). The gain setting can be controlled through the SPI.

8.3.5 Synthesizers and Clocking

8.3.5.1 Internal PLL/VCO

The device has an internal PLL with 4 separate VCOs to generate the clock at the DAC sample rate (or at 2x the DAC sample rate). The VCOs cover the frequencies around 7.5 GHz, 8 GHz, 9 GHz, 10 GHz and 12 GHz.

The recommended common reference clock frequency (F_{REF}) is 500 MHz, but the device can work with F_{REF} down to 125 MHz.

8.3.5.2 DAC/ADC Sample Rate Combinations

When using a divided DAC clock for the ADC clock (required for the FB ADCs), the available DAC and ADC sample rates combinations is given in [Table 8-8](#):

Table 8-8. TX DAC / FB ADC Rate Combinations

÷	f_{DAC} (MSPS)								
	4000	4500	5000	6000	7500	8000	9000	10000	12000
2	2000	2250	2500	3000					
3		1500		2000	2500		3000		
4			1250	1500		2000	2250	2500	3000
6							1500		

The RX ADC rate can be independently selected from the FB ADC rate. Additionally, the RX ADC can use the input clock directly at the RX ADC sample rate. In that case the input clock is divided to provide the reference clock for the internal PLL/VCO.

8.3.5.3 Clock Distribution

The device has a flexible clock distribution circuit that is shown in [Figure 8-104](#). The input clock can be used as a reference for the internal PLL/VCO and/or as an direct external clock for the DACs and ADCs. When used as a reference clock for the PLL/VCO, the input clock can be divided by the reference divider before the phase frequency detector (PFD). Each group of RX ADCs, FB ADCs or DAC can select either the PLL/VCO output or the external input clock. In this way for example, the RX ADCs can use the input clock directly, while a divided version of the input clock is used for the PLL/VCO, which then drives the DAC and FB ADCs.

When the reference divider is not equal to 1, the SYSREF input can be used to sync the N-divider. This is useful for synchronizing the PFD frequency of the on-chip PLLs across multiple devices.

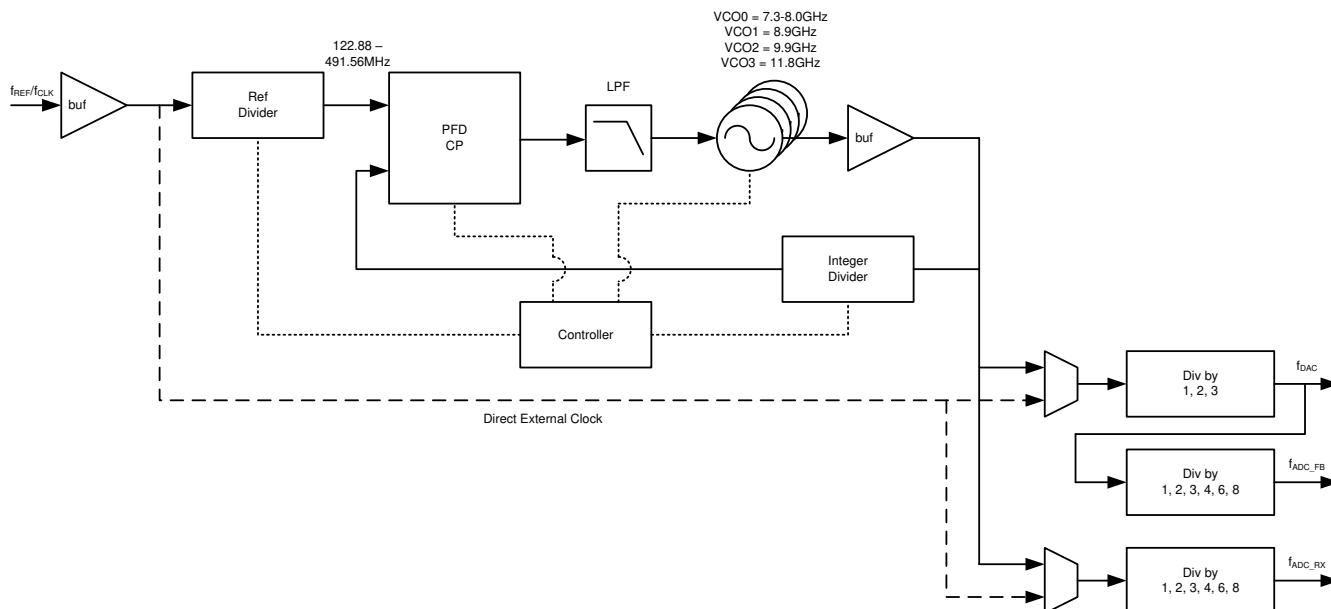


Figure 8-104. Clock Distribution Chain

8.3.6 SYSREF Requirements

In many applications, such as multi antenna systems where the various transmit channels information is correlated, it is required that the latency across the link is deterministic and multiple devices are completely synchronized such that their outputs are phase aligned. The device achieves the deterministic latency using SYSREF to synchronize the devices internal dividers, signal processing blocks and elastic buffer. SYSREF is generated from the same clock domain as the device clock.

The SYSREF capture requirements are shown in [Figure 8-105](#). Three SYSREF pulses are required to completely synchronize the device. These three pulses are necessary to synchronize the N-divider (if needed), clock divider for the digital logics, and the JESD204 link-up. SYSREF usage in the bring-up software flow is described in the AFE79xx Configuration Guide available from TI. For each pulse, a SPI register latch is programmed high, after which the 1st SYSREF pulse is captured and the following pulses are ignored. SYSREF then would need to be held low for the SPI latch to be programmed low then high again for the next pulse. After the 3 pulses, TI recommends that SYSREF is turned off or held low to prevent spurs coupling into the device clock.

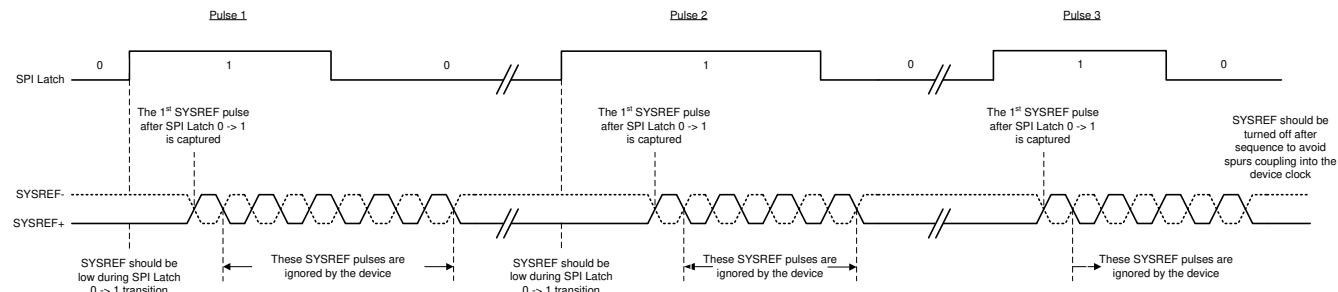


Figure 8-105. SYSREF Capture Requirements

The SYSREF pulse must match a gapped periodic timing with the frequency matching the following requirements:

- RX/FB ADC sampling rate/48
- TX DAC sampling rate/192

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- RX/FB/TX Interface Rate/16
- In the 204B case, all lane rates/LCM($40, 10 \times K \times F$) where K is the number of multi frames and F is the # of octets/frame.
- In the 204C case, all lane rates/ $(2112 \times E)$ where E is the number of Extended Multi Blocks.
- It should be a maximum of 5.76 MHz.

An Excel spreadsheet to calculate possible SYSREF frequencies is available from TI.

8.3.7 SYSREF Timing Detector

The device contains a detector to determine the optimum timing of SYSREF relative to the input device clock. The timing skew of SYSREF to device clock must be done externally.

Internal to the device, five phase shifted clocks are generated (CLK0 – CLK4). CLK2 is used to latch SYSREF for device operation. CLK0 and CLK1 are advanced 50ps and 25ps ahead of CLK2, CLK 3 and CLK4 are delayed 25ps and 50ps behind CLK2.

The outputs of SYSREF are latched using CLK0 to CLK4. These five outputs are then latched to SPI registers when SYSREF is latched on inverted CLK2. There are five possible outputs – 5'b11111, 5'b01111, 5'b00111, 5'b00011, 5'b00001 and 5'b00000. SYSREF can be aligned with fall edge of CLK2 (output = 5'b00111), so that use of CLK2 will result in deterministic latching of SYSREF. This is done by programming register bit `po_fbcd_3g_interface_control<23>` to invert the clock for the measurement. If the transition is centered on inverted clock then it will be ideal for non-inverted clock.

There is an option to provide the inverted version of latching clock to the SYSREF Monitor block (i.e. CLK = ~latching clock, so that SYSREF can be aligned with inverted version of latching clock (output = 5'b00111). With this, the SYSREF edge can be aligned with negative edge of latching clock. This will ensure deterministic latching of SYSREF in the end application.

Table 8-9 shows the SYSREF monitor output as the device clock is delayed relative to SYSREF. The device clock is inverted. With a delay of 0ps, SYSREF is aligned with the negative edge of the SYSREF latching clock and would be the optimum delay setting.

Table 8-9. Example of SYSREF Monitor Output with Device Clock Delay

Delay (ps)	SYSREF Monitor Output
0	5b00011
25	5b00111
50	5b01111
75	5b11111
100	5b11111
125	5b11111
150	5b11111
175	5b11111
200	5b11111
225	5b11111
250	5b11111
275	5b11111
300	5b11111
325	5b11111

8.3.8 SerDes

The AFE7900 has two SerDes macros. Each SerDes macro is composed by a TX block with 4 transmitter lanes, a RX block with 4 receiver lanes, and a common PLL block for TX and a common PLL block for RX. A high level

block diagram of each SerDes macro is shown in [Figure 8-106](#). The SerDes supports multiple lane rates divided in 3 modes: Full, Half, and Quarter rate mode.

Table 8-10. SerDes Lane Rates

MODE	RATES
Full Rate	18.5 to 29.5 Gbps
Half Rate	9.25 to 16.25 Gbps
Quarter Rate	4.625 to 8.12 Gbps

Within each SerDes macro, each TX and RX lane can be enabled or disabled independently to optimize the power dissipation.

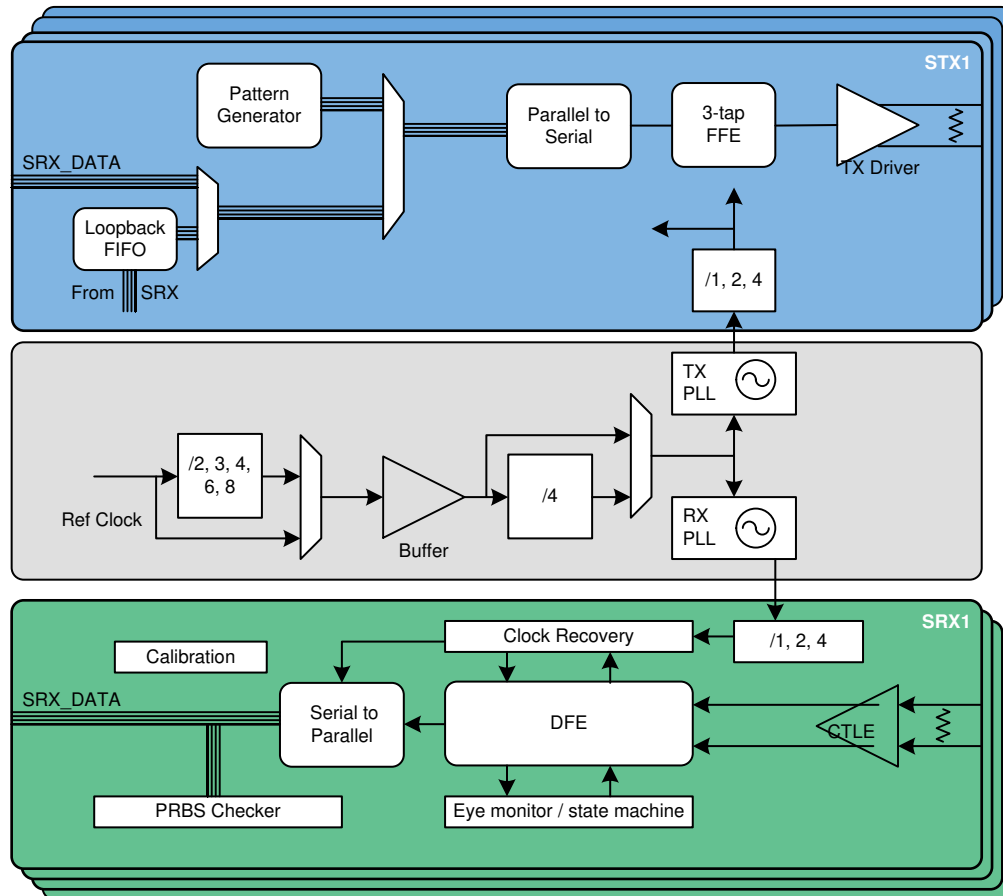


Figure 8-106. SerDes Block Diagram

8.3.8.1 SerDes Multiplexer

The device contains a multiplexer that is able to map any JESD stream to any SerDes transceiver. The SerDes rates will be limited by the common TX and RX PLLs so that the baud rate for each group of four SerDes will need to be related by a factor of 2 or 4.

8.3.8.2 SerDes Transmitter

Each SerDes transmitter incorporates a three tap finite impulse response (FIR) filter and a programmable output amplitude to compensate for frequency dependent loss in the transmission media. The 3-tap FFE for the TX pre-emphasis is defined by [Equation 2](#):

$$x(k) = c_{-1} a(k+1) + c_0 a(k) + c_1 a(k-1) \quad (2)$$

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where

- the binary input is $\{-1, 1\}$.

All coefficients are register programmable with a step size of 1. The coefficients have to be set such that $x(k)$ is less than or equal to 25 and is in accordance with [Table 8-11](#).

Table 8-11. SerDes TX FFE Settings

MAIN CURSOR VALUE	POST-CURSOR VALUE	PRE-CURSOR VALUE	POST-CURSOR EQUALIZATION (dB)	PRE-CURSOR EQUALIZATION (dB)	POST-CURSOR SETTING	PRE-CURSOR SETTING	MAIN SETTING
25	0	0	0	0	000	000	000
23	0	0	0	0	000	000	001
21	0	0	0	0	000	000	010
19	0	0	0	0	000	000	011
17	0	0	0	0	000	000	100
15	0	0	0	0	000	000	101
13	0	0	0	0	000	000	110
11	0	0	0	0	000	000	111
24	-1	0	0.72	0	001	000	000
20	-1	0	0.87	0	001	000	010
16	-1	0	1.09	0	001	000	100
12	-1	0	1.45	0	001	000	110
23	-2	0	1.51	0	010	000	000
21	-2	0	1.66	0	010	000	001
15	-2	0	2.33	0	010	000	100
22	-3	0	2.38	0	011	000	000
13	-2	0	2.69	0	010	000	101
21	-4	0	3.35	0	100	000	000
19	-4	0	3.71	0	100	000	001
14	-3	0	3.78	0	011	000	100
17	-4	0	4.17	0	100	000	010
20	-5	0	4.44	0	101	000	000
15	-4	0	4.75	0	100	000	011
16	-5	0	5.62	0	101	000	010
19	-6	0	5.68	0	110	000	000
17	-6	0	6.41	0	110	000	001
18	-7	0	7.13	0	111	000	000
24	0	-1	0	0.72	000	001	000
20	0	-1	0	0.87	000	001	010
22	-2	-1	1.66	0.87	010	001	000
16	0	-1	0	1.09	000	001	100
20	-4	-1	3.71	1.09	100	001	000
12	0	-1	0	1.45	000	001	110
14	-2	-1	2.69	1.45	010	001	100
16	-4	-1	4.75	1.45	100	001	010
18	-6	-1	6.41	1.45	110	001	000
23	0	-2	0	1.51	000	010	000
21	0	-2	0	1.66	000	010	001
22	-1	-2	0.87	1.66	001	010	000
15	0	-2	0	2.33	000	010	100
19	-4	-2	4.17	2.33	100	010	000
22	0	-3	0	2.38	000	011	000
18	-5	-2	5.62	2.69	101	010	000

Table 8-11. SerDes TX FFE Settings (continued)

MAIN CURSOR VALUE	POST-CURSOR VALUE	PRE-CURSOR VALUE	POST-CURSOR EQUALIZATION (dB)	PRE-CURSOR EQUALIZATION (dB)	POST-CURSOR SETTING	PRE-CURSOR SETTING	MAIN SETTING
13	0	-2	0	2.69	000	010	101
14	-1	-2	1.45	2.69	001	010	100
17	-4	-2	4.75	2.69	100	010	001
21	0	-4	0	3.35	000	100	000
19	0	-4	0	3.71	000	100	001
20	-1	-4	1.09	3.71	001	100	000
18	-4	-3	4.75	3.78	100	011	000
14	0	-3	0	3.78	000	011	100
17	0	-4	0	4.17	000	100	010
19	-2	-4	2.33	4.17	010	100	000
20	0	-5	0	4.44	000	101	000
15	0	-4	0	4.75	000	100	011
16	-1	-4	1.45	4.75	001	100	010
18	-3	-4	3.78	4.75	011	100	000
17	-2	-4	2.69	4.75	010	100	001
16	0	-5	0	5.62	000	101	010
18	-2	-5	2.69	5.62	010	101	000
19	0	-6	0	5.68	000	110	000
18	-1	-6	1.45	6.41	001	110	000

In the Quarter Rate mode, the 3-tap FFE is not available.

Each SerDes transmitter driver has an internal termination resistor of 100 Ω , and its maximum peak-to-peak differential output voltage is 1 V_{pp} and programmable down to 500 mV_{pp}.

8.3.8.3 SerDes Receiver

Each SerDes receiver consists of a Continuous Time Linear Equalizer (CTLE), followed by 1-tap adaptive decision feedback equalization (DFE). A clock recovery loop locks the incoming DFE data and makes the clock available to the common PLL block and can be used for the TX block if needed. The incoming signal first passes through the configurable CTLE. Then the remaining ISI at the CTLE output is removed by the DFE equalizer. DFE taps settings are constantly optimized based on the eye opening at the channel output. The data recovery block finds the optimal sampling phase for the equalized signal at the DFE output. The recovered clock, locked at the incoming data, is then used to generate the clock for the RX parallel data output.

The RX input includes an internal termination of 100- Ω differential. It doesn't integrate a DC-blocking capacitors, but each receiver lane can accept common-mode voltage within the range 0.4 V to 0.6 V. If the common voltage is outside this range, external series capacitors are required.

8.3.8.4 SerDes PLL, Common Block

The common block integrates two PLLs, one for the transmitters and one for the receivers; each PLL can be programmed separately. The TX PLL is shared by all 4 TX lanes and the RX PLL is shared by all 4 RX lanes. Each RX and TX lane has a dedicated clock divider by 1, 2, and 4, so that each lane can be configured independently into Full, Half, and Quarter rate mode. The VCO integrated in the both TX and RX covers the full rate mode frequency range (19.5 GHz to 32.5 GHz). The reference clock of the TX and RX PLL is derived from the external input reference clock through a programmable frequency divider with following division options: /1, /2, /3, /4, /6, and /8.

8.3.8.5 SerDes Test Modes

Each SerDes macro supports multiple test modes for self-test. In the TX block four self-generating PRBS patterns are available, as 32-bit repeating patterns, based on user register programmable data. The following PRBS patterns are supported:

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1. PRBS9 ($x^9 + x^5 + 1$).
2. PRBS15 ($x^{15} + x^{14} + 1$)
3. PRBS23 ($x^{23} + x^{18} + 1$)
4. PRBS31 ($x^{31} + x^{28} + 1$)

The receiver chain integrates a checker for detecting the PRBS pattern error. It includes also an eye monitor to detect the eye height as well as generating more detailed eye diagrams, that can be read through the SPI.

The SerDes macro supports loopback of the RX block recovered data to the TX block through a FIFO. In this mode, the TX and RX lanes rate need to match. The loopback allows for full data path (TX and RX) verification.

8.3.9 JESD204B, JESD204C**8.3.9.1 Link Configuration and SYNC\ Interface**

The AFE7900 interface can be configured with single or multiple links. The four transmitter chains and four received chains JESD can be arranged as single or dual links. The feedback path can be configured as single link. The possible link to SerDes lanes configurations are summarized in [Table 8-12](#):

Table 8-12. JESD Link Configurations

	CONFIGURATION	DESCRIPTION
RX/FB Chains	6 links	1 link for each RX or FB chain. 4 links with 1 SerDes lane, 2 links with up to 2 SerDes lanes.
	4 links	2 links for RX and 2 links for FB, or 3 links for RX (2 on AB, 1 on CD), 1 link for FB.
	3 Links	2 links for RX and 1 link for FB chain; Each link for up to 2 SerDes lanes
	2 Links	1 link for RX and 1 link for FB; Each link for up to 4 SerDes lanes
	1 Link	1 link for RX chains for up to 8 SerDes lanes
	2 Links Shared	RX and FB sharing SerDes lanes: 2 links each one for up to 4 SerDes lanes
	1 Link Shared	RX and FB sharing SerDes lanes: 1 link for up to 4 SerDes lanes
TX Chains	4 Links	Each link for up to 2 SerDes lanes
	2 Links	Each link for up to 4 SerDes lanes
	1 Link	Single link for up to 8 SerDes lanes

The AFE7900 ballmap includes 4 balls for the SYNC\ input and 4 balls for the SYNC\ output. Both the 4 inputs and the 4 outputs can be programmed to support two differential LVDS or up to four single-ended CMOS inputs/outputs. The four pins SYNCINA/B/C/D are used for both the RX and FB chains. In addition, two other GPIO balls can be assigned to support 2 addition SYNC\ inputs.

8.3.9.2 JESD204B/C Scrambler and Descrambler

For JESD204B, the scrambler is a 16-bit parallel self-synchronous scrambler based on the polynomial $1 + x^{14} + x^{15}$. For JESD204C, the scrambler is a 16-bit parallel self-synchronous scrambler based on the polynomial $1 + x^{58} + x^{39}$. From the standard specification, the scrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence.

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. From the JESD204B specification, the descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence.

8.3.9.3 JESD204B/C Frame Assembly

The JESD204B defines the following parameters:

- L = is the number of lanes
- M = is the number of I or Q streams per device (2 = 1 IQ pair, 4 = 2 IQ pairs, 8 = 4 IQ pairs)
- F = is the number of octets per frame clock period.
- S = is the number of samples per frame
- HD = is the High-Density bit which controls whether a sample may be divided over more lanes.
- N = NPRIME is the number of bits per sample (12 or 16 bits)

Same parameters are used for the JESD204C frame assembly.

8.3.9.3.1 JESD204B/C Frame Assembly for Transmitter Chains

The AFE7900 transmitter chains support multiple JESD modes, listed in the following [Table 8-13](#) for 1 DUC per TX and [Table 8-15](#) for 2 DUCs per TX (AFE7988/20 only). For each of the supported input rates, all possible L-M-F-S-Hd as single or dual links are listed with the associated SERDES RATES, for both 8b/10b and 64b/66b encoding.

Table 8-13. JESD204B/C Formats for 1 DUC per TX Chain

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
125	16	8/10b	20	1-8-16-1-0	
	16	8/10b	10	2-8-8-1-0	1-4-8-1-0
	16	64/66b	16.25 ⁽¹⁾	1-8-16-1-0	
187.5	16	8/10b	7.5	4-8-4-1-0	2-4-4-1-0
	16	8/10b	15	2-8-8-1-0	1-4-8-1-0
	16	64/66b	12.375	2-8-8-1-0	1-4-8-1-0
250	16	8/10b	20	2-8-8-1-0	1-4-8-1-0
	16	8/10b	10	4-8-4-1-0	2-4-4-1-0
	16	64/66b	16.25 ⁽¹⁾	2-8-8-1-0	1-4-8-1-0
	16	64/66b	8.125 ⁽¹⁾	4-8-4-1-0	2-4-4-1-0
375	16	8/10b	29.5 ⁽²⁾	2-8-8-1-0	1-4-8-1-0
	16	8/10b	20	3-6-4-1-0	
	16	8/10b	15	4-8-4-1-0	2-4-4-1-0
	16	8/10b	7.5	8-8-2-1-0	4-4-2-1-0
	16	64/66b	24.75	2-8-8-1-0	1-4-8-1-0
	16	64/66b	12.375	4-8-4-1-0	2-4-4-1-0
500	16	8/10b	20	4-8-4-1-0	2-4-4-1-0
	16	8/10b	10	8-8-2-1-0	4-4-2-1-0
	16	64/66b	16.25 ⁽¹⁾	4-8-4-1-0	2-4-4-1-0
	16	64/66b	8.125 ⁽¹⁾	8-8-2-1-0	4-4-2-1-0
	12	8/10b	29.5 ⁽²⁾	2-8-6-1-0	1-4-6-1-0
	12	8/10b	15	4-8-3-1-0	2-4-3-1-0
	12	8/10b	7.5	8-8-3-2-0	4-4-3-2-0
	12	64/66b	24.75	2-8-6-1-0	1-4-6-1-0
	12	64/66b	12.375	4-8-3-1-0	2-4-3-1-0
	24	64/66b	24.75	4-8-6-1-0	2-4-6-1-0
750	16	8/10b	29.5 ⁽²⁾	4-8-4-1-0	2-4-4-1-0
	16	8/10b	15	8-8-2-1-0	4-4-2-1-0
	16	64/66b	24.75	4-8-4-1-0	2-4-4-1-0
	16	64/66b	24.75	4-8-8-2-0	2-4-8-2-0
	16	64/66b	12.375	8-8-2-1-0	4-4-2-1-0
	12	8/10b	22.5	4-8-3-1-0	2-4-3-1-0
	12	8/10b	11.25	8-8-3-2-0	4-4-3-2-0
1000	16	8/10b	20	8-8-2-1-0	4-4-2-1-0
	16	64/66b	16.5	8-8-2-1-0	4-4-2-1-0
	12	64/66b	24.75	4-8-3-1-0	2-4-3-1-0
	12	64/66b	12.375	8-8-3-2-0	4-4-3-2-0
	24	64/66b	24.75	8-8-3-1-0	4-4-3-1-0

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Table 8-13. JESD204B/C Formats for 1 DUC per TX Chain (continued)

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
1500	16	8/10b	29.5 ⁽²⁾	8-8-2-1-0	4-4-2-1-0
	16	64/66b	24.75	8-8-2-1-0	4-4-2-1-0
	12	8/10b	22.5	8-8-3-2-0	4-4-3-2-0

- (1) The input rate is limited to 0.985x the stated input rate due to the serdes PLL frequency limitation for baud rates between 16.25 and 19GHz
- (2) The input rate is limited to 0.983x the stated input rate due to the maximum baud rate of 29.5Gbps

Table 8-14. Wide Bandwidth JESD204B/C Formats for 1 DUC per TX Chain (2TX Only)

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
2000	16	8/10b	20	8-4-1-1-0	4-2-1-1-0
	16	64/66b	16.25 ⁽¹⁾	8-4-1-1-0	4-2-1-1-0
	16	8/10b	20	8-4-2-2-0	4-4-2-2-0
	16	64/66b	16.25 ⁽¹⁾	8-4-2-2-0	4-4-2-2-0
3000	16	8/10b	29.5 ⁽²⁾	8-4-1-1-0	4-2-1-1-0
	16	64/66b	24.75	8-4-1-1-0	4-2-1-1-0
	16	8/10b	29.5 ⁽²⁾	8-4-2-2-0	4-2-2-2-0
	16	64/66b	24.75	8-4-2-2-0	4-2-2-2-0

- (1) The input rate is limited to 0.985x the stated input rate due to the serdes PLL frequency limitation for baud rates between 16.25 and 19GHz
- (2) The input rate is limited to 0.983x the stated input rate due to the maximum baud rate of 29.5Gbps

Table 8-15. JESD204B/C Formats for 2 DUCs per TX Chain

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
125	16	8/10b	20	2-16-16-1-0	1-8-16-1-0
	16	8/10b	10	4-16-8-1-0	2-8-8-1-0
	16	64/66b	16.25 ⁽¹⁾	2-16-16-1-0	1-8-16-1-0
	16	64/66b	8.25	4-16-8-1-0	2-8-8-1-0
187.5	16	8/10b	29.5 ⁽²⁾	2-16-16-1-0	1-8-16-1-0
	16	8/10b	15	4-16-8-1-0	2-8-8-1-0
	16	8/10b	7.5	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.75	2-16-16-1-0	1-8-16-1-0
	16	64/66b	12.375	4-16-8-1-0	2-8-8-1-0
	16	64/66b	6.25	8-16-4-1-0	4-8-4-1-0
250	16	8/10b	20	4-16-8-1-0	2-8-8-1-0
	16	8/10b	10	8-16-4-1-0	4-8-4-1-0
	16	64/66b	16.25 ⁽¹⁾	4-16-8-1-0	2-8-8-1-0
	16	64/66b	8.125 ⁽¹⁾	8-16-4-1-0	4-8-4-1-0
375	16	8/10b	29.5 ⁽²⁾	4-16-8-1-0	2-8-8-1-0
	16	8/10b	15	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.75	4-16-8-1-0	2-8-8-1-0
	16	64/66b	12.375	8-16-4-1-0	4-8-4-1-0

Table 8-15. JESD204B/C Formats for 2 DUCs per TX Chain (continued)

INPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
500	16	8/10b	20	8-16-4-1-0	4-8-4-1-0
	16	64/66b	16.25 ⁽¹⁾	8-16-4-1-0	4-8-4-1-0
	12	8/10b	29.5 ⁽²⁾	4-16-6-1-0	2-8-6-1-0
	12	8/10b	15	8-16-3-1-0	4-8-3-1-0
	12	64/66b	24.75	4-16-6-1-0	2-8-6-1-0
	12	64/66b	12.375	8-16-3-1-0	4-8-3-1-0
	24	64/66b	24.75	8-16-3-1-0	
750	16	8/10b	29.5 ⁽²⁾	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.75	8-16-4-1-0	4-8-4-1-0

(1) The input rate is limited to 0.985x the stated input rate due to the serdes PLL frequency limitation for baud rates between 16.25 and 19GHz

(2) The input rate is limited to 0.983x the stated input rate due to the maximum baud rate of 29.5Gbps

8.3.9.3.2 JESD204B/C Frame Assembly for Receiver Chains

The AFE7900 receiver chains support multiple JESD modes, listed in the following [Table 8-16](#) for 1 DDC per RX and [Table 8-17](#) for 2 DDCs per RX. For each of the supported output rates, all possible LMFSHd as single or dual links are listed with the associated SERDES RATES, for both 8b/10b and 64b/66b encoding.

Table 8-16. JESD204B/C Formats for 1 DDC per RX Chain (4 RX)

OUTPUT RATE [MSPS]	OUTPUT RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
62.5	16	8/10b	20	1-8-32-1-0	
	16	8/10b	10	1-8-16-1-0	
	16	8/10b	5	2-8-8-1-0	1-4-8-1-0
	24	8/10b	15	1-8-24-1-0	
	24	8/10b	7.5	2-8-12-1-0	1-4-12-1-0
	24	64/66b	12.375	1-8-24-1-0	
93.75	16	8/10b	15	1-8-16-1-0	
	16	8/10b	7.5	2-8-8-1-0	1-4-8-1-0
	16	64/66b	12.375	1-8-16-1-0	
	24	8/10b	11.25	2-8-12-1-0	1-4-12-1-0
125	16	8/10b	5	4-8-8-1-0	2-4-4-1-0
	16	8/10b	10	2-8-8-1-0	1-4-8-1-0
	16	64/66b	8.125 ⁽¹⁾	2-8-8-1-0	1-4-8-1-0
187.5	16	8/10b	29.5 ⁽²⁾	1-8-16-1-0	
	16	8/10b	15	2-8-8-1-0	1-4-8-1-0
	16	64/66b	24.75	1-8-16-1-0	
	16	64/66b	12.375	2-8-8-1-0	1-4-8-1-0
	12	8/10b	22.5	1-8-12-1-0	
	12	8/10b	11.25	2-8-6-1-0	1-4-6-1-0

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Table 8-16. JESD204B/C Formats for 1 DDC per RX Chain (4 RX) (continued)

OUTPUT RATE [MSPS]	OUTPUT RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
250	16	8/10b	20	2-8-8-1-0	1-4-8-1-0
	16	8/10b	10	4-8-4-1-0	2-4-4-1-0
	16	64/66b	16.25 ⁽¹⁾	2-8-8-1-0	1-4-8-1-0
	16	64/66b	8.25	4-8-4-1-0	2-4-4-1-0
	12	8/10b	29.5 ⁽²⁾	1-8-12-1-0	
	12	8/10b	15	2-8-6-1-0	1-4-6-1-0
	12	64/66b	12.375	2-8-6-1-0	1-4-6-1-0
	12	8/10b	7.5	4-8-3-1-0	2-4-3-1-0
	12	64/66b	24.75	1-8-12-1-0	
	24	8/10b	15	4-8-6-1-0	2-4-6-1-0
	24	64/66b	24.75	2-8-12-1-0	1-4-12-1-0
375	16	8/10b	29.5 ⁽²⁾	2-8-8-1-0	1-4-8-1-0
	16	8/10b	15	4-8-4-1-0	2-4-4-1-0
	16	8/10b	7.5	8-8-2-1-0	4-4-2-1-0
	16	64/66b	24.75	2-8-8-1-0	1-4-8-1-0
	16	64/66b	12.375	4-8-4-1-0	2-4-4-1-0
	16	64/66b	6.25	8-8-2-1-0	4-4-2-1-0
	16	8/10b	22.5	2-8-6-1-0	1-4-3-1-0
	16	8/10b	11.25	4-8-3-1-0	2-4-3-1-0
500	16	8/10b	20	4-8-4-1-0	2-4-4-1-0
	16	8/10b	10	8-8-2-1-0	4-4-2-1-0
	16	64/66b	16.25 ⁽¹⁾	4-8-4-1-0	2-4-4-1-0
	12	8/10b	29.5 ⁽²⁾	2-8-6-1-0	1-4-3-1-0
	12	8/10b	15	4-8-3-1-0	2-4-3-1-0
	12	8/10b	7.5	8-8-3-2-0	4-4-3-2-0
	12	64/66b	24.75	2-8-6-1-0	1-4-3-1-0
	12	64/66b	12.375	4-8-3-1-0	2-4-3-1-0
	12	8/10b	15	4-8-3-1-0	2-4-3-1-0
	24	8/10b	15	8-8-3-1-0	4-4-3-1-0
	24	64/66b	24.75	4-8-6-1-0	2-8-6-1-0
750	16	8/10b	29.5 ⁽²⁾	4-8-4-1-0	2-4-4-1-0
	16	8/10b	15	8-8-2-1-0	4-4-2-1-0
	16	64/66b	24.75	4-8-4-1-0	2-4-4-1-0
	16	64/66b	24.75	4-8-8-2-0	2-4-8-2-0
	16	64/66b	12.375	8-8-2-1-0	4-4-2-1-0
	12	8/10b	24.75	4-8-3-1-0	2-4-3-1-0
	12	8/10b	12.375	8-8-3-2-0	4-4-3-2-0
1000	16	8/10b	20	8-8-2-1-0	4-4-2-1-0
	16	64/66b	16.25 ⁽¹⁾	8-8-2-1-0	4-4-2-1-0
	12	8/10b	29.5 ⁽²⁾	4-8-3-1-0	2-4-3-1-0
	12	8/10b	15	8-8-3-2-0	4-4-3-2-0
	12	64/66b	24.75	4-8-3-1-0	2-4-3-1-0
	12	64/66b	12.375	8-8-3-2-0	4-4-3-2-0

Table 8-16. JESD204B/C Formats for 1 DDC per RX Chain (4 RX) (continued)

OUTPUT RATE [MSPS]	OUTPUT RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
1500	16	8/10b	29.5 ⁽²⁾	8-8-2-1-0	4-4-2-1-0
	16	64/66b	24.75	8-8-2-1-0	4-4-2-1-0
	12	8/10b	22.5	8-8-3-2-0	4-4-3-2-0

- (1) The output rate is limited to 0.985x the stated input rate due to the serdes PLL frequency limitation for baud rates between 16.25 and 19GHz
- (2) The output rate is limited to 0.983x the stated input rate due to the maximum baud rate of 29.5Gbps

Table 8-17. JESD204B/C Formats For 2 DDCs per RX Chain

OUTPUT RATE [MSPS]	OUTPUT RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS
62.5	16	8/10b	20	1-16-32-1-0	
	16	64/66b	16.25 ⁽¹⁾	1-16-32-1-0	
	16	8/10b	10	2-16-16-1-0	1-8-16-1-0
	16	64/66b	8.125 ⁽¹⁾	2-16-16-1-0	1-8-16-1-0
	24	8/10b	15	2-16-24-1-0	1-8-24-1-0
	24	64/66b	12.375	2-16-24-1-0	1-8-24-1-0
93.75	16	8/10b	15	2-16-16-1-0	1-8-16-1-0
	16	64/66b	12.375	2-16-16-1-0	1-8-16-1-0
	16	64/66b	24.75	1-16-32-1-0	
	24	8/10b	22.5	2-16-24-1-0	1-8-24-1-0
125	16	8/10b	20	2-16-16-1-0	1-8-16-1-0
	16	8/10b	10	4-16-8-1-0	2-8-8-1-0
	16	64/66b	16.25 ⁽¹⁾	2-16-16-1-0	1-8-16-1-0
	16	64/66b	8.125 ⁽¹⁾	4-16-8-1-0	2-8-8-1-0
	24	64/66b	24.75	2-16-24-1-0	1-16-24-1-0
187.5	16	8/10b	29.5 ⁽²⁾	2-16-16-1-0	1-8-16-1-0
	16	8/10b	15	4-16-8-1-0	2-8-8-1-0
	16	64/66b	24.75	2-16-16-1-0	1-8-16-1-0
	16	64/66b	12.375	4-16-8-1-0	2-8-8-1-0
250	16	8/10b	20	4-16-8-1-0	2-8-8-1-0
	16	8/10b	10	8-16-4-1-0	4-8-4-1-0
	16	64/66b	16.25 ⁽¹⁾	4-16-8-1-0	2-8-8-1-0
	16	64/66b	8.125 ⁽¹⁾	8-16-4-1-0	4-8-4-1-0
	12	64/66b	24.75	2-16-6-1-0	1-8-6-1-0
	12	64/66b	12.375	4-16-6-1-0	2-8-6-1-0
	24	64/66b	24.75	4-16-6-1-0	2-8-6-1-0
375	16	8/10b	29.5 ⁽²⁾	4-16-8-1-0	2-8-8-1-0
	16	8/10b	15	8-16-4-1-0	4-8-4-1-0
	16	64/66b	24.75	4-16-8-1-0	2-8-8-1-0
	16	64/66b	12.375	8-16-4-1-0	4-8-4-1-0

- (1) The output rate is limited to 0.985x the stated input rate due to the serdes PLL frequency limitation for baud rates between 16.25 and 19GHz
- (2) The output rate is limited to 0.983x the stated input rate due to the maximum baud rate of 29.5Gbps

8.3.9.3.2.1 JESD204B/C Frame Assembly for Feedback Chain

The feedback chains support multiple JESD204B/C modes, listed in [Table 8-18](#).

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Table 8-18. JESD204B/C Formats for Feedback Chain

OUTPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	PAIRED RX JESD MODE FOR SHARED SERDES	
						L-M-F-S-Hd	OUTPUT RATE
125	12	8/10b	7.5	1-4-6-1-0			
	16	8/10b	10	1-4-8-1-0			
	16	8/10b	10	1-4-16-2-0		1-8-16-1-0	62.5
	32	8/10b	20	1-4-16-1-0			
	32	64/66b	16.25 ⁽¹⁾	1-4-16-1-0			
	16	64/66b	8.125 ⁽¹⁾	1-4-8-1-0			
	24	8/10b	15	1-4-12-1-0			
	24	64/66b	12.375	1-4-12-1-0			
187.5	12	8/10b	11.25	1-4-6-1-0			
	16	8/10b	15	1-4-8-1-0			
	16	8/10b	7.5	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	7.5	2-4-8-2-0		2-8-8-1-0	93.75
	16	64/66b	12.375	1-4-8-1-0			
	16	8/10b	15	1-4-16-2-0		1-8-16-1-0	93.75
	24	8/10b	22.5	1-4-12-1-0			
	24	8/10b	11.25	2-4-6-1-0	1-2-6-1-0		
250	12	64/66b	16.25 ⁽¹⁾	1-4-12-1-0			
	16	8/10b	20	1-4-8-1-0			
	16	8/10b	20	1-4-16-2-0		2-16-16-1-0	125
	16	8/10b	10	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	10	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	125
	16	64/66b	16.25 ⁽¹⁾	1-4-8-1-0			
	16	64/66b	16.25 ⁽¹⁾	1-4-16-2-0		2-16-16-1-0	125
	16	64/66b	8.125 ⁽¹⁾	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	8.125 ⁽¹⁾	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	125
	24	64/66b	24.75	1-4-24-2-0		2-16-24-1-0	125
375	16	8/10b	29.5 ⁽²⁾	1-4-8-1-0			
	16	8/10b	29.5 ⁽²⁾	1-4-16-2-0		1-8-16-1-0	187.5
						2-16-16-1-0	187.5
	16	8/10b	15	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	15	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	187.5
						4-16-8-1-0	187.5
	16	8/10b	7.5	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	7.5	4-4-4-2-0	2-2-4-2-0		
	16	64/66b	24.75	1-4-8-1-0			
	16	64/66b	24.75	1-4-16-2-0		1-8-16-1-0	187.5
						2-16-16-1-0	187.5
	16	64/66b	12.375	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	12.375	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	187.5
						4-16-8-1-0	187.5
	16	64/66b	6.25	4-4-2-1-0	2-2-2-1-0		
	16	64/66b	6.25	4-4-4-2-0	2-2-4-2-0		
	32	64/66b	24.75	2-4-16-2-0	1-2-16-2-0	1-8-16-1-0	187.5
						2-16-16-1-0	187.5

Table 8-18. JESD204B/C Formats for Feedback Chain (continued)

OUTPUT RATE [MSPS]	RESOLUTION	ENCODING	SERDES RATE [Gbps]	L-M-F-S-Hd 1 LINK	L-M-F-S-Hd 2 LINKS	PAIRED RX JESD MODE FOR SHARED SERDES	
						L-M-F-S-Hd	OUTPUT RATE
500	16	8/10b	20	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	20	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	250
						4-16-8-1-0	250
	16	8/10b	10	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	10	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	250
						8-16-4-1-0	250
	16	64/66b	16.25 ⁽¹⁾	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	16.25 ⁽¹⁾	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	250
						4-16-8-1-0	250
750	16	8/10b	29.5 ⁽²⁾	2-4-4-1-0	1-2-4-1-0		
	16	8/10b	29.5 ⁽²⁾	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	375
						4-16-8-1-0	375
	16	8/10b	15	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	15	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	375
						8-16-4-1-0	375
	16	64/66b	24.75	2-4-4-1-0	1-2-4-1-0		
	16	64/66b	24.75	2-4-8-2-0	1-2-8-2-0	2-8-8-1-0	375
						4-16-8-1-0	375
1000	16	8/10b	20	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	20	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	500
	16	8/10b	10	8-4-1-1-0	4-2-1-1-0		
	16	8/10b	10	8-4-2-2-0	4-2-2-2-0	8-8-2-1-0	500
	16	64/66b	16.25 ⁽¹⁾	4-4-2-1-0	2-2-2-1-0		
	16	64/66b	16.25 ⁽¹⁾	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	500
	16	64/66b	8.125 ⁽¹⁾	8-4-1-1-0	4-2-1-1-0		
	16	64/66b	8.125 ⁽¹⁾	8-4-2-2-0	4-2-2-2-0		
	12	8/10b	29.5 ⁽²⁾	2-4-6-1-0	1-2-6-1-0	2-8-6-1-0	500
						4-8-6-1-0	500
	12	8/10b	15	4-4-3-1-0	2-2-3-1-0		
	12	64/66b	24.75	2-4-6-1-0	1-2-6-1-0	2-8-6-1-0	500
						4-8-6-1-0	500
	12	64/66b	12.375	4-4-3-1-0	2-2-3-1-0		
	24	64/66b	24.75	4-4-6-2-0	2-2-6-2-0	2-8-6-1-0	500
						4-8-6-1-0	500
1500	16	8/10b	29.5 ⁽²⁾	4-4-2-1-0	2-2-2-1-0		
	16	8/10b	15	8-4-2-1-0	4-2-2-1-0	8-8-2-1-0	750
	16	64/66b	24.75	4-4-4-2-0	2-2-4-2-0	4-8-4-1-0	750
	16	64/66b	12.375	8-4-2-1-0	4-2-2-1-0	8-8-2-1-0	750
	12	8/10b	22.5	4-4-3-1-0	2-2-3-1-0		

(1) The input rate is limited to 0.985x the stated input rate due to the serdes PLL frequency limitation for baud rates between 16.25 and 19GHz

(2) The input rate is limited to 0.983x the stated input rate due to the maximum baud rate of 29.5Gbps

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8.3.10 Sharing SerDes Lanes

For base stations operating in TDD modes, downlink and uplink time-share the same frequency band. During the downlink slot, transmitters are active often along with feedback observation receivers (FB) to monitor the TX output for various purposes (ex: to assist the Digital Pre-distortion algorithm for Power Amplifier linearization). In uplink time slots transmitters along with the feedback observation receivers are typically inactive, and traffic receivers (RX) are active. AFE7900 supports the timesharing of same SerDes TX lanes between the RX and FB chains to optimize the use of the SerDes lanes and the power consumption of the device. This mode is enabled through the SPI. Then the dynamic switching between the RX chains and the FB path connection to the shared SerDes lanes is controlled using the RX and FB enable GPIO pins according to [Table 8-19](#).

Table 8-19. RX/FB SerDes Sharing Switch Control

RXEN1/2 ^(b)	1FBEN	RX CHAINS	FB CHAIN	SerDes LANES TO
1	0	On	Off	RX
0	1	Off	On	FB
1	1	On/Off	On/Off	RX/FB ^(a)
0	0	Off	Off	

(a) (1,1) case same as (1,0) or (0,1) based on a programmable configuration

(b) Possible to select through the SPI which RXEN to use

8.3.11 Low-Speed Digital I/O Configuration

The AFE7900 supports multiple modes where controls and data exchange happen through several allocated Low-Speed Digital I/O (GPIO) pins. Because the required I/Os by all supported modes exceeds the number of available pins, there are several pins that can be configured differently based on the active mode. All the allocated pins for low-speed I/O (GPIO) are shown in the ballmap (see [Section 6](#)).

The AFE7900 supports flexible assignment of the GPIO functions to GPIO balls. However, some functions are fixed to certain balls, and other functions are only recommended and specified for certain balls [Table 8-20](#).

Table 8-20. Fixed and Recommended GPIO Functions

TYPE	FUNCTION	BALL NAMES
Fixed	JTAG	GTR_13_TRST
		GTR_18_TDI
		GTR_4_TCLK
		GTR_5_TDO
		GTR_10_TMS
		GTL_10_BIST0
		GTL_12_BIST1
	SPI A	GTL_17_SPIASDIO
		GTL_18_SPIASDO
		GTL_4_SPIACLK
		GTL_5_SPIASEN
Recommended	SPI B1	GTR_11_SPIB1_SDO
		GTR_12_SPIB1_SDIO
		GTR_14_SPIB1SEN
		GTR_17_SPIB1CLK
	SPI B2	GTR_2_SPIB2CLK
		GTR_6_SPIB2_SDIO
		GTR_7_SPIB2SEN
		GTR_9_SPIB2SDO

The GPIO functions supported by the device are listed in [Table 8-21](#).

Table 8-21. GPIO Functions

FUNCTION	# OF BALLS
Default (functions available after chip reset)	
JTAG	5 total (plus BIST0 and BIST1)
SPI A, SPI B1, SPI B2	12 total, 4 each
TDD switches	10 total, 4 each for TX, RX and 2 for FB
LNA Bypass	4 total, 1 each for each RX
Reset	1
JESD SYNC\ In	4 total, 2 x differential or 4x single ended
JESD SYNC\ Out	4 total, 2 x differential or 4x single ended
Other Available Functions	
Internal DSA control	12 total, 3 per RX
External DVGA control	6 total, 3 per RX 1/2 and 3/4
AGC Freeze	4 total, 1 per RX
NCO Select	10 total, 1 per TX, RX and FB
RX Peak Detectors	16 total, 4 per RX
RX Reliability Detectors	8 total, 2 per RX
DSA Swap	1 per TX, 1 per RX, 1 per FB

8.3.12 Available Alarms

Several alarms from different blocks can be enabled and monitored by AFE7900. Some of them can be configured to trigger the PA protection feature ([Section 8.3.3.1.2.1](#)) and or generate an interrupt signal. The device has two interrupt pins (INT1 and INT2). Through the SPI it is possible to configure which alarms can trigger the interrupt signal on each of the two pins. The list of all alarms available in the device is included in the following table.

Table 8-22. Alarm List

ALARM	BLOCK	NOTES
SerDes PLL unlock	SerDes	SerDes PLL becomes unlocked. One per SerDes block (group of four transceivers)
Loss of signal detection	SerDes	SerDes doesn't detect any more signal transition
Frame Sync Error	JESD204B	Ctrl-K in middle of data
Multiframe alignment error	JESD204B	Failure in multi-frame alignment
Frame alignment error	JESD204B	Failure in frame alignment
Link configuration error	JESD204B	Wrong link configuration
Elastic buffer match error	JESD204B	First non-/K/ doesn't match the programmed data
Code synchronization error	JESD204B	
8b/10b not-in-table code error	JESD204B	
8b/10b disparity error	JESD204B	
Frame sync error	JESD204B	a /K/ symbol is detect while receiving data (8b/10b encoding)
Short pattern check	JESD204B	short pattern test fails.
Elastic buffer overflow	JESD204B/C	Bad RBD value
Frame Sync Error	JESD204C	Fixed ones error
Invalid SYNC Header	JESD204C	Wrong header is detected - '11' or '00'
CRC error	JESD204C	Error detected in the supported CRC3 or CRC12
EoEMB error	JESD204C	Wrong End of Extended Multi-Bock detected
EoMB error	JESD204C	Wrong End of Multi-Bock detected
CMD data not matching SPI register	JESD204C	cmd-data in CRC mode not matching with spi register bits
Header Parity Check	JESD204C	Parity error detected

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Table 8-22. Alarm List (continued)

ALARM	BLOCK	NOTES
PLL unlock	PLL	Separate lock detect alarms for each RF and DC PLL
SPI conflict	SPI	Register access conflict between the two SPI
TX digital chain FIFO overflow	TX dig block	One FIFO overflow alarm for each of TX digital chain
RX digital chain FIFO overflow	RX dig block	One FIFO overflow alarm for each of RX digital chain
FB digital chain FIFO overflow	FB dig block	One FIFO overflow alarm for each of FB digital chain
Macro Complete	SPI	Macro execution is completed
Macro error	SPI	Macro terminated with an error
Input Signal Error	PAP block	Trigger from incoming signal measurements (average power or programmable filter power; see Section 8.3.3.1.2)

8.3.13 TX and RX DSA Gain and Phase Error Calibration

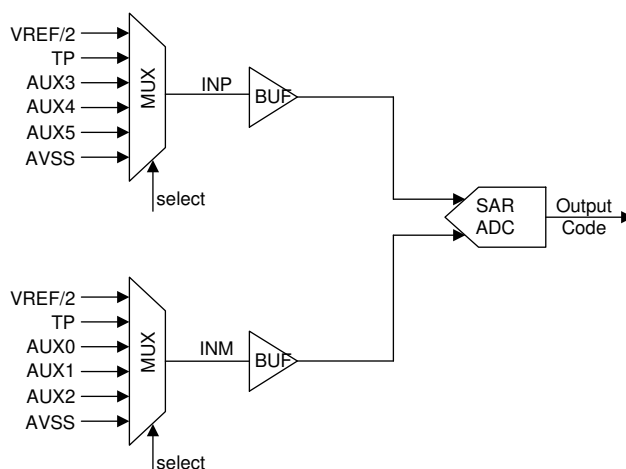
The AFE7900 TX DSA steps mismatch in amplitude and phase can be compensated through a dedicated calibration procedure. Such calibration should be performed once for each device on the final assembled board, because the actual source and load impedance seen by the device can affect the phase and amplitude mismatch. TI suggests to perform this calibration on the final assembled board at the customer factory for this reason.

The AFE7900, during the calibration, computes and stores internally the gain and phase compensation parameters for all the 4 TX and 4 RX chains. At the end of calibration procedure, the host needs to read the calibration tables from the device internal memory and store in a non-volatile memory. The estimated calibration data packet size for 4 RX channels is approximately 1000 bytes, while the estimated calibration data packet size for four TX channels is approximately 800 bytes.

When the device is used in normal mode, during the configuration, the host has to download the calibrations tables into the AFE7900 internal memory. These tables will then be used by the device to compensate the gain/phase errors of the DSA steps.

8.3.14 Auxiliary Low-Speed ADC

The device integrates a 12-bit, 200-ksps differential SAR ADC to enable the monitoring of external DC or low-speed signals. The ADC inputs are multiplexed to 6 pins on the package, to allow the measurements of multiple signals. The digital output words are accessed through the SPI.

**Figure 8-107. Auxiliary ADC Block Diagram**

As shown in the block diagram, the differential ADC inputs can be connected through a multiplex to:

- the 6 package pins indicated as *_AUX0 through *_AUX5;
- $V_{REF}/2$ or
- Ground (AVSS).

$V_{REF}/2$, $AVSS$ and TP are internal connections (TP are internal test points for debugging). V_{REF} is typically 1.4 V and it is generated internally. The SAR ADC samples the signals at its differential inputs. As such, by the correct configuration of the multiplex, it is possible to measure the level at any of the AUX input pins with reference to $V_{REF}/2$, ground or another AUX input. The ADC output code word is related to the input voltages by the following formula:

$$\frac{V_{INP} - V_{INM}}{V_{REF}} = \frac{2 * code + 1 - 4096}{4096} \quad (3)$$

The following 3 plots show the expected output code as function of the input voltage in 3 different measurement modes: differential, single-ended with other side connected to $V_{REF}/2$; single-ended with the other side connected to ground.

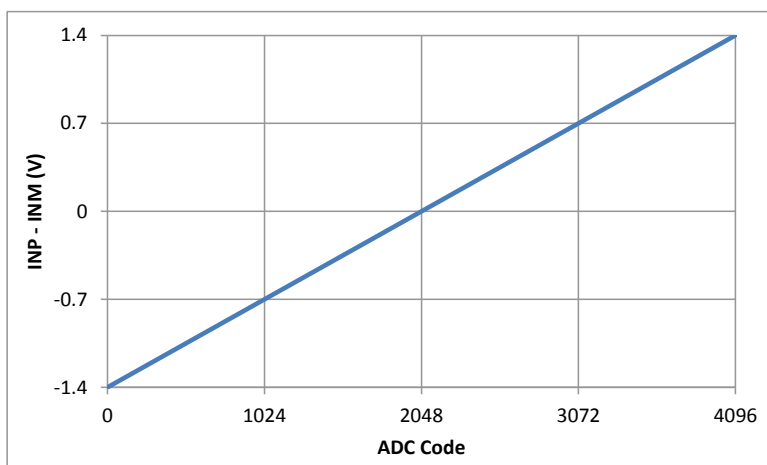


Figure 8-108. Input Differential Voltage vs Auxiliary ADC Output Code

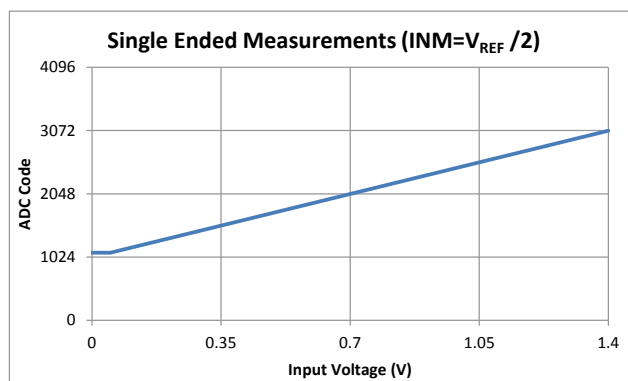
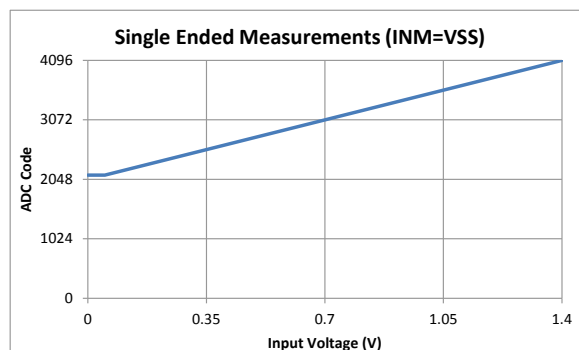


Figure 8-109. Auxiliary ADC Output Code vs Single-Ended Input ($V_{REF}/2$ Reference)

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**Figure 8-110. Auxiliary ADC Output Code vs Single-Ended Input (Ground Reference)****8.3.15 Temperature Sensor**

The device incorporates a temperature sensor block which monitors the die temperature by measuring the voltage across two transistors. The voltage is converted to an 8-bit digital word using a successive approximation (SAR) analog to digital conversion process. The result is scaled, limited and formatted as a two's complement value representing the temperature in degrees Celsius.

The temperature sensor is not calibrated and can have an error of 10-20 degrees Celsius device to device. It is useful for relative measurements between operation modes. For example, in a low power sleep mode of operation, the die temperature should be close to the device package temperature, and can be used as a baseline to improve the absolute temperature accuracy by providing a temperature offset for use in other conditions.

8.3.16 Serial Peripheral Interface (SPI)

The serial port of the AFE7900 is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of the device. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 terminal interface through register field GLOBAL_4PIN in global register GLOBAL0. In both configurations, SCLK is the serial interface input clock and SDEN\ is serial interface enable. For 3 terminal configuration, SDIO is a bidirectional terminal for both data in and data out. For 4 terminal configuration, SDIO is bidirectional and SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of SCLK. The SPI registers except for global register GLOBAL0 and GLOBAL1 are reset by writing a "1" to GLOBAL_SOFT_RESET in the global register GLOBAL0.

Each read/write operation is framed by signal SDEN\ (Serial Data Enable Bar) asserted low. The first two bytes is the instruction cycle which identifies the following data transfer cycle as read or write as well as the 15-bit address to be accessed. The data transfer cycle consists of one byte. There are 64 pages of registers in the device and address 0x00h-0x1Fh are assigned for global registers in every page. The particular register page is selected by writing "1" to the corresponding page selection bits through field GLOBAL_PAGE_SEL in the global register GLOBAL_PAGE_SEL0-GLOBAL_PAGE_SEL7 (address 0x10h-0x15h).

The AFE7900 includes two additional SPI interfaces (SPIB1, SPIB2)) with identical functions as the main SPI. The three SPIs can be accessed simultaneously as long as the accessed registers are not in the same page. Both main SPI and SPI-B1/2 also support streaming reads/writes and broadcasting as shown below. The address automatically increments or decrements depends on the setting of register field GLOBAL_ASCEND. The streaming addressing formation depends on the setting of register field GLOBAL_ADDRESSING_TYPE. [Figure 8-111](#) and [Figure 8-112](#) show the timing of a regular SPI write and read cycle. [Figure 8-113](#) and [Figure 8-114](#) show an example of SPI streaming write and read. [Figure 8-115](#) and [Figure 8-116](#) show the timing diagram of SPI write and read.

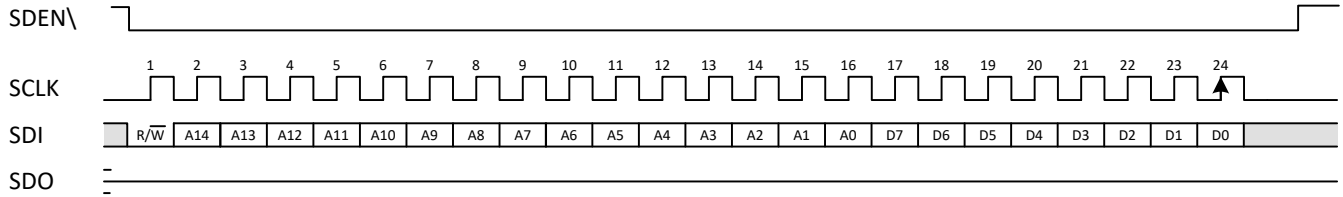


Figure 8-111. SPI Write Bus Cycle

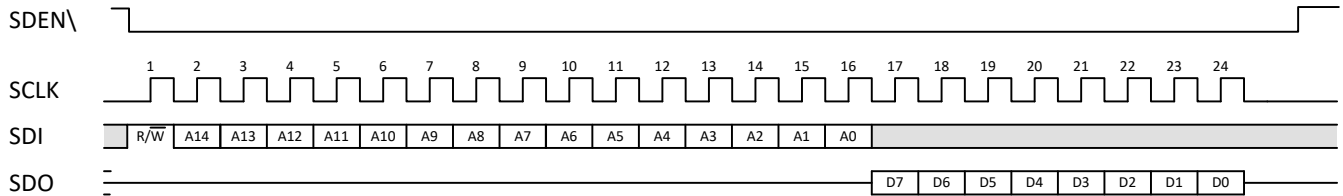


Figure 8-112. SPI Read Bus Cycle

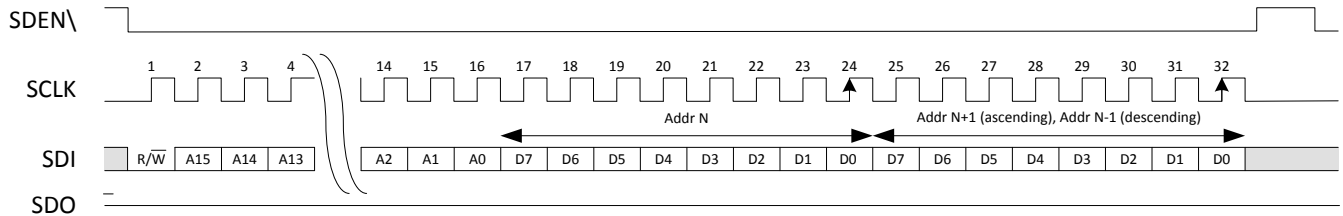


Figure 8-113. SPI Streaming Write Example

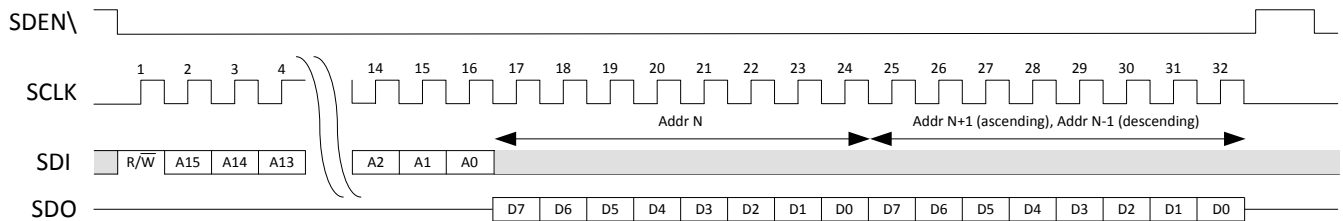


Figure 8-114. SPI Streaming Read Example

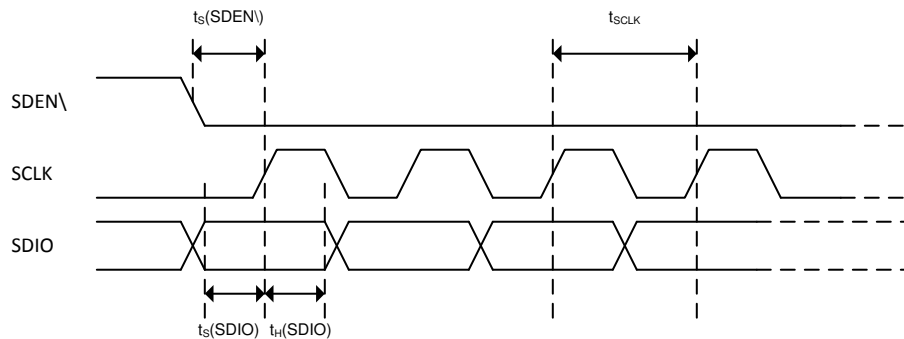


Figure 8-115. SPI Write Timing Diagram

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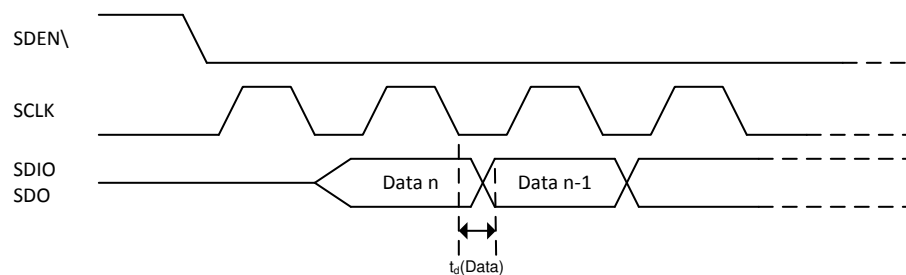


Figure 8-116. SPI Read Timing Diagram

8.4 Device Functional Modes

The AFE7900 supports very flexible configuration on the device functional modes. Each 2T2R1F half of the device can be configured independently. Each transmitter and receiver can work in Active Mode, Standby Mode, or Sleep Mode. With the transmitter and receiver in different operating modes, the whole device can operate at various functional modes:

- TDD mode with shared RX/FB ADCs and dynamic switching
- Transmitter only mode
- Receiver only mode

Note that all the above functional modes are configured separated for each 2T2R or 2T2R1F group. The status between standby and active for the TX/FB and RX channels are controlled by up to 10 GPIO functions, one per TX (TXTDDn, n = 1-4), RX (RXTDDn, n = 1-4) and FB (FBTDDn, n = 1-2) channels.

8.4.1 TDD Mode With Shared RX/FB ADCs and Dynamic Switching

In this mode, the RX and FB share the RX ADC and switches between the RX and FB DDCs using the TXTDDn, RXTDDn, and FBTDDn GPIO functions. It is also possible that both RX and FB are in standby states to save power if the FB channel is not needed.

8.4.2 Transmitter Only Mode

In this mode, only the transmitter channels are in Active mode. The receivers can be put in standby mode by simply setting GPIO functions RXTDDn and FBTDDn to 0. It is also possible to set the transmitter and feedback chains in Standby mode or through off-state programming the dedicated internal registers in the SPI.

8.4.3 Receiver Only Mode

In this mode, only the receiver and feedback channels are in Active mode. The transmitter channels can be put in standby mode by simply setting GPIO functions TXTDDn to 0. It is also possible to set the transmitter and feedback chains in Standby mode or through off-state programming the dedicated internal registers in the SPI.

8.5 Programming

The AFE7900 software interaction is primarily an initial configuration, based on registers access through the SPI. The device is configured through the SPI using a combination of direct register reads/writes for simple configurations and register writes to initiate macros.

Macro commands abstract out the internal device configuration sequence to a simple set of configuration and simplify the host interaction. They reduce complex configurations into simple writes, avoid computation complexity on the host side, and provide simple status information in response.

9 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The AFE7900 is a highly integrated and flexible RF transceiver, which can be used by the customers in multiple use cases and modes of operation.

9.2 Typical Application

9.2.1 4T4R S-Band Radar Transceiver

9.2.1.1 System Schematic

[Figure 9-1](#) shows a system block diagram for the device when used as a S-band radar transceiver. Each of four antennas is connected to a AFE7900 TX path and RX path through a circulator to prevent the TX output from connecting directly to the RX path. The AFE7900 TX output has one or more amplifier stages to increase the TX output power at the antenna. The RX path has a low noise amplifier (LNA) to reduce the system noise figure contribution of the AFE7900 and a Nyquist filter to suppress noise and energy of out of band signals picked up by the antenna.

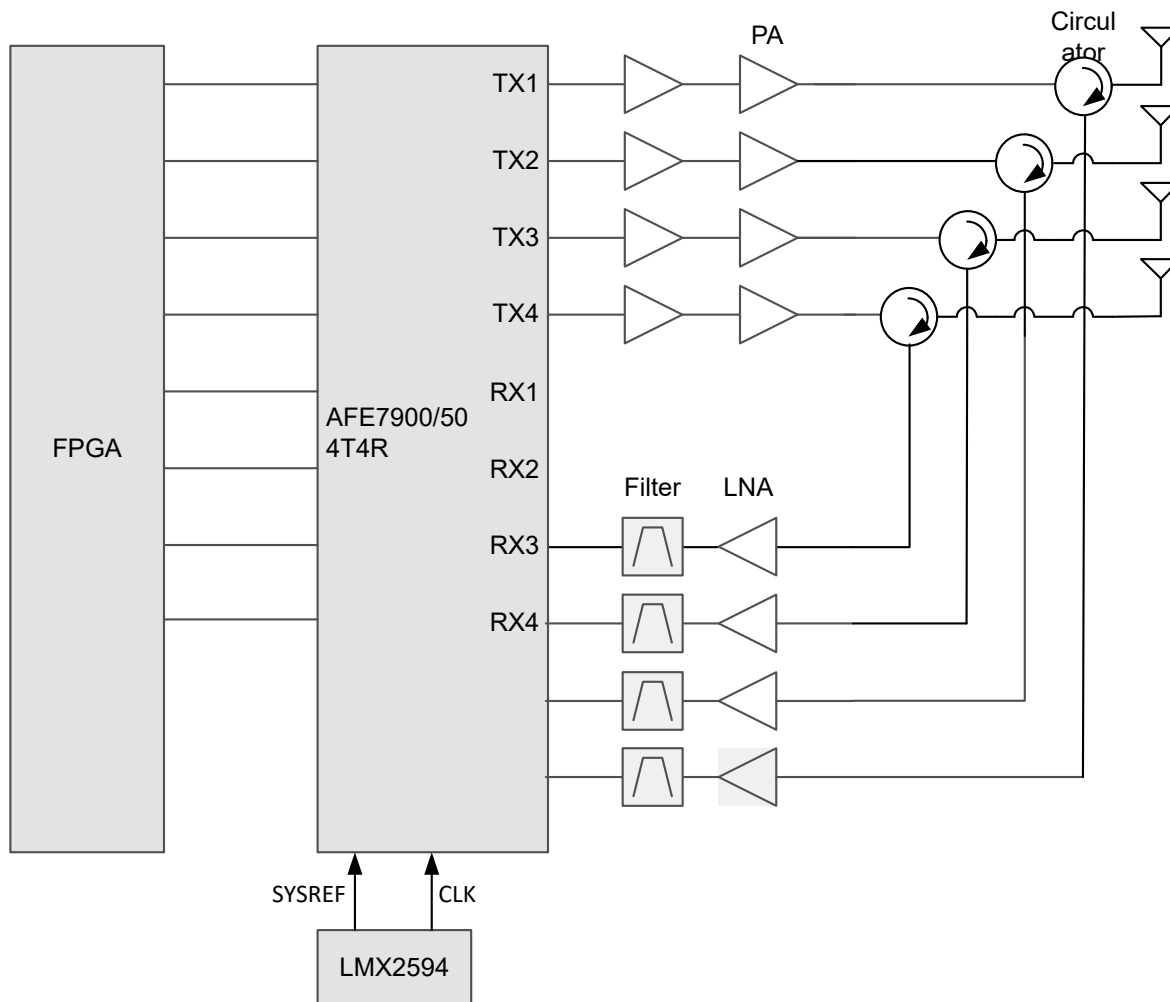


Figure 9-1. 4T4R Radar Transceiver

9.2.1.2 Design Requirements

S-band covers a frequency range of 2GHz to 4GHz. With an ADC sample rate of 3GSPS, the AFE7900 can cover 2GHz to 3GHz in 2nd Nyquist zone and 3GHz to 4GHz in 3rd Nyquist zone. The AFE7900 RX supports a maximum of 1.2GHz of signal bandwidth in decimate by 2 mode, but typical S-band radars have at most a few 100MHz BW. For this example, we will consider a radar with signal bandwidth of 300MHz and a center frequency of 3.7GHz.

Doppler radars use the frequency shift in the returned signal to measure the velocity of object. Large reflected signals from for example ground clutter mix with the TX and RX phase noise, which can potentially swamp the return signal from a small moving object. This places a requirement on close in phase noise for the TX DAC and RX ADC clock.

Radars are also sensitive to spurious returned signals, and for this example we assume 85dBFS is required for the RX SFDR.

9.2.1.3 Detailed Design Procedure

To maximize the offset between the TX output signal in 1st Nyquist and it's image in 2nd Nyquist to ease filtering, a DAC sample rate of 12GSPS is chosen. To minimize the clock phase noise, an external clock source at 12GHz with very low phase noise is used rather than the AFE7900's internal PLL/VCO.

A TX input sample rate of 375MSPS covers the 300MHz signal bandwidth, and interpolation by 32x is used to increase the TX sample rate to 12GSPS. The AFE7900 numerically controlled oscillator (NCO) is used to place

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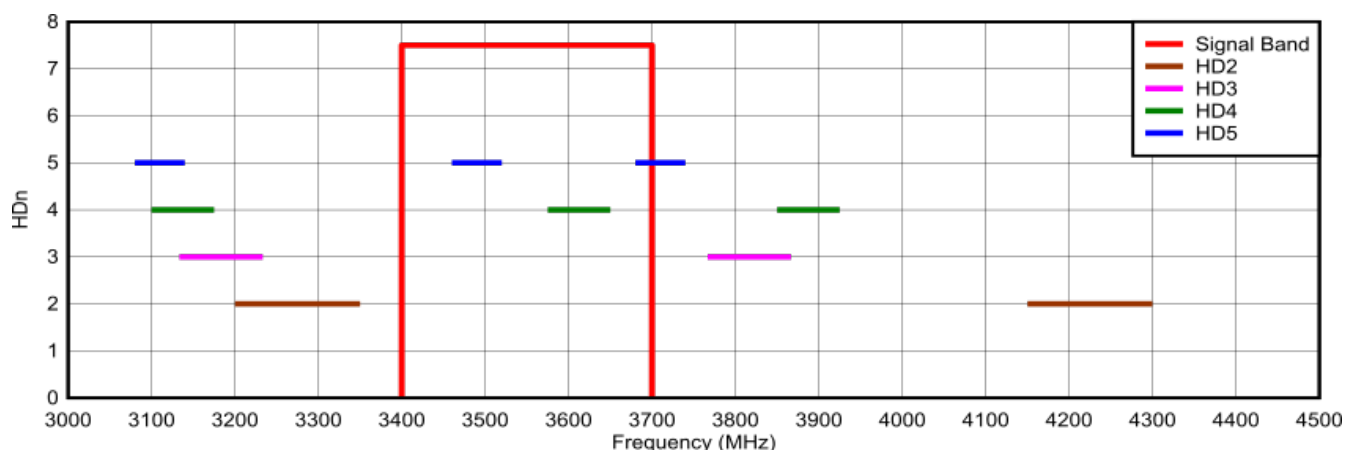
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the signal at the TX output at 3.7GHz. An ADC sample rate of 3GSPS is used, $1/4^{\text{th}}$ of the DAC sample rate. The RX NCO downconverts the RX signal to 0Hz and the sample rate is decimated by 8x to 375MSPS for the RX output.

For this example, a circulator with 0.25dB insertion loss is assumed. For the RX path, a QMC283 LNA from Qorvo was chosen, providing a noise figure of 0.6dB, 26dB OIP3 and 27dB of gain.

Table 9-1. Design Parameters for an S-band Radar

Parameter	Value
Input Clock	12GHz
DAC Sample Rate	12GSPS
ADC Sample Rate	3GSPS
TX Interpolation Factor	32x
RX Decimation Factor	8x
TX Input Rate	375MSPS Complex
RX Output Rate	375MSPS Complex

**Figure 9-2. Frequency Plan for S-band Radar Design**

An advantageous choice of RX ADC sample rate can improve the inband SFDR by assuring that the worst harmonics (HD2 and HD3) for inband signals do not fall back in band. Figure 9-2 shows the frequency of signals whose harmonics (HD2 through HD5) will fall in band for this design. Only signals outside the signal band can produce HD2 or HD3 that will fall back in band - this provides the opportunity to suppress these harmonics by reducing the out of band signal power with filtering. Suppression of the out of band signals to less than 10dBFS will reduce HD2 and HD3 to less than 85dBFS, our design requirement.

The RX filter should suppress noise and spurious signals picked up by the antenna for the images of the signal band in 2nd and 4th Nyquist zones, below 2.6GHz and above 5.3GHz respectively.

Table 9-2 summarizes the RX filter requirements, assuming the maximum out of band received signal is the same as the maximum in band received signal.

Table 9-2. RX Filter Requirements

Band	Frequency	Attenuation
Passband	3.4 - 3.7GHz	NA
Harmonic suppression	< 3.35GHz	10dB
	> 3.75GHz	10dB
Image suppression	< 2.6GHz	85dB
	> 5.3GHz	85dB

9.2.1.4 Application Curves

The RX system (referred to the antenna input) fullscale, noise figure and input IP3 is shown in [Figure 9-3](#). For small input signals, the AFE7900 automatic gain controller will set the RX DSA to 0dB.

The additive phase noise at 3.7 GHz for TX and RX is shown in [Figure 9-4](#).

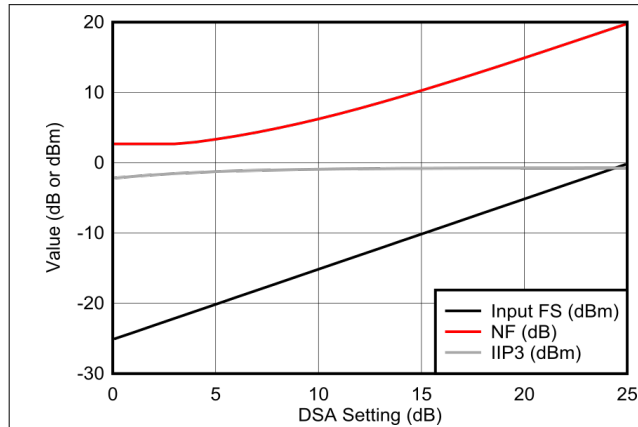


Figure 9-3. Cascaded fullscale, Noise Figure and IIP3

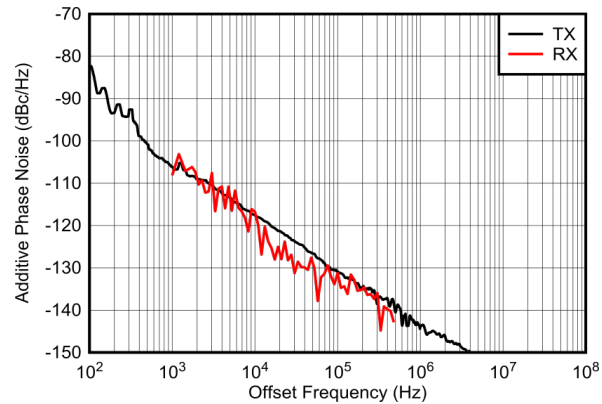


Figure 9-4. TX and RX Additive Phase Noise at 3.7 GHz

The single tone output frequency spectrum at 3.6 GHz across 500 MHz of bandwidth is shown in [Figure 9-5](#). The highest spur is ~ 90 dBc. The 2-tone SFDR vs input amplitude over temperature and DSA setting is shown in [Figure 9-6](#) - as the input amplitude per tone reduces from -7 to -20 dBFS, the highest spur created improves from -90 dBFS to -110 dBFS.

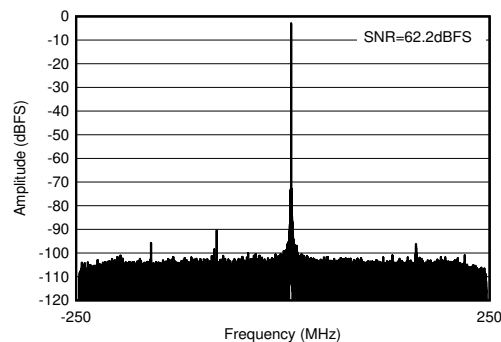


Figure 9-5. In Band SFDR at 3.6 GHz

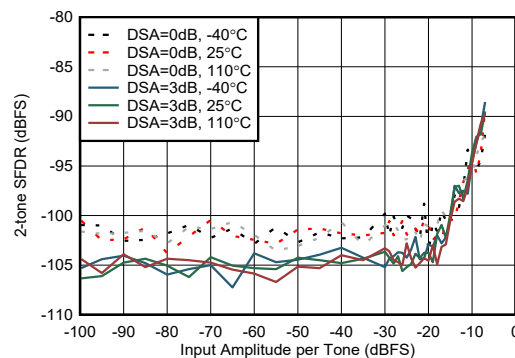


Figure 9-6. 2-tone SFDR vs Input Amplitude

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10 Power Supply Recommendations**10.1 Recommended Power Supply Groups**

Table 10-1 lists the recommend power supply groups and sub-groups. Each supply group would typically share a voltage regulator, and each supply sub-group would be isolated by ferrite beads.

Table 10-1. Power Supply Groups

POWER SUPPLIES (BALL NAMES)	VOLTAGE (V)	POWER SUPPLY GROUP	POWER SUPPLY SUB-GROUP (EVM SUPPLY NAMES)
DVDD	0.9	1A	DVDD
VDDT0P9		1A	VDDT
VDD1P2FB	1.2	2A	VDD1P2FB
VDD1P2RX		2A	VDD1P2RX
VDD1P2TXCLK		2B	VDD1P2TX_CLK
VDD1P2TXENC		2B	VDD1P2TX_CLK
VDD1P2PLLFCML		2C	VDD1P2PLL
VDD1P2PLLRCML		2C	VDD1P2PLL
VDD1P2PLLCLKREF		2C	VDD1P2PLL
VDD1P8FB	1.8	3A	VDD1P8FB
VDD1P8RX		3A	VDD1P8RX
VDD1P8GPIO		3A	VDD1P8GPIO
VDD1P8TX		3B	VDD1P8TX
VDD1P8FBCLK		3B	VDD1P8FB_CLK
VDD1P8RXCLK		3B	VDD1P8RX_CLK
VDD1P8TXDAC		3B	VDD1P8TX_DAC
VDDA1P8		3B	VDD1P8PLL
VDD1P8PLLVCO		3C	VDD1P8PLLVCO
VDD1P8PLL		3C	VDD1P8PLL

10.2 Power Supply Sequence

The power supply bring-up sequence requirements are shown in [Figure 10-1](#).

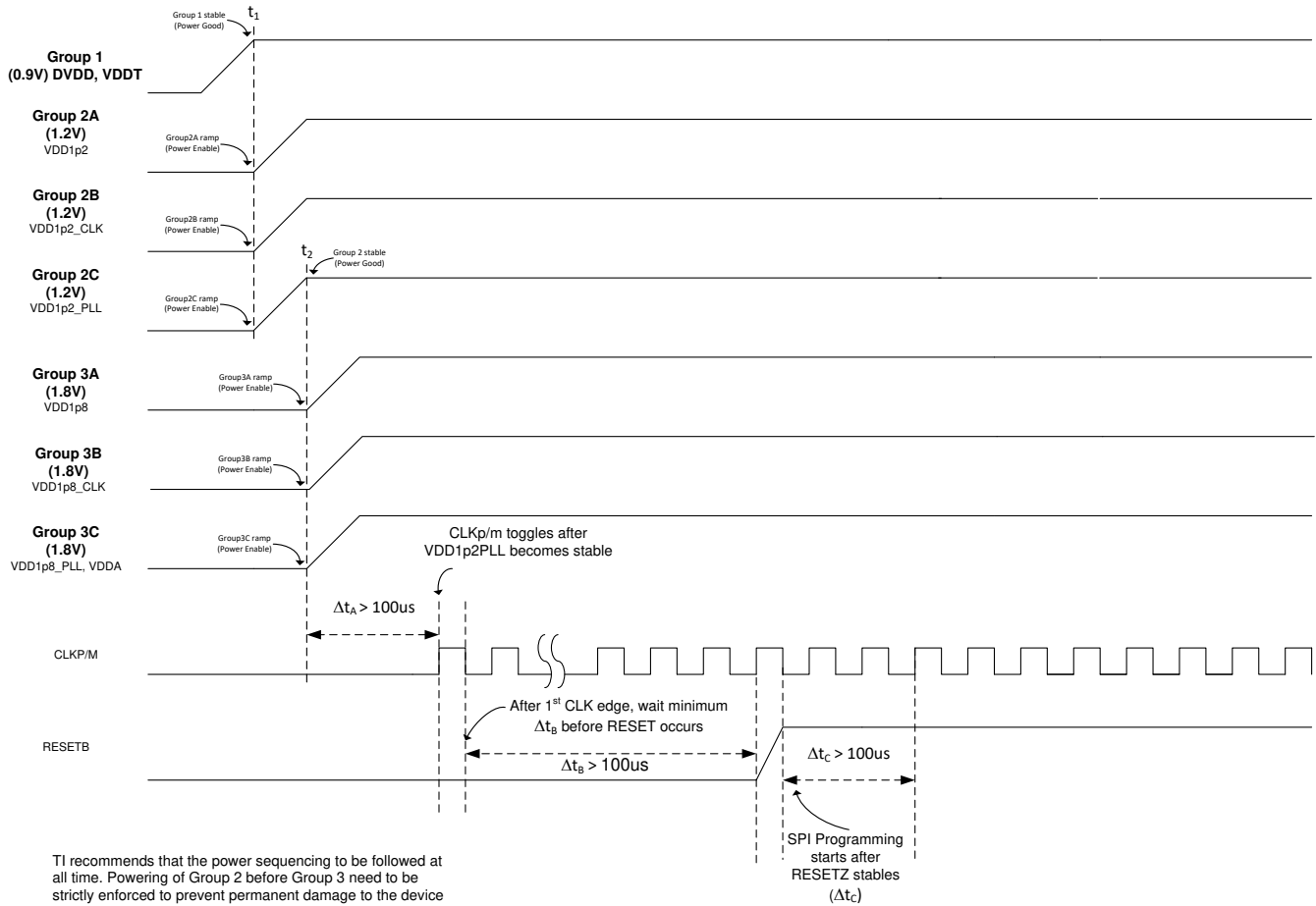


Figure 10-1. Power Supply Sequence Requirements

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11 Layout

11.1 Layout Guidelines

TI recommends to follow the layout used on the EVM. Layout guidelines are found in the application note AFE79xx Layout Guide ([SBAA405](#)) and is available by request from TI.

11.1.1 Layout Examples

Layout and symbol files for the AFE79xx EVM are available from TI upon request.

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

AFE7900

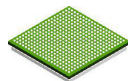
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13.1.1 Packaging Information

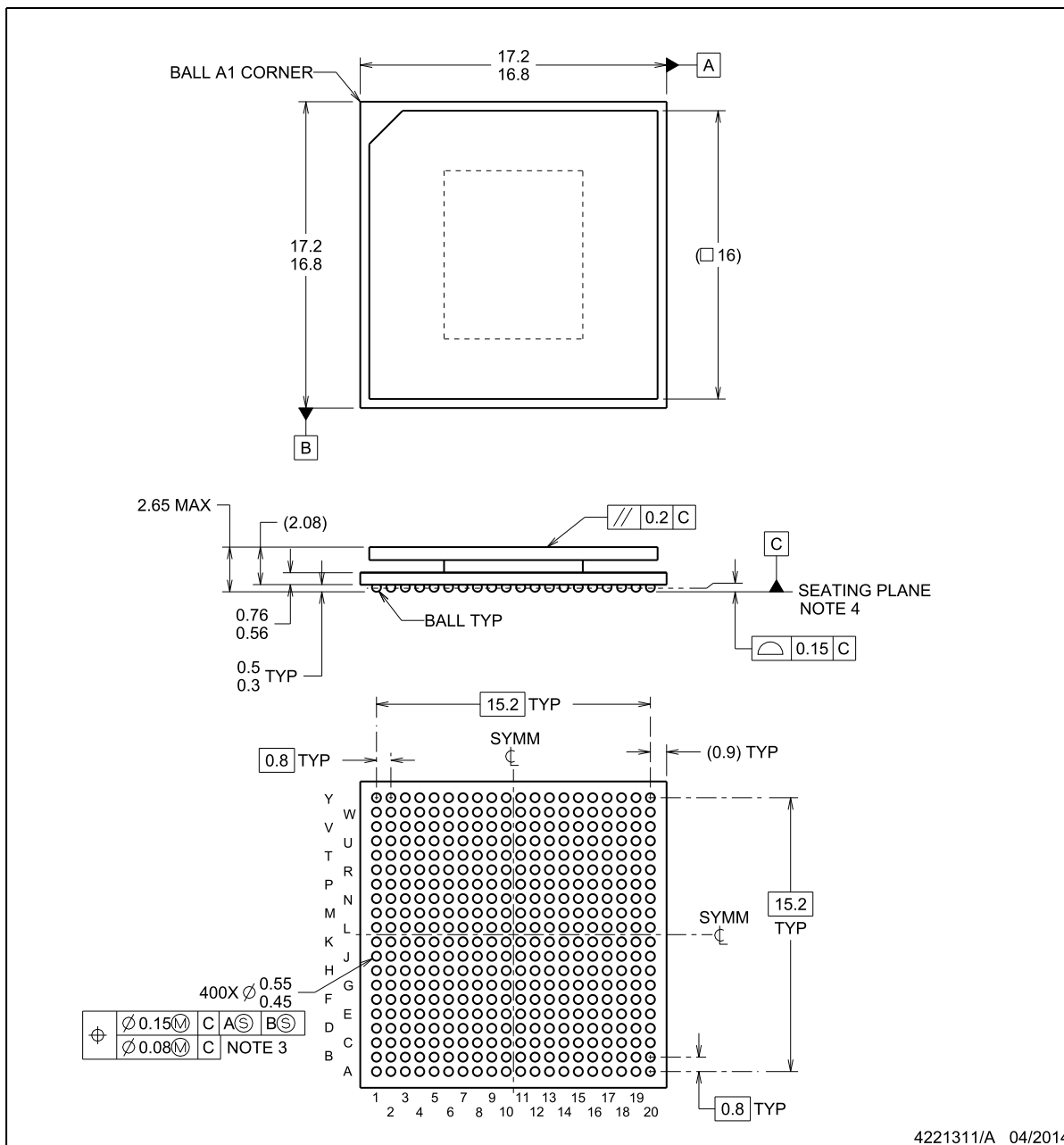
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁴⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^{(5) (6)}
AFE7900ABJ	ACTIVE	FCBGA	ABJ	400	90	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7900

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
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13.1.2 Mechanical Data

ABJ0400A**PACKAGE OUTLINE****FCBGA - 2.65 mm max height**

BALL GRID ARRAY



NOTES:

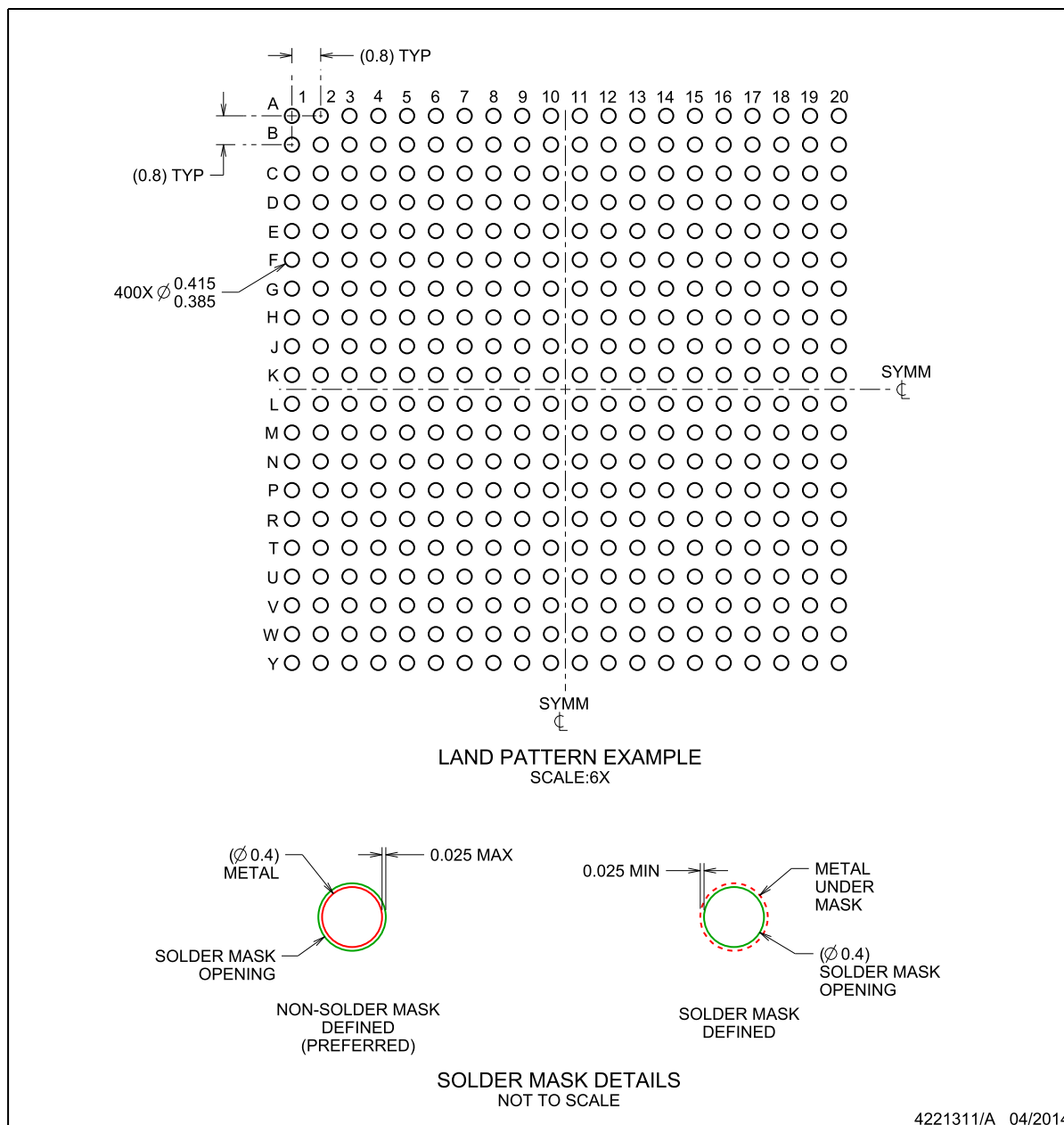
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

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EXAMPLE BOARD LAYOUT**ABJ0400A****FCBGA - 2.65 mm max height**

BALL GRID ARRAY

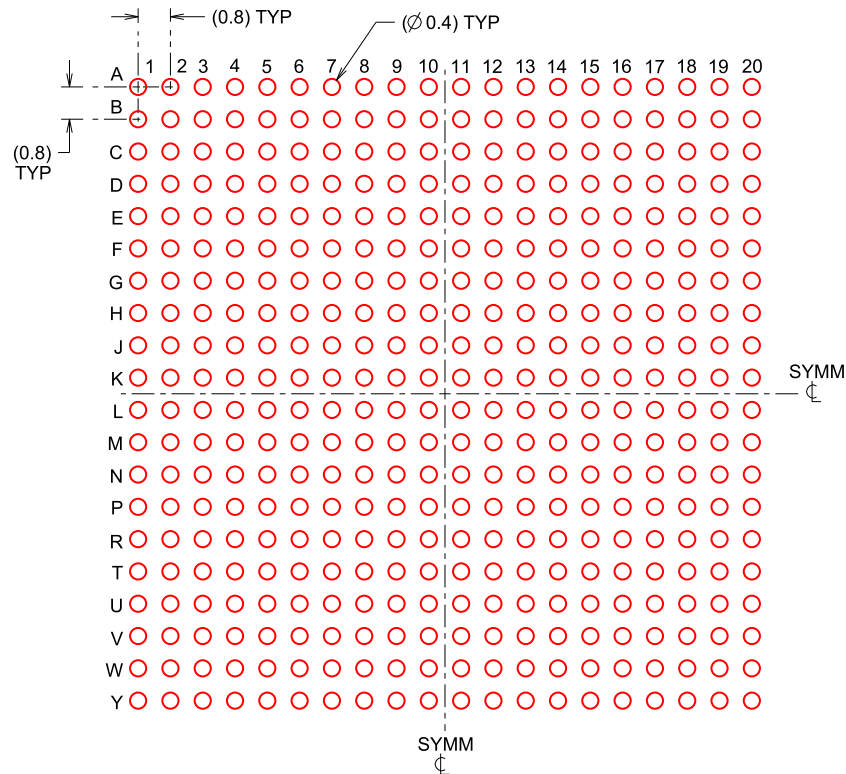


NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN**ABJ0400A****FCBGA - 2.65 mm max height**

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
 BASED ON 0.15 mm THICK STENCIL
 SCALE:6X

4221311/A 04/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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