Driving a Capacitive Load

A purely capacitive load can react with the pin and bondwire inductance of the AD8132 resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the amplifier's outputs as shown in TPC 47.

LAYOUT, GROUNDING AND BYPASSING

As a high-speed part, the AD8132 is sensitive to the PCB environment in which it has to operate. Realizing its superior specifications requires attention to various details of good high-speed PCB design.

The first requirement is a good solid ground plane that covers as much of the board area around the AD8132 as possible. The only exception to this is that the two input pins (Pins 1 and 8) should be kept a few mm from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input pins. This will minimize the stray capacitance on these nodes and help preserve the gain flatness vs. frequency.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. Good high-frequency ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 μF to 0.1 μF for each supply. Further away, low frequency bypassing should be provided with 10 μF tantalum capacitors from each supply to ground.

The signal routing should be short and direct in order to avoid parasitic effects. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This will reduce the radiated energy and make the circuit less susceptible to interference.

CIRCUITS

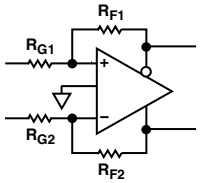

Figure 4. Typical Four-Resistor Feedback Circuit

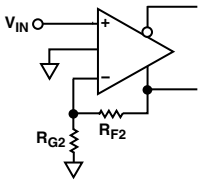

Figure 5. Typical Circuit with β1 = 0

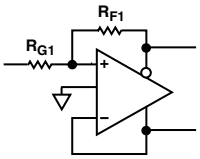

Figure 6. Typical Circuit with β2 = 1

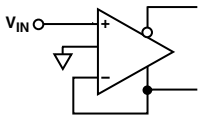

Figure 7. Resistorless G = 2 Circuit with β1 = 0

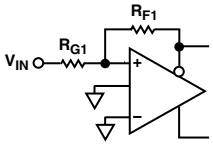

Figure 8. Typical Circuit with β2 = 0