# Active quenching circuit for a InGaAs single-photon avalanche diode*

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**Abstract:** We present a novel gated operation active quenching circuit (AQC). In order to simulate the quenching circuit a complete SPICE model of a InGaAs SPAD is set up according to the $I$–$V$ characteristic measurement results of the detector. The circuit integrated with a ROIC (readout integrated circuit) is fabricated in an CSMC 0.5 $\mu$m CMOS process and then hybrid packed with the detector. Chip measurement results show that the functionality of the circuit is correct and the performance is suitable for practical system applications.

**Key words:** single-photon avalanche diode (SPAD); active quenching circuit; gated operation
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## 1. Introduction

The high sensitivity infrared single photon avalanche diode (SPAD) is widely used in 3D imaging, laser ranging, quantum cryptography, fluorescent decays, luminescence measurements, etc.[1]. A SPAD operated in the so-called Geiger mode is essentially a p–n junction biased above the breakdown voltage[2]. Geiger mode means that, once triggered, the avalanche current keeps on flowing, thus rendering the device useless for subsequent detections. A fast quench circuit is necessary which can quickly sense the leading edge of the avalanche current of the SPAD, generate a standard output pulse and immediately bring the SPAD back to its original quiescent state.

As can be seen in published literature, there are mainly three types of quenching circuit[3]: passive quenching circuit (PQC), active quenching circuit (AQC) and gated operation active quenching circuit. The simplest circuit is the PQC that consists of a high-value (about 100 kΩ or more) ballast resistor connected in series to the diode. While the large resistor's die area and slow quenching time (about 100 ns) limit its application. To overcome the drawbacks of the PQC, a new type of quenching circuit called the AQC was proposed and soon became a widespread method in scientific literature. Such a circuit senses the avalanche through a low impedance resistor and quenches an avalanche by lowering the bias voltage below breakdown. The quenching time can reduce to about 10 ns[3]. The former two circuits operate in the so called free-running mode of operation that the detector is always biased above the breakdown at a fixed voltage to detect photons. While in some applications, such as laser ranging, where the signal presents only in a well defined interval after the laser pulse, the gated operation active quenching circuit is more desirable. This solution is to keep the SPAD below the breakdown voltage when gated-off, and at the desired excess bias state when gated-on. Comparing to the AQC, the gated operation can further reduce the quenching time, after pulse effect, and save power consumption.

Besides quenching the avalanche, quenching circuits' other duty is to generate a digital pulse signal providing a start signal to the subsequent processing circuit when detecting a photon. The rise time of the pulse directly affects the performance of the systems. For example, a slow quenching circuit will limit the time resolution in a laser ranging imaging system. The quenching circuit is closely related to the detector itself and the application.

In this paper we will introduce a novel gated operation AQC applied in an infrared readout integrated circuit (ROIC). The contents of the paper are organized as follows. In Section 2, we present more details about the ROIC operation principle that is connected to the gate controlled SPAD operation mode. The SPAD $I$–$V$ characteristic is introduced according to the experimental results in Section 3. The SPICE model of the SPAD that we applied is demonstrated in Section 4. The novel AQC architecture followed by an accurate analysis of the circuit operation principles and the key parameter design is presented in Section 5. In Section 6, we demonstrate the simulation and measurement results. The conclusions of this study are summarized in Section 7.

## 2. Gated operation mode

The basic functionality of the ROIC is to measure the time of flight (TOF) of the photon and quantized the time by a high frequency digital counter, in this way the absolute as well as the relative space distance of the object can be calculated for infrared 3D imaging. As a critical component, the SPAD is used to detect the exact arrival time of when a photon is detected and hybridized to the ROIC. Since the return time of a photon can be predicted, gated operation active quenching circuit is employed.

The EN signal controlling the SPAD operating under various modes is shown in Fig. 1, where the frame frequency

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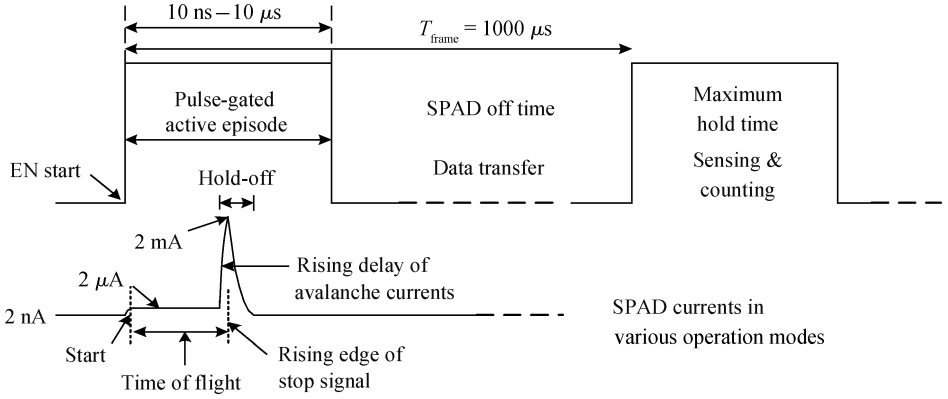


Fig. 1. EN signal and SPAD operation modes.

between adjacent infrared photon emissions for detection is 1 kHz, or the frame period time is 1 ms, and the positive pulse-gated episode of EN is variable between 10 ns to 10 $\mu$s, corresponding to a maximum duty cycle of less than 1% at 1 kHz frame frequency, providing a safe and reliable operation for the SPAD.

The photon emission starts at the rising edge of the EN pulse, at the same time the counter of the ROIC starts to count, and the SPAD is immediately biased under a reversed voltage ready for sensing.

If the back photon is sensed, a current pulse is generated with a very fast transient response. The order of the intrinsic delay for the avalanche current is around tens of picoseconds. The sensed current is transferred to a voltage pulse through a linear resistor in series with the SPAD detector. Due to the parasitic capacitance effect, the voltage pulse transient delay obviously increases compared to the current pulse. The moment when the voltage pulse generated from the avalanche current is referred to is the exact arrival time of a photon, which should be sensed as quickly as possible by the AQC to provide a stop trigger signal pulse for the high-speed counter of the ROIC, corresponding to the practical arrival time. So the rising time of the sensed voltage pulse and the total transfer delay in processing the sensed signal should be limited within the time resolution of the ROIC.

## 3. SPAD $I$–$V$ characteristics

The definition of reverse-bias breakdown voltage $V_{BR}$ is associated with the reverse bias current; usually we define the bias voltage when the reverse bias current increases sharply as the reverse-bias breakdown voltage[4, 5]. When the reverse bias voltage value is less than the $V_{BR}$, the reverse bias current is very small and changes slowly, the reverse bias current increases rapidly when the reverse bias voltage is greater than $V_{BR}$. The $I$–$V$ characteristic for SPAD is mainly related to device parameters such as device material and doping concentration.

As shown in Fig. 2, the bias tee structure is used to test the SPAD transient characteristics, where a pulse with the voltage amplitude of $V_{sw}$ is coupled to an LC network, the pulse frequency is about 1 Hz, and the gated-on time ($t_{on}$) is varied from 500 to 900 ns. $C_p$ is the parasitic capacitance containing detector intrinsic capacitance, cable and test instrument input capacitance. $R_s$ is sensing resistance that converts the avalanche current to voltage. The test is carried out at room temperature for convenience, and the avalanche current is triggered by dark current. The situation is similar to the avalanche triggered by absorbing photons at low temperatures. In the static condition outside $t_{on}$ when $V_{pulse} = 0$, $V_C = V_{power}$, and the SPAD is cut off due to $V_{power}$, which is far less than its breakdown voltage, thus $V_{sen} = 0$. In the dynamic condition within ton when $V_{pulse} = V_{sw}$, $V_C = V_{power} + V_{sw}$, the avalanche currents can probably be triggered since $V_C$ is very close to its breakdown voltage.

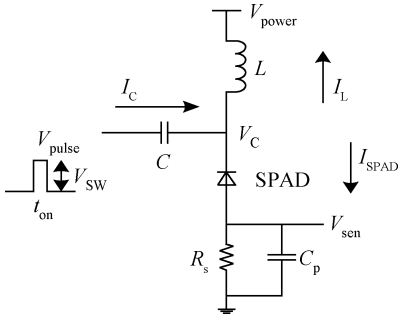


Fig. 2. Test circuit of SPAD.

The sensed voltage $V_{sen}$ within the $t_{on}$ period is shown in Fig. 3, where the maximum pulse amplitude is related to $R_s$, and rising time is related to time constant $\tau = R_s C_p$. The experimental results under different $R_s$ and $V_{power}$ conditions are given in Table 1. It can be seen that the sensed voltage pulse amplitudes and rising time are both increased with $R_s$, and the rising time increased more quickly as proportional to the $R_s$, however, the increasing of $V_{sen}$ amplitude with $R_s$ gradually slows down. This is because of the nonlinearity between the SPAD dynamic current ($I_{dynamic}$), SPAD intrinsic resistor ($R_d$) and $V_{sen}$. The dynamic current of the SAPD can be approximated by $I_{dynamic} = (V_{power} - V_{sen})/R$, where the sensing voltage $V_{sen} = R_s I_{dynamic}$ will cause the reversed voltage applied on the SPAD to reduce, and $R_d$ will also be increased due to continuous decreasing of $V_{power} - V_{sen}$, so the peak avalanche current is limited.

In fact, the rising delay time of $V_{sen}$ depends on the avalanche currents charging to the parasitic capacitance $C_p$ and sensing resistance $R_s$, and the current continuous equation can

Table 1. Rising time and pulse amplitude of the sensing voltage under different conditions.

| No | $R_S$ (Ω) | Rising time (ns) | Pulse amplitude (V) | Test condition |
|---|---|---|---|---|
| 1 | 100 | 3.5 | 0.34 | |
| 2 | 150 | 6.8 | 0.42 | |
| 3 | 200 | 10 | 0.55 | $V_{power} = 78.5$ V, EN: $t_{on} = 500$ ns |
| 4 | 270 | 15 | 0.63 | |
| 5 | 300 | 15 | 0.65 | |
| 6 | 1000 | 60 | 1.5 | $V_{power} = 78$ V, EN: $t_{on} = 900$ ns |
| 7 | 3000 | > 100 | 2.3 | |
| 8 | 1200 | 82 | 1.8 | |
| 9 | 820 | 65 | 1.4 | $V_{power} = 78.8$ V, EN: $t_{on} = 500$ ns, SMA cable |
| 10 | 510 | 45 | 1.2 | |

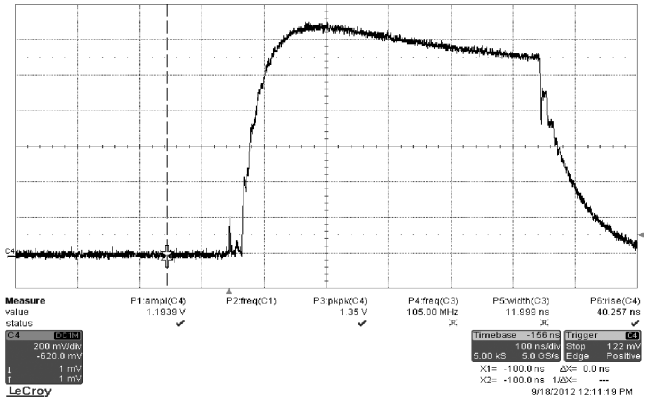


Fig. 3. Sensing voltage ($V_{sen}$).

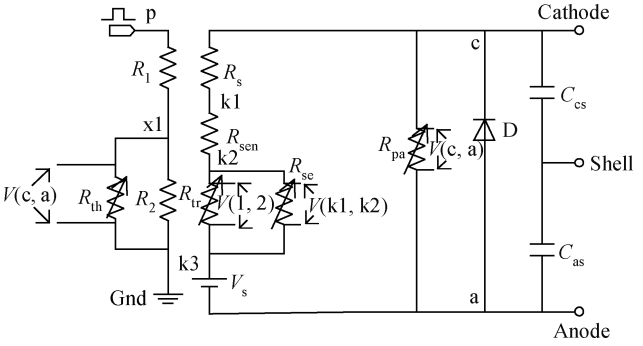


Fig. 4. The complete SPICE model for the SPAD.

be expressed as

$$\frac{V_{sen}(t)}{R_S} + C_p \frac{dV_{sen}(t)}{dt} = I_{SPAD}(t). \quad (1)$$

The intrinsic delay of sensing avalanche currents can be neglected compared to the voltage. In order to simplify the calculation, the avalanche current variable with conditions can be replaced by its peak value $I_{peak}$, which is related to $R_s$, as mentioned above. So the sensed voltage pulse peak amplitude is $V_{swing} = I_{peak} R_s$. In order to detect the voltage pulse more reliably, the voltage swing should be obviously larger than the threshold voltage of the comparator or inverter that follows, so that a relatively large $R_s$ is required to increase the swing.

However, large $R_s$ will result in a larger voltage rising delay, where the rising delay time of the sensing voltage pulse (TD) from $V_{start}$ to $V_{end}$ is given by

$$t_d = R_s C_p \ln \frac{V_{swing} - V_{start}}{V_{swing} - V_{end}}. \quad (2)$$

If $V_{start} = 10\% V_{swing}$, $V_{end} = 90\% V_{swing}$, thus $t_d \approx 2.2 R_s C_p$, which is proportional to $R_s$ and $C_p$. For fast detection, the sensing resistance $R_s$ should be as small as possible.

Based on the experimental results in Table 1 and the equation, the total capacitance is around 40 pF when the SMA cable is used in testing. It is under the precision test by a high frequency differential probe for 510 Ω that the parasitic capacitance is reduced to 4 pF, the voltage swing remains unchanged, but the rising time decreases from 45 to 4–5 ns when the sensing resistance is 510 Ω. In this situation the intrinsic capacitance contributed by the SPAD is estimated to be less than 2 pF, and the actual rising time is approximately 1–2 ns; such a delay time can be accepted for the 2 ns timing resolution of the ROIC.

## 4. SPICE model of the SPAD

A complete SPICE model of the SPAD is shown in Fig. 4, considering the dynamic imitation of the SPAD, the resistor $R_s$ represents the resistance of the neutral zone and the value is 320 Ω. According to the device structure, the shell can be left floating or connected to the anode. $R_{th}$, $R_{tr}$, and $R_{se}$ are the voltage-controlled resistors which control the working process of the SPAD. A pulse voltage is used to imitate the arrival of the photon, which is divided between the resistances $R_1$ and $R_2$. $R_{th}$ is used to enforce the device working in Geiger-mode. $R_{tr}$ is used to trigger the avalanche current by checking the voltage between the voltage node x1 and gnd. If the voltage difference is higher than the threshold voltage, such as 0.05 V, $R_{tr}$ will be zero. As the duration of the pulse voltage is too short to exceed 1 ns, after the pulse the voltage applied on $R_2$ will be zero and writer will be large enough to quench the branch current to zero. Voltage-controlled resistor rice is added to check the voltage between the nodes k1 and k2, which ensures the self-sustaining property.

The model employed in this paper can be implemented into the HSPICE simulation environment to precisely predict the static and dynamic operation mechanism of the device. Simulation results and measurement results have proved the consistency and accuracy of the model.

## 5. Gated operation active quenching circuits

The architecture of the AQC applied in our ROIC is presented in Fig. 5, where EN is the pulse-gated signal, $R_s$ is the sensing linear resistor converting the avalanche current to the voltage, $V_{power}$ and $V_{DD}$ are the supply voltages to power the SPAD detector and the AQC logic circuit, respectively. The power is much larger than $V_{DD}$. If the SPAD is reversely biased by $V_{power}$ , the detector will enter detection mode, and if the reversed voltage drops to $V_{power} - V_{DD}$, the detector will operate under the sleeping mode.

A pair of switch transistors of PM and NM controlled by a DFF is used to shift the reversed biasing voltage of SPAD under a different time sequential. Being limited by the pixel area, the inverter is used instead of a conventional comparator to trigger the mono stable circuit (MS) when the voltage $V_{sen}$ reaches a certain threshold value. The short duration time under the non-stable statue is generated from the delay line circuit (DL). Other than the XOR gate, a NAND gate is used in the output of the MS, the stable output is logically high, thus only a falling edge occurred at the input that can trigger the MS into the non-stable state temporarily and return back to the stable statue.

As mentioned above, three kinds of working statue of a AQC are summarized as below:

(1) When EN = 0, then $V_{sen}$ is pulled up to $V_{DD}$ by the PM transistor to keep the SPAD in sleeping mode. At the rising edge of EN from low to high and EN = 1, under the control of DFF, $V_{sen}$ is pulled down to GND by the NM transistor to keep the SPAD under the detecting mode;

(2) When EN = 1 and one or more photons are detected, $V_{sen}$ generates a small positive pulse. Through an inverter the positive pulse becomes a negative pulse. The falling edge of Trig appears at the input of the MS circuit, so that a negative pulse generates at the output (OS). The Stop signal is just the inversion of OS. At the same time, the negative pulse of OS resets the DFF(E = 0), so that $V_{con} = 0$ even when EN = 1, and $V_{sen}$ is pulling up back to $V_{DD}$ to quench the avalanche current and returns the SPAD back to the sleeping mode.

(3) If there is no photon arrival during gated-on time (EN = 1), the SPAD is in the detecting mode until EN = 0, then $V_{con} = 0$, the PM transistor turns on and the NM transistor turns off. The reverse bias voltage of SPAD is pulled down to $V_{power} - V_{DD}$, so the detector returns to sleeping mode.

As mentioned above, the rising time of $V_{sen}$ should be as small as possible to fit for ROIC timing resolution, thus the $R_s = 600\ \Omega$ is selected according to the experimental results, and the peak avalanche current is around 2 mA generating a maximum of 1.2 V voltage swing. Due to serious area and current consumption limitation, an inverter is used instead of a conventional differential comparator, where the threshold voltage of inventor ($V_{inv}$) can be calculated by the W/L ratio relationship, as given by

$$V_{inv} = \frac{V_{TN} + (V_{DD} - V_{TP})\sqrt{\alpha_{pn}}}{1 + \sqrt{\alpha_{pn}}}, \tag{3}$$

where the respective gain factor ratio is defined as $\alpha_{pn} = k_p/k_n = (\mu_p/\mu_n)\ [(W/L)_p/(W/L)_n]$, $\mu_n$, $\mu_p$ are electron and hole mobility, $(W/L)_p$, $V_{TP}$ and $(W/L)_n$, $V_{TN}$ are $W/L$ ratio and threshold voltage of NMOS and PMOS respectively. When $(W/L)_n \gg (W/L)_p$, $\alpha_{pn} \to 0$, and $V_{inv} = (1+m)\ V_{TN}$, thus the scaled $W/L$ ratio is given as:

$$\alpha_{WL} = \frac{(W/L)_p}{(W/L)_n} = \frac{\mu_n}{\mu_p}\left[\frac{m}{(V_{DD} - V_{TP})/V_{TN} - (1+m)}\right]^2. \tag{4}$$

In order to reduce the rising time of vision and quench time, $m$ should be as small as possible. If $V_{DD} = 5$ V, $\mu_n/\mu_p = 2.5$, and $V_{TP} = 1.0$ V, $V_{TN} = 0.8$ V around –20 ℃, when $m = 0.2$ is selected, we can get $\alpha_{WL} \approx 1/144$, $V_{inv} = 0.96$ V, resulting in a falling edge at the output of the inverter when its input pulse $V_{sen} \geqslant 1.2$ V. The pull-up transistor PM can be smaller due to less current needed, and the pull-down transistor NM should be relatively large to make the turn-on resistance smaller as a part of total $R_s$.

The $R_s$ is implemented by P+ resistance with 168.9 Ω/□, the nominal value of the resistance is 442.25 Ω under square dimension of $W \times L = 4.0\ \mu m \times 10\ \mu m$, where the resistance can be slightly adjusted by the width while keeping the length fixed. The turn on resistance $R_{on}$ of the MN transistor under $V_{DD} = 5$ V is varied about from 64 to 89 Ω when the process shifts, resulting in a total sensing resistance approximately 540 ± 60 Ω. So even at the least value of $R_s = 480\ \Omega$, $V_{sen} = 0.96$ V, that value can make the inventor output in a falling edge.

Table 2. Post simulation results of the AQC.

| Condition | Reset time | Detecting delay | Quenching time |
|---|---|---|---|
| Post simulation | 5.1 ns | 1.7 ns | 7.3 ns |

## 6. Simulation and measurement results

The proposed AQC is implemented by a CSMC 0.5 $\mu$m CMOS process, and the area of the circuit is around 2400 $\mu m^2$. The supply voltage to bias SPAD can be altered at an approximate level of $V_{power} = 78.26$ V, and the supply voltage for logical circuit operation is fixed at $V_{DD} = 5$ V. Figure 6 illustrates the circuit operation during a single avalanche pulse, showing when EN is gate-on, the circuit begins resetting, and after a single photon arrives, the SPAD is successfully quenched.

The time elapsed from the onset until the avalanche is quenched is called "quenching time". This latter procedure is called "reset", and the "reset time" is the time taken to bring the device back to its original state. For a given excess bias voltage, the avalanche charge can be reduced by quick quenching avalanche. Also, a fast reset can make the SPAD prepare for the next detection as soon as possible. These two characteristics directly affect the performance of the SPAD.

The rising delay as well as its dispersion are both degenerated under the parasitic capacitance and resistance influence, in order to keep the relative precision, the layout of the AQC is well designed to minimize the parasitic effects. The key characteristics under post simulation are summarized in Table 2.

Figure 7 illustrates the waveforms of the resetting event and quenching event of the SPAD anode, showing that the functionality of the circuit is correct, but due to the big input capacitance of the oscilloscope, the quenching time is about 78.5 ns, and the value of $V_{sen}$ is a little smaller than expected. As the

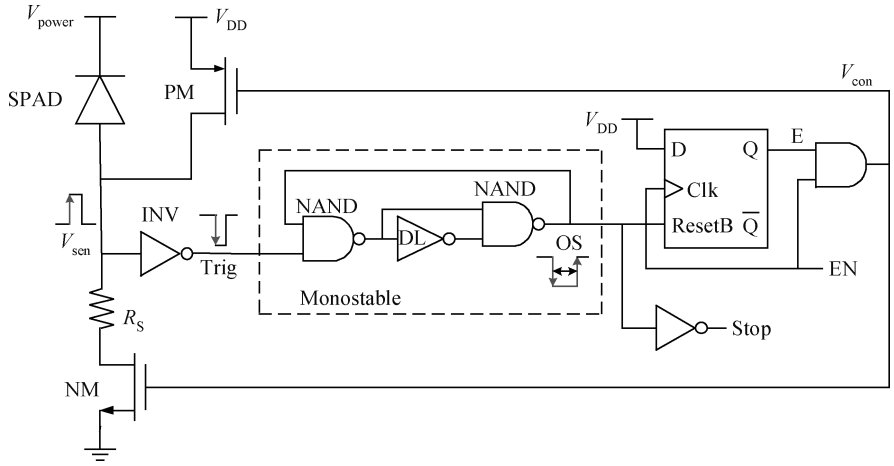


Fig. 5. The proposed gated operation active quenching circuit.

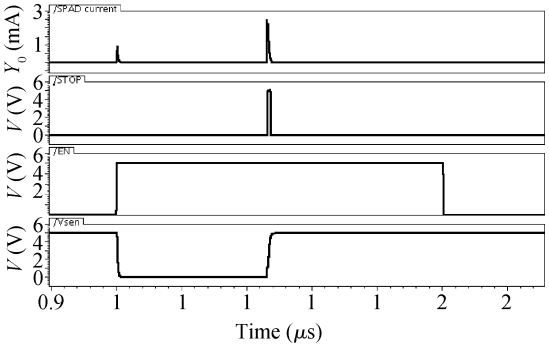


Fig. 6. Simulation results: an avalanche event with a successful quenching in a frame.

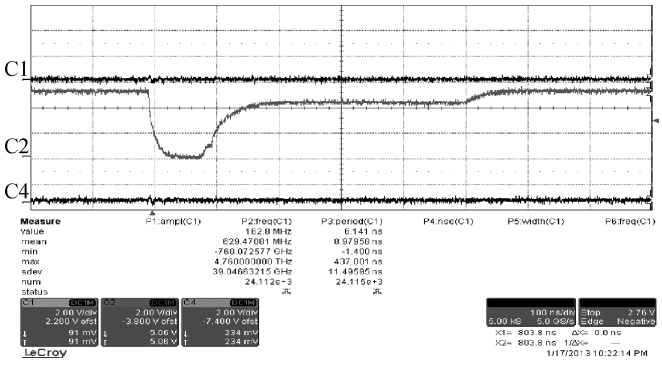


Fig. 7. Measurement waveforms of the SPAD anode.

test fall time of $V_{sen}$ is 22.8 ns and $t_d \approx 2.2R_sC$, the big input capacitance of the oscilloscope ($C_o$) can be calculated to about 15.6 pF. Table 3 shows that the measurement results are close to the post simulation results with $C_o$. From the comparison we can conclude that the real reset time, detecting delay and quenching time of the chip is close to post simulation without $C_o$.

Single-photon detection is relatively a kind of advanced technology. The existing study on single-photon detection mostly focuses on theoretical analysis and circuit simulation, but lacks test results and verification[6]. The main reason for this is that the InGaAs detector needs to be carried out through

Table 3. Post simulation results with $C_o$ and measurement results of AQC.

| Condition | Reset time (ns) | Detecting delay (ns) | Quenching time (ns) |
|---|---|---|---|
| Post simulation+$C_o$ | 34 | 12.25 | 60 |
| Measurement | 35 | 13 | 78.5 |

Table 4. Comparison of quenching circuit measurement results.

| Reference | This work | Ref. [7] | Ref. [8] |
|---|---|---|---|
| Process ($\mu$m) | 0.5 | 2 | 0.8 |
| Circuit type | AQC | AQC | AQC |
| Quenching time (ns) | 7.3 | 3 | 12 |
| Reset time (ns) | 5.1 | 1 | 8 |
| Voltage detection method | Inverter | Transistor | Comparator |

hybrid packaging with a detection circuit, namely, the detector has to be fabricated on the finished circuit, followed by the high requirements for the testing environment, equipment and methods. Table 4 shows the comparison measurement results of the proposed circuit with other published quenching circuits. The performance of the quenching circuit is directly affected by the detector. The detector used in this paper is produced domestically. According to the compared results, the designed AQC in this article has the following merits: a novel voltage detection method and simple configuration, but there is still a certain gap in the test performance between it and most advanced designs abroad.

## 7. Conclusion

In this paper a type of active quenching circuit for biasing and quenching InGaAs SPAD detectors is presented. The circuit operates in gated mode which can reduce the quenching time and save power consumption compared to conventional circuits. Achieving a compact chip area, the circuit is integrated with the ROIC and fabricated in a CSMC 0.5 $\mu$m process. Moreover, the circuit uses only simple logical circuits

and a few transistors, and thus occupies a small silicon area. The circuit integrated with ROIC is used for infrared ranging in 3D imaging systems. Chip measurement results show the circuit achieves a faster quench and reset time.

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