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A High -Temperature, High-Voltage, Fast Response Time Linear Regulator in 0.8um BCD- on-SOI

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To the Graduate Council:

I am submitting herewith a dissertation written by Chia Hung Su entitled "A High -Temperature, High-Voltage, Fast Response Time Linear Regulator in 0.8um BCD-on-SOI." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Syed K. Islam, Major Professor

We have read this dissertation and recommend its acceptance:

Benjamin J. Blalock, Leon Tolbert, Joshua S. Fu

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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Degree
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Chiahung Su
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ABSTRACT

The sale of hybrid electric vehicles (HEVs) has increased tenfold from the year 2001 to 2009 [1]. With this the demand for high temperature electronics has also increased dramatically making, high temperature electronics for HEV applications desirable in the engine compartment, power train, and brakes where the ambient temperature normally exceeds 150°C. Power converters (i.e. DC-DC converter, DC-AC inverter) inside the HEVs require gate drivers to control the power switches. An integrated gate driver circuit has been realized in 0.8-um BCD-on-SOI process. This gate driver IC needs a step-down voltage regulator to convert the unregulated high input DC voltage (V_{DDH}) to a regulated nominal CMOS voltage (i.e. 5 V). This step-down voltage regulator will supply voltage to the low-side buffer (pre-driver) and other digital and analog circuits inside the gate driver ICs. A linear voltage regulator is employed to accomplish this task; however, very few publications on high temperature voltage regulators are available. This research presents a high temperature linear voltage regulator designed and fabricated in a commercially available 0.8-um BCD-on-SOI process. SOI processes typically offer reduced junction leakage current by three orders of magnitude compared to the bulk-CMOS processes at temperatures beyond 150°C. In addition, a pole swap compensation technique is utilized to achieve stability over a wide range (four decades) of load current. The error amplifier inside the regulator is designed using an inversion coefficient based design methodology, and a temperature stable current reference is used to bias the error amplifier. The linear regulator provides an output voltage of 5.3 V at room temperature and can supply a maximum load current of 200 mA.

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CHAPTER 1

INTRODUCTION

In this chapter, the research motivation is introduced in section 1.1. The gate driver circuit designed to turn on the power switches of the power converter modules inside the HEVs (Hybrid Electric Vehicle) is presented in section 1.2. The topologies of voltage regulators and the specifications are discussed in sections 1.3 and 1.4, respectively. The selection criteria of the pass transistor of the voltage regulator are provided in section 1.5. Section 1.6 briefly introduces the Silicon-on-Insulator (SOI) technology.

1.1 Motivation

The application of high temperature electronics can be found among well logging, aerospace, nuclear and automotive industries. In particular, hybrid electric vehicles (HEVs) which employ high temperature drive electronics for traction motors are attracting significant investment of effort and time from the auto manufacturers and researchers, leading to their successful commercialization [1]. The HEVs require more high performance integrated automotive electronics systems to achieve high output power, better fuel efficiency and clean exhaust [2]. Figure 1.1 depicts the schematic of a plug-in hybrid vehicle. Inside the hybrid vehicle system, the power converter modules are required to drive the electric motor.

The power converter modules (DC-DC converter and DC-AC inverter) for automotive application are normally placed under the hood, where the ambient temperature is around 150°C to 200°C. Every power converter modules requires power switches to control the flow of power

Therefore, inside the power converter module of the HEVs, the gate driver is employed to control the “ON” and “OFF” operations of the power switches [3].

Nowadays, most of the power switches (i.e. IGBT, Power MOSFET, and JFET) are made of silicon material. DMOS power transistors are widely utilized in automotive application because it is easier to interface these devices with the digital microcontrollers [4]. However, the silicon power switches are limited by breakdown voltage, operating temperature, current density, leakage current and switching losses.

Increasing the operating device temperature decreases the bandgap of the semiconductors [4] and the reduced bandgap with increasing temperature leads to increased intrinsic carrier densities and leakage current. The intrinsic carrier concentration of a semiconductor, n_i , is negligible compared to the doping concentration at room temperature. However, n_i is doubled with every 11°C increment of the temperature. Due to the low intrinsic carrier concentration of the wide bandgap materials such as SiC and GaN, power switches realized in these material systems can potentially be employed to replace silicon power switches in near future.

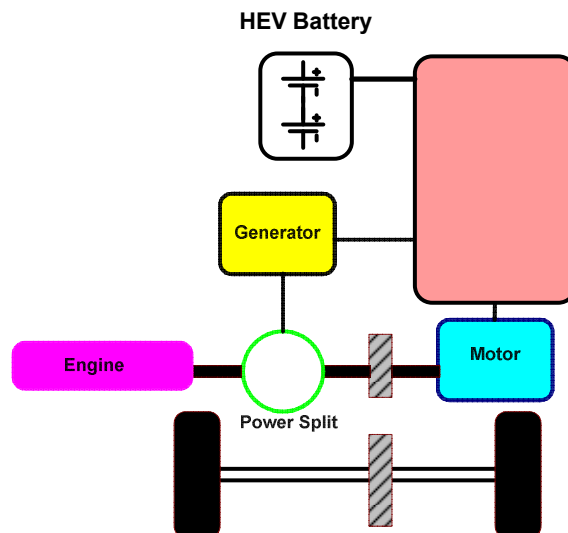


Figure 1.1 Block diagram of a hybrid electric vehicle

The power switches in HEVs require high temperature and high voltage operation, high current density and low power losses. The wide bandgap semiconductors offer potentially better high temperature performance compared to silicon. Table 1.1 compares the properties of Si, SiC and GaN.

In Table 1.1, the thermal conductivity determines the ability of the semiconductor to dissipate heat at ambient environment. The device with higher thermal conductivity can quickly and effectively remove the heat [5, 6] and can minimize the need of costly cooling system which increases the weight and volume of the power converters.

Table 1.1 Properties of Si, SiC and GaN [4]

Material	Bandgap, E_g (eV)	Mobility ($\text{cm}^2/\text{V.s}$)	Thermal Conductivity ($\text{W/cm}^2\text{K}$)	Electric Breakdown Field (MV/cm)	Dielectric constant	T_{max} ($^{\circ}\text{C}$)
Si	1.121	1450	1.5	0.3	11.9	150
SiC	3.02	1000	4.9	7	9.7	600
GaN	3.45	600	1.5	2	10.4	700

Power switches made of wide bandgap materials such as SiC possess higher thermal conductivity and high electric field strength compared to Si. The wide bandgap of SiC results in low intrinsic carrier density and low leakage current properties making these devices properly function at temperatures beyond 600°C [5]. The commercially available SiC power MOSFETs have demonstrated the maximum operating temperature up to 250°C . [6]

The SOI (Silicon-on-Insulator) process technology is an alternative solution for designing reliable high temperature electronics. The commercially available SOI process extends the

maximum operating temperature beyond 225°C which covers the reported ambient temperature under the hood of the HEVs.

High temperature electronics designed for both automotive and oil well logging require reliable operation at elevated temperatures. The SOI fabrication process based analog integrated circuit is more suitable for operating at elevated temperatures compared to the standard bulk CMOS process based analog integrated circuits due to the reduced junction leakage current, smaller variation of threshold voltage with temperature, reduced parasitic capacitance and latch-up immunity offered by the SOI processes [4,7]. On the other hand, the bulk CMOS integrated circuits (IC) suffer significant performance degradation and increase of self-heating at elevated temperature as a result of the increased leakage current [4].

The SOI (Silicon-On-Insulator) process technology offers a better solution for analog electronic operating at elevated temperature by suppressing the leakage current. Nevertheless, a temperature stable reference current is extremely important for biasing an error amplifier, because the increasing leakage current with temperature may result in the shift of operating point. Meanwhile, the temperature stable current biased error amplifier will preserve the power consumption, the quiescent current consumption, the DC open loop gain and the stability across the wide temperature range.

An important concept for maintaining the linearity of the circuit over temperature utilizing the temperature coefficient of the biasing current, stability, and matching is also very crucial for amplifiers, voltage regulator, ADC (analog-to-digital converter) and oscillators operating at elevated temperatures [8].

The current reference (bias current) can be realized on-chip for the purpose of reducing the overall cost and the need for off-chip components. This work also presents an on-chip

temperature stable current reference that will benefit both the error amplifier and the voltage regulator for biasing the error amplifier.

This research utilizes the high temperature analog integrated circuit design techniques and methodologies to design amplifier and current reference. Therefore, a high temperature linear voltage regulator has been implemented based on the high temperature IC design techniques.

1.2 Gate Driver Circuit and Voltage Regulator

In hybrid electric vehicles, there is a trend toward using more electrical systems to replace mechanical and hydraulic systems. Figure 1.2 illustrates the estimated value of automotive electronics per vehicle. In 1955, there was only \$20 spent in automotive electronics per vehicle, the only automotive electronics in 1950's being the radio. In 2013, the value of automotive electronics is predicted to be spent over \$2000 per vehicle [4, 9, 10].

High temperature electronic circuits for HEV applications are desired in the engine compartment, power train, and brakes where the ambient temperature normally exceeds 150°C. The hybrid electric vehicle needs high temperature power converters to drive the electric motor. Power electronic circuits are employed to perform three major tasks: (i) turn on/off the switching load, (ii) act as a suitable controller for electric traction motor, and (iii) convert electrical power from one form to another (i.e. DC/DC, DC/AC, and AC/DC converters) [20]. Inside a power converter module, a gate driver circuit is employed to turn on/off the power switch device (i.e. silicon power MOSFET, IGBT, SiC power MOSFET, etc.).

A digital signal from the microcontroller does not have sufficient drivability to drive the huge parasitic capacitances of the power semiconductor devices. Therefore, the gate driver is utilized to charge/discharge the large parasitic capacitance (C_{gd} , C_{gs}) of power switches [11, 12].

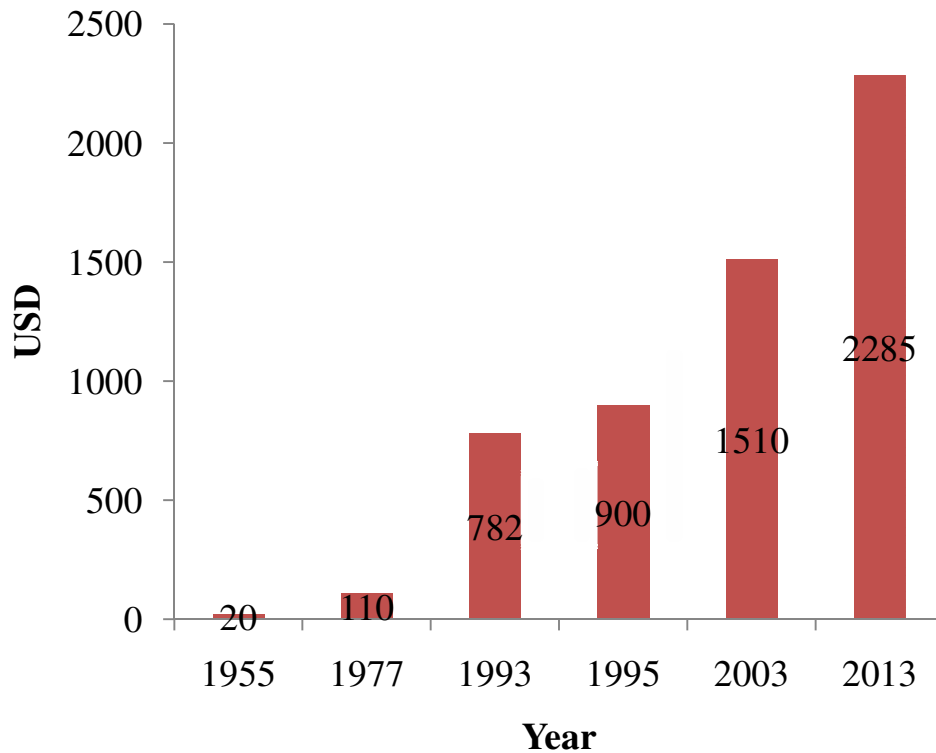


Figure 1.2 The estimated value of automotive electronics per vehicle [4]

In addition, because the power switching device is exposed to high temperature environment (above 175°C); a high temperature gate driver circuit is needed inside the hybrid electric vehicle system. Figure 1.3 shows the block diagram of the gate driver circuit which is an example of a synchronized digital system. A voltage regulator is required to provide power (5 V) to the low-side driver, the pulse generator, the non-overlapping clock generator, the input buffer and to charge the bootstrap capacitor. This voltage regulator needs to meet the specifications of the gate driver circuit (i.e. high voltage/temperature, low quiescent current, line and load regulation).

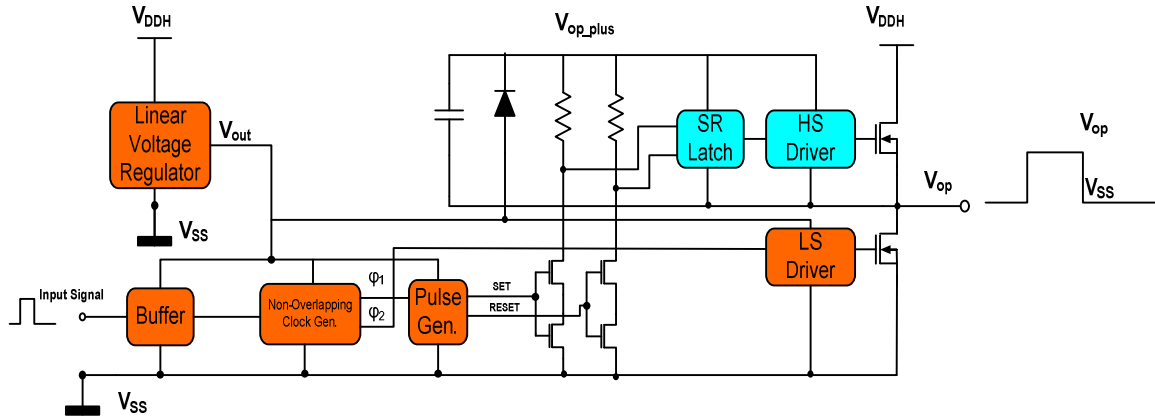


Figure 1.3 The block diagram of gate driver circuit.

A voltage regulator is an essential component of the analog integrated circuit. The function of voltage regulator is to provide a noiseless and stable output voltage regardless of the load current variation. By means of design topology, the voltage regulator can be classified into linear voltage regulator, switching mode regulator and shunt voltage regulator. Most of published literatures nowadays are concentrated on linear voltage regulator and the switching mode voltage regulator due to the consideration of load regulation, efficiency and power consumption.

In the process of designing a voltage regulator, the line regulation, the output voltage droop, the open loop gain of error amplifier, the power supply rejection ratio (PSRR) and the current efficiency have been considered which will dictate the performance of the regulator. While the standard CMOS voltage regulator can be operated at elevated temperature, the leakage current from the parasitic PN junction of the standard CMOS process will increase which will degrade the performance of the error amplifier. Hence, the CMOS based voltage regulator may not provide a regulated output voltage.

The linear voltage regulator designed for this work includes a 2.2 V bandgap voltage reference circuit, an error amplifier (folded-cascode OTA), a voltage buffer, a feedback resistor,

a frequency compensation circuit, a temperature stable current reference circuit, a shunt pre-regulator and a HV NMOSFET (DMOS) pass transistor. A prototype of high temperature linear regulator has been designed and fabricated in a commercially available BCD-on-SOI process (0.8-micron, 2-poly and 3-metal). The design supports an input DC power supply voltage range of 10 V to 45 V and a maximum operating temperature of 175°C. The linear regulator provides an output voltage of 5.3 V at room temperature and can supply a maximum output load of 200 mA.

1.3 Comparison of Voltage Regulator Topologies

The voltage regulator accepts a poorly specified DC input voltage and produces a constant DC output voltage, which is used to supply the analog, digital and mixed signal integrated circuits. Based on the design topologies the voltage regulator can be classified as linear voltage regulator, switching mode voltage regulator and shunt voltage regulator. The following section briefly introduces the design topologies of the voltage regulator.

1.3.1. Linear Regulator

Linear regulator is also called series regulator, because the pass device is in series with the regulated output voltage node. The linear voltage regulator utilizes the series-shunt negative feedback to generate the output voltage. A voltage reference circuit can generate a stable reference voltage, but it cannot be employed as a voltage regulator because of its insufficient current sourcing capability. In the linear regulator structure the reference voltage is applied to the input of the non-inverting terminal while the feedback voltage node is connected to the input of inverting terminal, and the output voltage is determined by the closed loop gain of the non-inverting amplifier configuration. The output voltage is a multiple of the reference voltage. A

typical linear voltage regulator consists of a voltage reference circuit (such as Zener diode or bandgap voltage reference), an error amplifier, a pass transistor, a frequency compensation circuit and a feedback resistor [14, 15, 16].

Low dropout voltage (LDO) regulator is widely used in consumer electronics, cell phone, microprocessor, etc., because of the low dropout nature of the output voltage. That is to say, when LDO voltage regulator sources a load current above 100's mA range, the efficiency of the LDO voltage regulator can simply be defined by the ratio of the output voltage over the input voltage. In this case, the linear voltage regulator efficiency can be comparable with that of the switching mode voltage regulator.

A linear regulator can only serve as a step-down DC converter, which means the input DC voltage is larger than the regulated output voltage. In addition, the linear voltage regulator responds faster than the switching voltage regulator. The response time is normally less than 2 μ s [14], because it utilizes less analog components for its implementation. The noise of the linear regulator is lower than that of the switching mode regulator as the switching regulator introduces switching noise at the output voltage. Meanwhile, the low quiescent current LDO design is feasible by utilizing low-voltage and low-power design techniques. The linear regulator can be implemented in bulk CMOS, BiCMOS, bipolar and SOI processes.

1.3.2. Switching Regulator

The switching mode voltage regulator, which can be considered as a mixed-signal integrated circuit, is a combination of digital and analog circuits. The benefit of using switching regulator is its high efficiency which is between 80%~95% [14]. Switching regulator can provide

an output voltage lower than the input voltage (step down converter/buck converter) and an output voltage larger than the input voltage (step up converter/boost converter).

The switching regulator consists of voltage reference, comparator, error amplifier, pass transistor, PWM (pulse width modulated) controller, clock generator, saw-tooth wave generator, inductor, and capacitor.

Obviously, the switching mode voltage regulator adds more design complexity and cost compared to the linear voltage regulator. The system response time is slower than that of the linear voltage regulator and is typically between 2 and 8 μ s [16].

The switching mode voltage regulator utilizes switching on and off of the PMOS and the NMOS bridge configurations to convert the input DC voltage to an average output voltage. The average output voltage is determined by controlling the switching on and off durations and can be adjusted by varying the duty cycle of the switching period, T_s , where the duty cycle is controlled by the PWM controller. Due to its switching nature, the switching regulator is noisier than the linear regulator. Therefore, it is suitable for less noise sensitive circuits or a pre-regulator for linear voltage regulator.

In addition, the switching mode voltage regulator requires multi-phase to reduce the output voltage ripple [17], and the multi-phase switching mode voltage regulator will increase the chip area overhead.

1.3.3. Shunt Regulator

The shunt regulator has the least design complexity among all regulator configurations. “Shunt” represents a pass transistor which is paralleled with the output voltage node. In the board level design of the shunt regulator, it only requires resistor and Zener diode to implement a shunt

regulator. The shunt regulator does not utilize negative feedback, so it is an open loop circuit, and the output current capability of the shunt regulator is decided by the voltage drop across the resistor and the value of the resistor. The pass transistor of a CMOS shunt regulator requires adequate capability to sink the current required from the load.

Therefore, the power consumption limits the application of a shunt regulator, and it does not utilize negative feedback to regulate the change of the output voltage during load-dumps. In addition, it suffers from poor load and line regulation, but it can be employed as a pre-regulator. This research has utilized a shunt regulator as a pre-regulator to lower the input DC voltage that allows a regular MOSFET to operate under device breakdown limitation. Table 1.2 summarizes the comparison of the voltage regulator topologies.

1.4 Specifications of Voltage Regulator

This section will discuss the specifications of a voltage regulator [13~23]. Figure 1.4 shows the conventional linear voltage regulator; the output voltage is expressed as $V_{ref} \cdot (1 + R_2/R_1)$. The performance of a voltage regulator can be evaluated by load regulation, line regulation, power supply rejection, quiescent current, power efficiency, current efficiency, transient response, dropout voltage and frequency response. The frequency response analysis is closely related to the overall system stability. It will be discussed and analyzed in chapter 5.

Table 1.2 Comparison of voltage regulator topologies

Voltage Regulator	Speed	Output	Area	Power Efficiency	Complexity	Noise	Isolation
Linear	Fast	Step Down	Small	Low	Moderate	Low Noise	Good
Switching	Slower	Step Up/Down	Large	High	Complex	High Noise	Good
Shunt	Fast	Step Down	Small	Low	Simple	High Noise	Poor

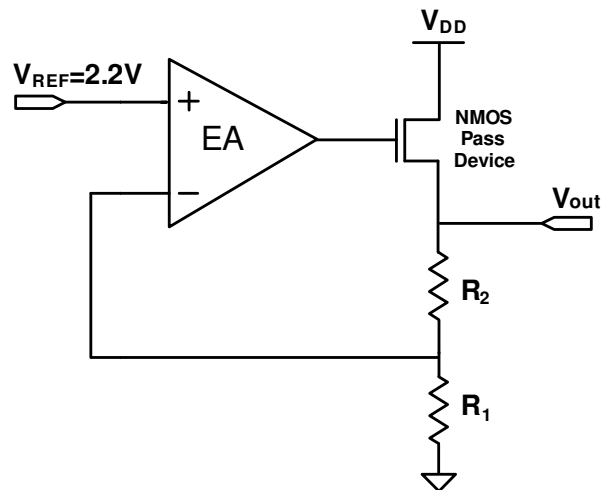


Figure 1.4 Conventional linear voltage regulator

1.4.1. Load Regulation

The load regulation is defined as the amount of the output voltage variation, ΔV_{out} due to the load current variation, ΔI_{Load} . It can be expressed as,

$$\Delta V_{out} = R_{out} \cdot \Delta I_{Load} \quad (1.1)$$

$$R_{out} = \frac{\Delta V_{out}}{\Delta I_{Load}} = \frac{R_{out_OL}}{1 + A_{OL} \cdot \beta} = \frac{R_{out_OL}}{1 + A_{OL}} \cdot \left(1 + \frac{R_2}{R_1}\right) \quad (1.2)$$

where R_{out_OL} represents the open loop output resistance, A_{OL} is the open loop gain of the voltage regulator, and β represents the feedback factor. According to equation (1.2), the load regulation can be improved if the open loop gain is large and the closed loop gain is small.

1.4.2. Line Regulation

The line regulation is defined as the amount of output voltage variation, ΔV_{out} , due to the input voltage variation, ΔV_{in} . It can be expressed as,

$$Line_regulation = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (1.3)$$

$$Line_regulation = \frac{1}{1 + g_{m_pass} A_{OL} \cdot \beta} \cdot \frac{R_L}{R_{o_pass} + R_L} \quad (1.4)$$

where R_L represents the load resistance, g_{m_pass} is the transconductance of the pass transistor, R_{o_pass} represents the output resistance of the pass transistor. The line regulation can be improved with high open loop gain and high loop bandwidth.

1.4.3. Power Supply Rejection

The power supply rejection (PSR) is also a very important specification for a voltage regulator design. The purpose of a voltage regulator is to supply a noiseless constant DC voltage source to subsequent analog circuits. PSR refers to the ability of voltage regulator to reject the supply ripple. From the ref [18] and [19], the PSR can be defined as,

$$PSR = \frac{V_{out}}{V_{dd}} \cong \frac{1}{A_{OL} \cdot \beta} \text{ at DC/LF} \quad (1.5)$$

$$PSR = \frac{V_{out}}{V_{dd}} \cong 1 \quad \text{at UGF} \quad (1.6)$$

$$PSR = \frac{V_{out}}{V_{dd}} \cong \frac{R_{ESR}}{R_{ESR} + R_{o_pass}} \text{ at HF} \quad (1.7)$$

From equation (1.5), it is obvious that the PSR at DC and low frequency range is inversely proportional to the open loop gain of the voltage regulator. Therefore, the PSR can be improved by increasing the DC open loop gain. It can be seen from equation (1.6) that the PSR is approximately unity while frequency is beyond the unity gain frequency (UGF) of the error amplifier. This means that the linear regulators cannot reject the supply ripple at this frequency range. At high frequency, equation (1.7) represents that the large output capacitor shunts the feedback resistors to ground or very low impedance. During this frequency range, the PSR can be determined by the output resistance of the pass transistor and the ESR (Equivalent Series Resistance) of the output capacitor [18, 19].

1.4.4. Quiescent Current

The quiescent current is the current consumed by the voltage regulator when there is no load current drawn from the output voltage node (no load/zero load) of the regulator. This current consumption may come from the voltage reference circuit, the error amplifier, the pass transistor, the current reference circuit, the frequency compensation circuit, the pre-regulator, etc. In other words, the quiescent current is the current when the voltage regulator is turned off. A lower quiescent current can improve the current efficiency and extend the battery life. The low quiescent current consumption is desired in the high temperature analog integrated circuit design as well, because more current consumed by the circuit itself will increase the need of using heat sink and thus the total cost. Therefore, low quiescent current design considerations have been applied in this research.

1.4.5. Power Efficiency

The power efficiency is defined as the ratio of the output power, P_{out} , to the input power, P_{in} as,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_{Load}}{V_{in} \cdot I_{in}} \quad (1.8)$$

where V_{in} and I_{in} represent the input voltage and current, respectively. V_{out} is the output voltage of the regulator, and I_{Load} is the load current. Power efficiency is a very important specification of a voltage regulator design. Higher efficiency will save more power, extend the battery life and minimize the heat sink for high temperature applications.

1.4.6. Current Efficiency

The current efficiency is defined as the ratio of load current, I_{Load} , to the input current, I_{in} as,

$$\eta_{current} = \frac{I_{Load}}{I_{in}} = \frac{I_{Load}}{I_{Load} + I_q} \quad (1.9)$$

where I_{in} represents the input current of a voltage regulator, input current is $I_{Load} + I_q$, where I_q is the quiescent current. Low quiescent current design can improve the current efficiency when the voltage regulator is operating at light load condition (I_{Load} is small). The linear regulator will suffer from low current efficiency during light load condition. At heavy load (i.e. 100 mA), the current efficiency can be approximated to be 100%.

1.4.7. Transient Output Voltage Variation

The transient output voltage variation is the output voltage variation due to the load current variation as shown in Figure 1.5, and can be expressed as,

$$\Delta V_1 \approx \frac{\Delta I_{Load}}{C_{out}} \Delta T_1 + \Delta V_{ESR} \quad (1.10)$$

$$\Delta V_{ESR} \approx \Delta I_{Load} \cdot R_{ESR} \quad (1.11)$$

The output voltage variation can be alleviated by low ESR value, large output capacitance and fast system response time, ΔT_1 , where ΔT_1 is inverse proportional to the closed loop bandwidth of the regulator. ΔT_1 can be represented as [14, 15, 16],

$$\Delta T_1 \cong \frac{0.37}{BW_{CL}} + C_{para2} \left(\frac{\Delta V_{para2}}{I_{buffer}} \right) \quad (1.12)$$

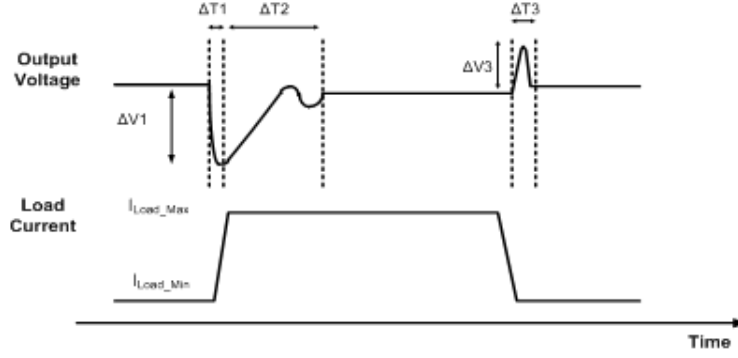


Figure 1.5 The transient output voltage waveform of a linear regulator

From equation (1.12), it is evident that the fast response can be achieved by increasing the closed loop bandwidth. The fast response will improve the supply regulation of regulator load. The AC specifications of the regulator are all dependent on the loop dynamics and stability. To maintain the system stability, the phase margin of a linear regulator is desired to be at least 45 degree or greater. The PM (phase margin) refers to how much margin in phase exists at unity gain frequency.

1.4.8. Dropout Voltage

Dropout voltage is the minimum voltage difference between the input and output voltages where the voltage regulator stops to regulate [14] and can be expressed as,

$$V_{Drop_out} = I_{Load} R_{on} \quad (1.13)$$

where R_{on} is the switch on resistance of pass transistor, and the pass transistor is operating in the linear region. Low dropout (LDO) voltage regulator is widely used in cellular phone, MP3 player, consumer electronics, because the low dropout voltage between the input and the output voltages can increase the power efficiency of the LDO voltage regulator which can be compared with switching mode voltage regulator while the dropout voltage is minimized. (i.e. $V_{in} = 1.2V$, $V_{out} = 0.9V$).

1.5 Selection of Pass Transistor

When designing the high temperature linear voltage regulator or the linear voltage regulator, the type of pass transistor needs to be decided at the very beginning of the design process [16]. The pass transistor can be selected from BJT or MOSFET device according to the devices available from the process technology. Most of low dropout (LDO) voltage regulators utilize PMOS as the pass transistor because the output voltage, V_{out} , can be as high as $V_{in} - V_{Drop_out}$. This results in higher power efficiency, but the penalty is the complexity of frequency compensation scheme and slower transient response time. In this case, the PMOS pass transistor acts like a common source amplifier and two amplifier stages exist (error amplifier and pass transistor) inside the feedback loop.

BJT device and BJT Darlington pair could be utilized as pass transistor as well. The BJT device is a current driven device and has larger transconductance compared to the MOSFETs. When using BJT as the pass transistor, the error amplifier needs to provide sufficient current to the base of the BJT. If the BJT has high current gain, β , the required amount of base current of a regulator system can be reduced.

Darlington pair can help reduce the amount of base current needed from the error amplifier, because $I_c = \beta^2 \cdot I_b$. BJT and BJT Darlington pair are very good choices for the pass transistor of a linear voltage regulator if the fabrication process technology offers high current gain (β), high breakdown voltage of V_{CE} , and the quiescent current is not the major concern.

In addition to the device characteristics, the selection of the pass transistor needs to follow the design specification. The input voltage range for this work is between 10V to 30 V, thus the PMOS pass transistor is not suitable because the high input voltage is applied to the source terminal.

For preventing the device breakdown, the gate voltage of the PMOS pass transistor needs to be maintained within $V_{in} - V_{sg_breakdown}$ ($V_{in} - 5.5V$).

Obviously, the high voltage MOSFET needs to be used for designing an error amplifier if PMOS pass transistor is selected. Using the high voltage MOSFET will also increase the power dissipation (high voltage at the output of error amplifier) and chip area. Meanwhile, the BJT and BJT Darlington pair are also not suitable because their input voltages exceed the V_{CE} breakdown voltage given by the foundry model, and higher quiescent current consumption may place another limitation if the current gain of the BJT is not large enough (i.e. 100).

According to the design specification, a HV NMOSFET (DMOS) is the only choice for the pass device of the regulator. The input voltage specification can be taken care of by using the high voltage NMOSFET (DMOS) offered by the foundry. In addition, the high voltage DMOSFET has low on-resistance at elevated temperatures and the leakage current at elevated temperatures is reduced as well.

Since the input voltage is connected to the drain terminal of the HV NMOSFET, the error amplifier can be designed using regular 5V MOSFETs utilizing folded-cascode techniques. Hence, the power consumption is lower than that of the regulator using high voltage PMOSFET as the pass transistor. Figure 1.7 summarizes the selection criteria of the pass transistors.

Device	NMOS	PMOS	NPN	PNP
HV Capability	Up to 80V	Up to 80V	12V	25 V
Comment	Suitable No HV device needed in amplifier design Low power consumption Fast Response	Not Suitable High Vin Need HV Amplifier High power consumption (HV Device)	Not Suitable High Vin (HV Device) Fast Response	Not Suitable High Vin (HV Device) High quiescent current

Figure 1.6 Selection criteria of pass transistors of high temperature linear voltage regulator

1.6 Silicon-on-Insulator Technology

The bulk CMOS LDO voltage regulator is not suitable for applications in the temperature above 150°C because the leakage current of CMOS increase by approximately five orders of magnitude. The leakage current at temperature beyond 150°C is given by,

$$I_{diff}(V_r, T) = q \cdot A \cdot \frac{D_{n,p} \cdot n_i^2(T)}{L_{n,p} \cdot N_{a,d}} \quad (1.14)$$

Where V_r	Applied junction reverse bias voltage,
T	Temperature
A	Effective p-n junction area
$D_{n,p}$	Electron and hole diffusion constants
$L_{n,p}$	Electron and hole diffusion lengths
n_i	Intrinsic carrier concentration
$N_{a,d}$	Acceptor and donor doping concentrations

Equation (1.14) represents the diffusion leakage current which is the dominant source of the leakage current when the temperature is increased beyond 150°C [25]. Increased leakage current will degrade the DC voltage gain of the error amplifier and will change the operating point. Hence, the increased leakage current with increasing temperature will cause latchup which may also lead to catastrophic failure of the regulator system.

Leakage current can be minimized by layout or SOI process technology. The SOI process technology can lower leakage current by approximately three orders of magnitude compared to the bulk CMOS process [8].

Figure 1.8 shows the simulation of the leakage currents for CMOS and SOI processes. The solid line represent the leakage current over temperature of the bulk CMOS process technology, while the dotted line represents the leakage current over temperature of the SOI process. This simulation confirms that the SOI processes technology is a better process technology for high temperature analog integrated circuits.

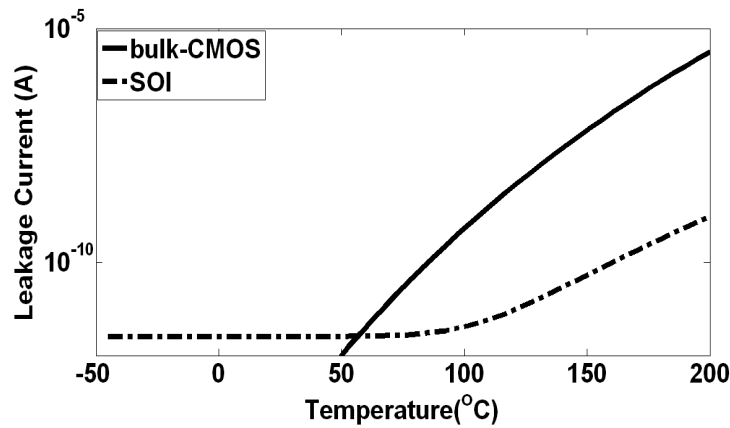


Figure 1.7 The simulation of leakage current over temperature bulk-CMOS and SOI Process.

The Silicon-on-Insulator technology provides a buried oxide layer inserted between the surface (Si Layer) and the silicon substrate [4, 98, 99] as shown in Figure 1.9. The leakage current of the SOI devices is significantly reduced because the area of PN junction is reduced. Hence, the latch-up susceptibility is reduced as well [4]. With the reduced leakage current and increased latch-up immunity, the SOI technology can extend the operating temperature up to 300°C [4, 46].

In addition, the parasitic capacitance, the threshold voltage variation over temperature and the short channel effect of the SOI devices are also smaller compared to the bulk CMOS [4, 98, 99].

Furthermore, the FD-SOI (fully-depleted) device suppresses the quasi-neutral regions which exist in the PD-SOI (partially-depleted) device. Thus only the generation current contributes to the junction leakage current [24]. Nevertheless, the high temperature circuit design techniques need to be employed to take care of the problems related to threshold voltage shift, mobility degradation etc. over increasing temperature.

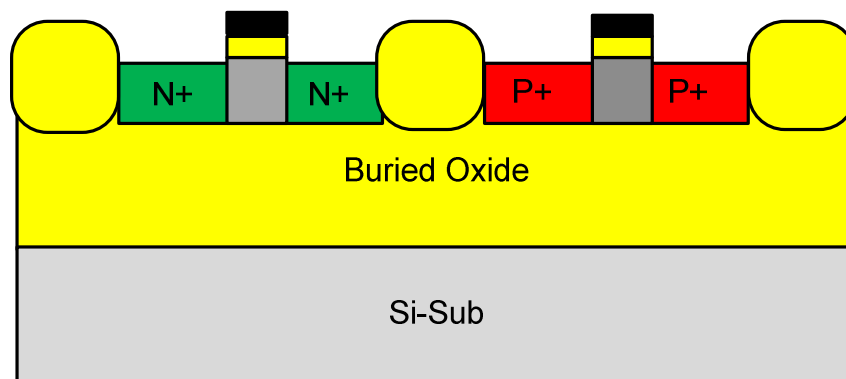


Figure 1.8 The cross-section of a SOI Process.

CHAPTER 2

Literature Review

2.1 Introduction

Linear voltage regulator is a key component for any consumer electronics. With the CMOS process technology continuously shrinking down, the device breakdown voltage can approach as low as 1.2 V. In this situation, the linear voltage regulator can improve its efficiency by adopting LDO topology and operating at heavy load condition. A considerable volume of literatures on LDOs has been published in the past decades but very few of them are related to high temperature linear voltage regulator. This chapter will discuss the selected literature of the LDO voltage regulator and the high temperature linear voltage regulator. Section 2.5 discusses the problem statements of the high temperature linear regulator.

2.1.1. Low Dropout Voltage Regulator

The most widely used linear voltage regulator topology used today is low dropout voltage regulator (LDO). In the LDO, a PMOSFET pass transistor is utilized because the voltage difference between the input and the output is only a $V_{SD,SAT}$ drop. The high impedance node due to the output resistance seen from the drain of the PMOSFET pass transistor creates another pole at low frequency and the two poles inside a negative feedback loop tends to create an unstable response.

Therefore, the frequency compensation scheme needs to be carefully selected. Meanwhile, low quiescent current, small chip area, better power efficiency and low cost

(economical bulk CMOS process) are the main reasons for the LDOs to become popular in research and industrial applications.

2.1.2. High Temperature Linear Voltage Regulator

The SOI process technology is a better solution for designing high temperature analog integrated circuits. In addition, to design high temperature linear voltage regulator by taking advantage of using SOI process technology, high temperature design techniques also need to be utilized. The high ambient temperature will create problems for the analog electronic circuits, such as the need for preserving the stability of the amplifiers over wide temperature variation, stabilization of the pole locations, maintaining a constant power consumption of the amplifiers, reducing the gain degradation of the amplifier with temperature and reduced speed [4].

The system stability of the voltage regulator over wide temperature is extremely important. For maintaining the system stability, the temperature stable current reference is needed to bias the amplifier of the regulator because the line and load regulations are closely related to the gain of the amplifier. DC and AC analyses over wide temperature range are desired, and the selection of the off-chip output capacitance is very critical to stability, performance and cost of the entire system.

The ESR of the output capacitor will generate a LHP zero for compensation purpose. Thus LHP zero will add more phase margin to the AC response of the regulator. The ESR value dictates the transient voltage variation of the regulator. Besides the wide loop bandwidth will minimize the duration of the voltage droop during load current switching.

In addition, the reduced quiescent current consumption is also a challenging task for this research. A linear voltage regulator suffers from poor efficiency during zero load condition. A g_m/I_d versus normalized drain current curve can predict the quiescent current needed for

designing the error amplifier. The lowest quiescent current can be achieved when biasing a transistor in weak inversion region, but the tradeoff is the speed of the amplifier.

2.2 Design Examples in Prior Arts

2.2.1. Design Examples -Rincon-Mora

In 1998 Rincon-Mora *et al* published a design of a voltage regulator [14]. This design of a CMOS LDO voltage regulator targets portable electronic application. The minimum supply voltage is 1.2 V and the output voltage is 0.9 V. The maximum load current can reach up to 50mA. This regulator only consumes 23 μ A quiescent current and the error amplifier utilizes frequency shaping amplifier scheme. A pair of pole and zero has been added at the output node of the error amplifier for the purpose of shaping the frequency response.

A NPN BJT voltage buffer is inserted between the output of error amplifier and the P-type pass transistor. This NPN BJT voltage buffer will separate the pole locations at the output of the error amplifier and the parasitic pole due to large P-type pass transistor. The NPN BJT has larger transconductance compared to CMOS transistor. Therefore, the parasitic pole will be moved toward a higher frequency compared to the MOSFET based voltage buffer. If this buffer is not added, the high impedance node exists at the output of the error amplifier and the high parasitic capacitance of pass transistor (C_{gs}) will create a low frequency pole close to the dominant pole which tends to make the system unstable.

In addition, a current efficiency buffer mirrors a fractional current from the pass transistor. This will push the parasitic pole associated with the large pass transistor to higher frequency when regulator is sourcing a huge amount of current (heavy load). The drawback of

this design is that the passive components for generating pole/zero pair take huge chip area, and the biasing technique may not be suitable for high temperature applications.

2.2.2. Design Examples - Bontempo

Bontempo published a design of a voltage regulator in 2001 [26]. This design is a BCDMOS (Bipolar, CMOS, DMOS) LDO voltage regulator targeted for microprocessor, cellular phone and automotive applications. The minimum supply voltage is 2 V and output voltage is 1.8 V, its maximum load current can reach 4 A. This regulator consumes 200 μA quiescent current, standby current is only 2 μA , and the pass transistor utilizes NMOSFET.

The error amplifier of this LDO is implemented using NPN bipolar transistors. A compensation network, in other word, a zero has been added at the output node of the error amplifier for compensating the high frequency pole associated with the load capacitance (C_L) and the load resistance (R_L). A BJT voltage buffer is inserted between the output of error amplifier and the N-type pass transistor. This BJT voltage buffer will separate pole locates at output of error amplifier and parasitic pole due to large N-type pass transistor. The parasitic pole associated with the parasitic capacitance at the gate of the pass transistor is ignored, the purpose of this buffer is the same with Rincon-Mora's design, and this technique is also called buffer impedance attenuation (BIA).

A charge pump is used to boost up the supply voltage for the error amplifier and the voltage buffer. This will increase the gate overdrive voltage of the pass transistor and a new trimming technique is applied to obtain high precision output voltage. The drawback of this scheme are that the charge pump and passive components for generating LHP zero add chip area overhead, the stability is limited at a certain range(0.2A~5A) and the transient response time is slow (8 μs).

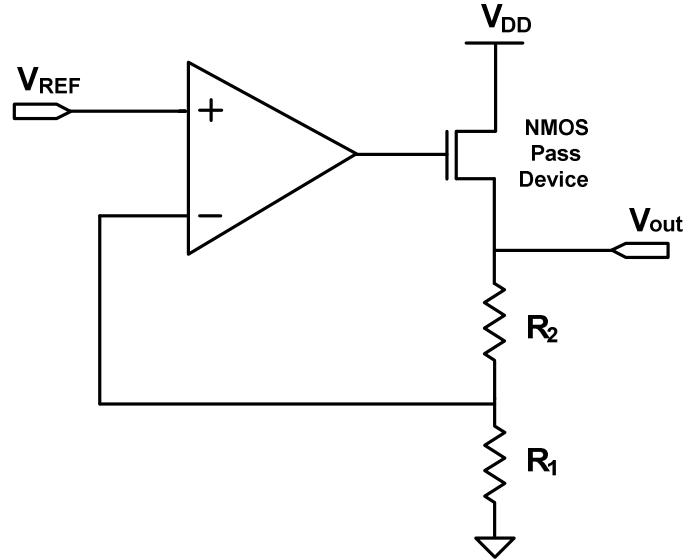


Figure 2.1 Block diagram of Bontempo's design

The stability could be a problem at ultra light load condition (less than 1 mA) due to the fact that the compensation scheme sets ESR zero at 8 KHz and it cannot track 2nd pole which is proportional to the transconductance of the pass transistor. The transient response (8 μ s) time can be improved by extending the dominant pole to higher frequency while a biasing technique may not be suitable for high temperature application.

2.2.3. Design Examples –Holter, High Temperature

Holter *et al* reported a high temperature regulator design in 1997 [27]. This design has been fabricated in 1.2 μ m BiCMOS process, and is targeted for oil well applications. The output voltage of this circuit is externally adjustable from 5 V - 12 V. The maximum load current of this regulator can reach 250 mA and consumes 2.7 mA quiescent current, while the pass transistor utilizes NPN Darlington pair. The NPN Darlington pair pass transistor occupies 50% of the chip area. In addition, power-down, watch-dog and reset function are included in this design.

The error amplifier design had not been discussed in this paper. The dominant pole can be placed at the output of voltage regulator or the base terminal of the NPN Darlington pair. Stability could be a problem at ultra light load condition (under 1 mA) due to the compensation scheme only relying on ESR zero. Transient response time and transient output voltage variation are not discussed as well in this literature. Large (2.7 mA) quiescent current may help to guarantee the stability of the system. This voltage regulator reported functional circuits at up to 290°C while the temperature specification of this regulator is between 0°C to 200°C.

2.2.4. Design Examples - Ohme, High Temperature

Ohme published a design of high temperature voltage regulator in 1998 [28]. This design is fabricated in SOI CMOS process. This work proposed a control circuit for high temperature linear regulator, and an external NMOS pass transistor is incorporated with this control circuit to configure a high temperature voltage regulator. This regulator is capable of operating at -55°C to 225°C and 300°C for short term operation. The input and output voltage ranges are from 8 V - 30 V, and 5 V, 10V, 15V, respectively. The maximum load current of this regulator can reach 500 mA, and it consumes 2 mA quiescent current, and the pass transistor utilizes an external (off-chip) NMOSFET.

An on-chip regulator supplies 5 V to the error amplifier, the voltage reference and the biasing circuit. However, the error amplifier design, stability and transient response have not been discussed in this literature. A temperature independent biasing circuit is used to bias the error amplifier. The disadvantage of this design is that the external pass transistor increases the cost since a special process technology is needed to implement the low V_t MOSFET.

2.3 Summary of Prior Arts

In addition to the designs reviewed in the previous sections, there are still some brilliant designs in CMOS LDO voltage regulator, but they will not be reviewed in detail. The performances and FOM (Figure of Merit) of these designs are summarized in Table 2.1

Since each design adopts different architecture, different compensation topology, different process and supply voltage, it is very hard to justify which design is the best. For example, the low quiescent current may cause long transient response time and the capacitorless LDO may suffer from large transient voltage variation, and some design may not guarantee the stability of the system particularly at ultra light load conditions. For these reasons, the figure of merit (FOM) is used to evaluate similar designs. The FOM is given by,

$$FOM_1 = T_R \frac{I_q}{I_{Load_max}} = \frac{C_{out} \cdot \Delta V_{out}}{I_{Load_max}} \cdot \frac{I_q}{I_{Load_max}} \quad (2.2)$$

where T_R is the transient response time of the voltage regulator during load-dumps, I_q represents the quiescent current, I_{Load_max} is the maximum current the voltage regulator can source to the load, C_{out} and ΔV_{out} are the output capacitor and transient output voltage variation (voltage droop), respectively, during load switching condition. The lower the FOM1 value indicates the better performance of a voltage regulator.

FOM1 did not take process technology into account for evaluating the performance of the regulator. Reference [29] proposed FOM2 which can remove the process dependence while comparing performance of the regulator. FOM2 can be defined by,

$$FOM_2 = \frac{FOM_1}{T_G} \quad (2.3)$$

where, T_G represents the fan-out of four delays. However, the linear voltage regulator can be designed using different topology, and the desired performance and the design specification may

be different in different applications, and a fair comparison among these linear regulators remains a challenging task.

Figures 2.2-2.5 illustrate FOM1, FOM2 with respect to the transient voltage droop, transient response time, respectively of the regulator. FOM1 and FOM2 of this work are calculated from the CADENCE SPECTRE simulation result.

Table 2.1 Literature review of published linear voltage regulator

Ref.	H.T.	Pass Device	I _q (uA)	I _{Load} (max, mA)	Area (mm ²)	Process (μm)	V _{DD} (V)	V _{out} (V)	T _r (us)	ΔV _{out} (mV)	Cou _t (uF)	FOM 1 [ns]	4 gate delay[ns]	FOM 2
Rincon-Mora[9]	NO	PMOS	23	50	1.4	2um BiCMOS	1.2	0.9	1.2	19	4.7	8.2	0.51	16
Den Besten[30]	NO	NMOS	750	300	1	0.5um CMOS	5	3.3	0	400	0.00018	0.00060	0.13	0.0047
Bontempo[26]	NO	NMOS	200	4000	5	0.6um BCD MOS	2	1.8	8	220	100	0.28	0.15	1.8
Al-Shyookh[31]	NO	PMOS	20	200	0.264	0.35um CMOS	3.35	3.15	0.27	54	1	0.027	0.09	0.3
Leung[42]	NO	PMOS	38	100	0.31	0.6um CMOS	1.5-4.5	1.3	2	150	10	4.9	0.15	32
Hazucha[29]	NO	PMOS	6000	100	0.098	0.09um CMOS	1.2	0.9	0.00054	90	0.0006	0.032	0.023	1.4
Chava[32]	NO	PMOS	25	160	N.A	0.5um CMOS	3.3	2.8	2.75	200	2.2	0.43	0.13	3.3
Milliken[33]	NO	PMOS	65	50	0.29	0.35um CMOS	3	2.8	15	90	0.1	19.5	0.09	216.67
Strik[34]	NO	PMOS	20	150	0.28	0.5um CMOS	5	3.3	35	60	1	4.4	0.13	33.8
Oh[35]	NO	PMOS	100	50	N.A	0.25um CMOS	2~2.5	1.5~1.97	0.6	30	0.05	1.2	0.064	18.75
Lau[36]	NO	PMOS	100	100	0.13	0.35um CMOS	1.2~3.3	1	50	30	10	50	0.09	555
Lin [37]	NO	PMOS	27	150	0.41	0.35um CMOS	2	1.8	5	70	1	0.9	0.09	10
Lin[38]	NO	PMOS	24	138	N.A	0.35um CMOS	2.7~5.5	2.5	2	100	1	0.35	0.09	3.89
Man[39]	NO	PMOS	1.2	50	0.09	0.18um CMOS	1	0.9	2.8	400	0.1	0.067	0.046	1.46
Lam[40]	NO	PMOS	4~164	50	0.053	0.35um CMOS	1.05	0.9	0.132	6.6	1	0.01	0.09	0.1
Lu[41]	NO	PMOS	45	150	0.33	0.35um CMOS	2~5	1.8	4	170	1	1.2	0.09	13.3
Holter[27]	YES	NPN Darlington	2700	250	5.25	1.2um BiCMOS	>12	5-12	N.A	N.A	N.A	N.A	0.31	N.A
Ohme[28]	YES	NMOS External	2000	500	N.A	0.8um Honeywell SOI	8-28	5	N.A	N.A	N.A	N.A	0.2	N.A
This work	YES	NMOS	600	200	3	0.8um SOI	10-45	5.375	1.2	50	10	3.6	0.2	18

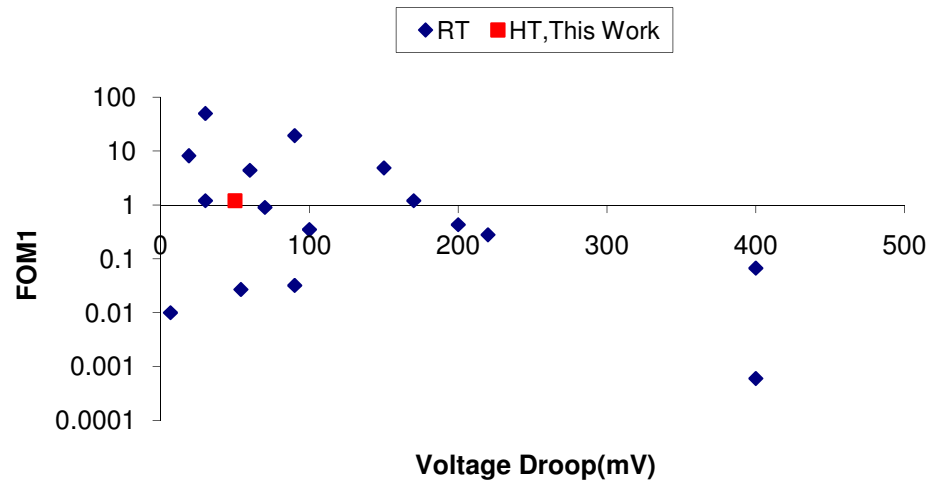


Figure 2.2 FOM1 versus voltage droop

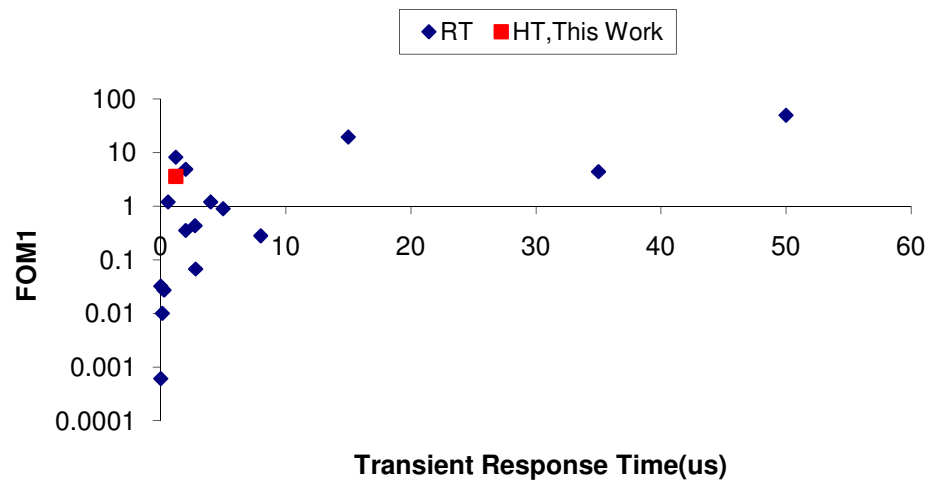


Figure 2.3 FOM1 versus transient response time

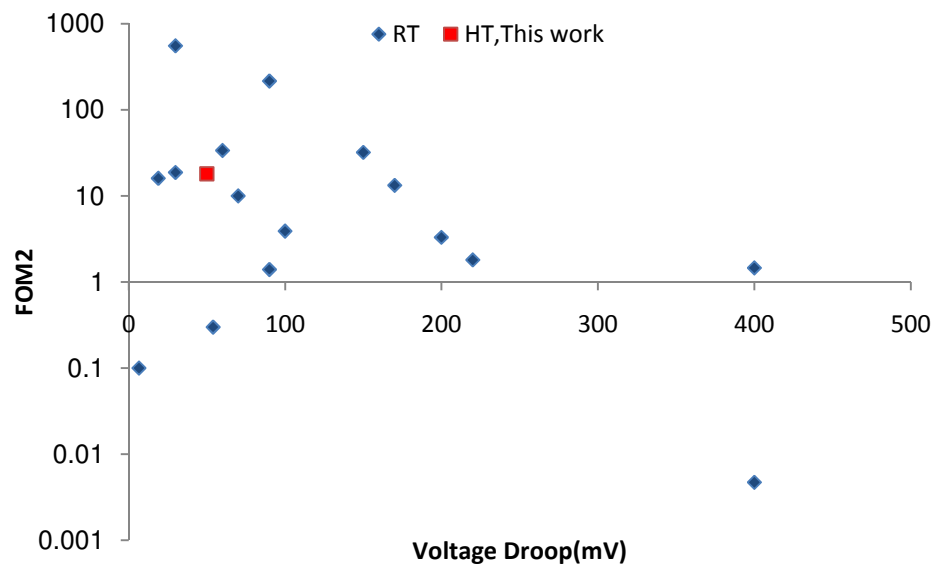


Figure 2.4 FOM2 versus voltage droop

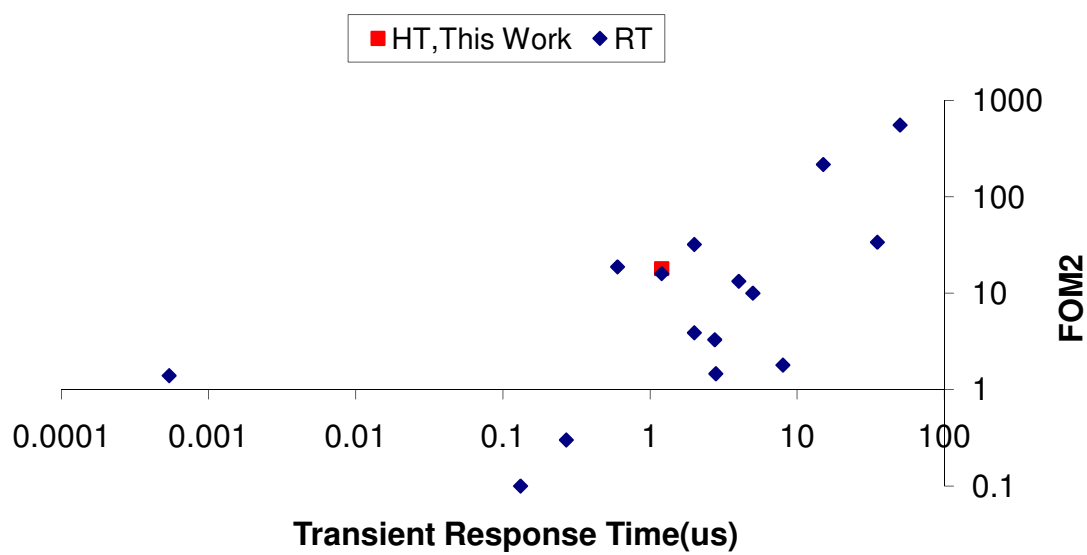


Figure 2.5 FOM2 versus transient response time

2.4 Problems in High Temperature Linear Voltage Regulator Design

Since analog circuits are very sensitive to noise, a low-noise voltage regulator is required to offer a clean power supply to the analog circuitry. The linear regulator edges its counterpart switching mode voltage regulator in the application for portable device, consumer electronics, and system-on-chip (SoC). Most of published literature in the area of linear voltage regulator have focused on conventional CMOS temperature range (below 125⁰C) and have utilized bulk CMOS fabrication process technology. All these published literatures emphasize on low dropout voltage (LDO) due to the low quiescent current and power efficiency considerations. The PMOS pass device is utilized for reducing the dropout voltage. In addition, the maximum input voltage of these voltage regulators are below 5V, and thus lower power dissipation can easily be achieved in LDO voltage regulator configurations.

With the increasing demand for high temperature automotive electronics, high temperature analog integrated circuits operating at elevated temperature (over 200⁰C) are needed. Obviously, the previously published literature did not address the problems and design considerations for linear regulator operating at elevated temperatures. The primary objective of this research is to demonstrate a high temperature linear voltage regulator for high temperature gate driver circuit.

The following problems need to be thoroughly addressed in the process of designing linear voltage regulators for high operating temperatures:

1. High temperature effects of MOSFETs include mobility degradation, threshold voltage degradation, increase of leakage current (proportional to the effective PN junction area), transconductance degradation, gain bandwidth degradation, increase of leakage conductance (gain degradation). These effects degrade the performance of the amplifier at elevated

temperatures. While operating at elevated temperatures, the conventional CMOS LDO voltage regulator suffers from increased leakage current leading to gain degradation and biasing point shift.

2. The wide range of load current variation in magnitude typically exceeds three decades ($\mu\text{A} \sim \text{mA}$) and fast (nano second range) switching load current impulse increases the magnitude of voltage droop at the output node of the regulator. Selection of the most appropriate compensation technique and the architecture of the voltage regulator are dictated by the device parameters of the fabrication process technologies. The voltage regulator needs to maintain the system stability over temperature. Meanwhile, the output voltage needs to be independent of the loading condition within the design specification of the load current (200mA).

3. Since the threshold voltage is temperature dependent, the inversion coefficient (g_m/I_d) methodology needs to be applied in designing high temperature OTA. The performance of the OTA dictates the overall performance of the linear voltage regulator. The inversion coefficient method offers more meaningful insight of designing amplifier, especially for OTA targeted to operate at elevated temperatures.

4. To determine the specification of the voltage regulator, noise, PSR, CMRR, bandwidth of error amplifier, line regulation, load regulation, open loop gain, offset voltage and transient response (output voltage droop) need to be considered. Estimation of the transient response time requires detailed information on the specification (i.e.: capacitance of output capacitor, variation of load current, etc.) of the voltage regulator

5. Selection of the most appropriate error amplifier topology for designing linear voltage regulator is another key component of the design. The DC gain of the error amplifier will

determine the performance of line and load regulations, transient response, PSR (Power-Supply Ripple Rejection) etc.

6. The load current profile is very difficult to predict. It could be a constant DC current, a square wave current or a dynamic current pulse [16]. The dynamic current pulse normally comes from the transient current of the digital inverter buffer. This is because the huge parasitic capacitance exists at the gate of the inverter buffer and the current drivability is insufficient from previous stage which slows down the charging time of the parasitic capacitor. It leads to turning on of both the PMOS and the NMOS simultaneously inside the inverter buffer. Hence, a large and a fast dynamic current pulse is drawn from voltage supply (voltage regulator) as shown in Figure 2.7.

7. Minimizing the usage of the HV MOSFET in the design of matching sensitive analog circuit (error amplifier, bandgap voltage reference) is also an important consideration. The HV MOSFETs are physically larger than regular 5V MOSFETs. The HV MOSFET can handle high drain-source voltage, but the gate-source breakdown voltage remains the same (5.5V) as the regular 5V MOSFETs.

8. Reducing the quiescent current of the voltage regulator is another design consideration. The higher quiescent current will reduce the efficiency of the voltage regulator and increase the power consumption. The average power dissipation by voltage regulator must be limited to less than 15% of average power consumed by the gate driver circuit.

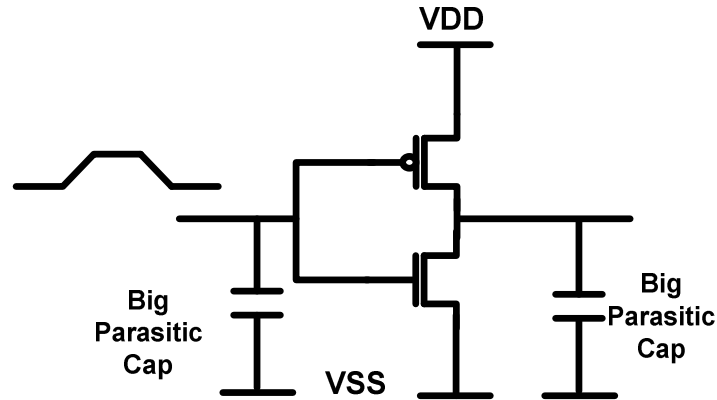


Figure 2.6 The schematic of the Inverter Buffer

2.5 Problem Statement

This section introduces the problem statement for of the high temperature linear regulator design. The problems of load regulation optimization in CMOS voltage regulator powering digital system in high temperature application are listed below:

- ❑ Load regulation is impacted by the loop bandwidth over wide load current
- ❑ Synchronization of the digital systems results in wide load current variation
 - *Switching at clock edge(fast load-dump, worst transient)*
- ❑ Transient load current complicates load regulation – requiring a wide loop bandwidth from the voltage regulator
 - *Fast recovery/settling time*
- ❑ Due to the mobility reduction in high temperature, wide bandwidth is difficult to achieve in CMOS linear voltage regulator
- ❑ Lack of good regulation may result in digital fault
 - *E.g. Undetermined logic state*

Table 2.1 summarizes the problems and challenges in designing high temperature linear voltage regulator.

Problem	Possible Solutions	Solution	Reason
High Input Voltage (10V-30V)	High Voltage Fabrication Process is needed.	SOI Fabrication Process	HV Device(DMOS)
High Temperature (up to 200°C)	1.High Temperature Fabrication Process is needed 2. CMOS Process with high temperature model	SOI Fabrication Process	Minimize leakage current at high temperature
Selection of Error Amplifier	1.Two-Stage OTA 2. Folded-Cascode OTA	Folded-Cascode with two supply voltage	Good ICMR Self-Compensation Better PSRR
Selection of Pass Device	BJT (PNP/NPN) MOSFET(PMOS/NMOS)	HV NMOSFET	Fast Response Suitable for system's specification
Compensation	1.Capacitorless with Miller Compensation 2.Large Output Capacitor 3.Buffer Impedance Attenuation	Large output capacitor & Buffer Impedance Attenuation	Compensation and reduce voltage droop
Power Consumption	Minimized quiescent current	Lower quiescent current	Extend battery's life
Temperature Stable Biasing	Internal Biasing External Biasing	Internal Biasing	Stability and reduce off-chip component
Output voltage from shunt pre-regulator is temperature dependent	Supply insensitive biasing	Supply-Insensitive biasing	Reduce current reference's temperature sensitivity
Line/Load Regulation	High performance OTA	Inversion coefficient g_m/I_d technique	Reduce gain degradation over temperature
Matching of HV MOSFET	Reduce usage of HV MOSFET in matching sensitive analog circuit	Shunt Pre-Regulator	Reduce input voltage

CHAPTER 3

High Temperature OTA and Inversion Coefficient

An error amplifier (operational transconductance amplifier (OTA)) is the fundamental building block of the linear voltage regulators. Its higher open-loop gain enhances the overall performance of a linear regulator. The lower quiescent current consumption of the OTA is very important for improving the current efficiency of the linear regulator and reducing the power dissipation. High temperature linear voltage regulators in SOI and BiCMOS processes, respectively, have been presented in [27, 28]. However, both lack treatments in addressing the design methodology of an OTA at high temperature.

This work presents a high temperature OTA design based on the inversion coefficient design methodology. In addition, temperature stable current reference will maintain the stability of the power consumption of the OTA over a wide temperature variation. Section 3.2 introduces high temperature OTA design using inversion coefficient (g_m/I_d). Section 3.3 investigates the mismatch and the offset voltage of the OTA, and lastly the noise analyses of the OTA are discussed in section 3.4.

3.1 OTA Topology

A PMOS input pair folded cascode OTA topology as shown in Figure 3.1, has been selected as an error amplifier in this work. The PMOS input pair offers wider ICMR (input common-mode range) and empirically lower flicker noise compared to its NMOS counterpart [59]. By cascading the current mirror load at the output node, a folded cascode OTA has higher CMRR, power supply rejection ratio and DC open loop gain than a simple single stage OTA

topology. (See Figure 3.2.) The voltage gain of a single stage OTA is the product of the transconductance of the input pair and the output resistance of the output node. The DC open loop voltage gain of the folded cascode topology is boosted up by the cascode current mirror. The DC open loop gain of a folded cascode OTA can be expressed as,

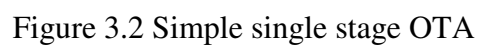
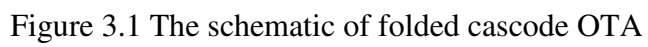
$$Av = g_{m_in} \cdot (R_{o_ncascode} // R_{o_pcascode}) \quad (3.1)$$

where g_{m_in} represents the transconductance of the input pair, $R_{o_ncascode}$, $R_{o_pcascode}$ represent the output impedance of the NMOS cascode and the PMOS cascode current mirrors, respectively.

The input pair and the cascode current mirror load do not share the same supply voltage as a conventional folded cascode OTA. The PMOS input pair connects to a 5.6V voltage from a shunt pre-regulator. The cascode current mirror needs higher supply voltage from the shunt pre-regulator to increase the gate overdrive voltage headroom. The higher the gate overdrive voltage, the more current can be sourced from the pass transistor. The voltage variation at the output node may swing from $2V_{DS,SAT}$ to $(9V - 2V_{SD,SAT})$. Therefore, HV (25V) NMOS (M_6 , M_7) are needed to avoid device breakdown due to excess voltage stress on the drain-source terminal (5.5V). The transistors $M_1 \sim M_5$ and $M_8 \sim M_{11}$ are regular LV MOSFETs.

The cascode current mirror load is biased by an on-chip current reference which offers a stable reference current over temperature.

Folded cascode OTA topology consumes more power than a simple single stage OTA due to the bias current needed to flow into M_4 and M_5 is between the range of $I_1 \sim 2I_1$. The other penalty is higher noise. The noise analysis will be discussed in section 3.3.



3.2 High Temperature OTA Design using Inversion Coefficient (g_m/I_d)

The junction leakage current in the bulk CMOS analog integrated circuits increases at high temperatures. The amount of leakage current is comparable to the bias current at elevated temperature. Leakage current compensation techniques have been proposed in [25, 44, 45]. References [25] and [44] used compensation diode to compensate the leakage current. Reference [45] uses large external hold capacitors to reduce the performance degradation and the doughnut shape layout is employed to minimize the diffusion area of the switches. All of these compensation techniques require larger chip area, extra power consumption and more external discrete components. Meanwhile, the extra external discrete component will increase the cost and the PCB real estate.

The SOI fabrication process offers a better process solution by minimizing leakage current at elevated temperature. Nevertheless, the threshold voltage and the bias point shifts along with the transconductance degradation with increasing temperature need to be taken care of by using special design techniques [46~51].

Reference [47,48] proposed g_m/I_d method in designing high temperature SOI OTA. Both of these previous works in high temperature linear regulator [27, 28] lack treatments in addressing the design methodology of the OTA at high temperature. Reference [27] used SOI process technology to implement the high temperature linear voltage regulator. Temperature independent biasing had been mentioned in this work, but it did not address the detail design techniques for the temperature independent biasing circuit and the OTA. Reference [28] also presented a high temperature linear voltage regulator in BiCMOS process technology but the discussion of temperature stable biasing and the OTA design techniques are also missing.

This research presents a high temperature OTA design based on inversion coefficient [52~54], and a temperature stable current reference for biasing OTA. The detail of temperature stable current reference will be discussed in next chapter.

The g_m/I_d parameter in the saturation region can be expressed as,

$$\frac{g_m}{I_d} = \frac{2I_d}{V_{GS} - V_{th}} \cdot \frac{1}{I_d} = \frac{2}{V_{GS} - V_{th}} = \frac{2}{V_{DS,SAT}} \quad (3.2)$$

where $V_{DS,SAT}$ is the drain-source saturation voltage of the transistor, I_d is the DC drain current of the MOS transistor. Figures 3.3~3.5 show the simulated g_m/I_d as a function of normalized drain current and temperature for LVNMOS, LVP MOS, respectively. The g_m/I_d curve offers more meaningful insight into the design of the amplifier. The voltage gain of simple single stage OTA in Figure 3.2 can be given by,

$$\begin{aligned} Av &= g_{m_in} \cdot (R_{o_n} // R_{o_p}) = g_{m_in} \cdot \left(\frac{1}{\lambda_n I_d} // \frac{1}{\lambda_p I_d} \right) \\ &= \frac{g_{m_in}}{I_d} \cdot \left(\frac{1}{\lambda_n + \lambda_p} \right) = \frac{g_{m_in}}{I_d} \cdot \left(\frac{1}{\frac{1}{V_{A,n}} + \frac{1}{V_{A,p}}} \right) \\ &= \frac{g_{m_in}}{I_d} \cdot [V_{A,n} // V_{A,p}] \\ &= \frac{g_{m_in}}{I_d} \cdot [V_{A_Equivalent}] \end{aligned} \quad (3.3)$$

where g_{m_in} Transconductance of input pair

λ_n, λ_p Channel length modulation parameters for NMOS and PMOS, respectively

$V_{A,n}, V_{A,p}$ Early voltage for NMOS and PMOS, respectively

$V_{A_Equivalent}$ Equivalent Early voltage

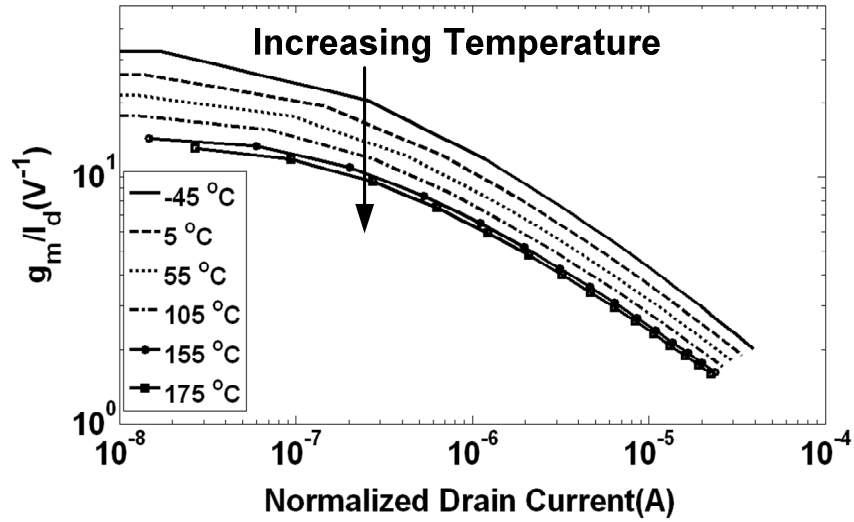


Figure 3.3 Simulation of LV NMOS g_m/I_d parameter over temperature, $V_{DS}=2.5V, W/L=48\mu m/2\mu m$

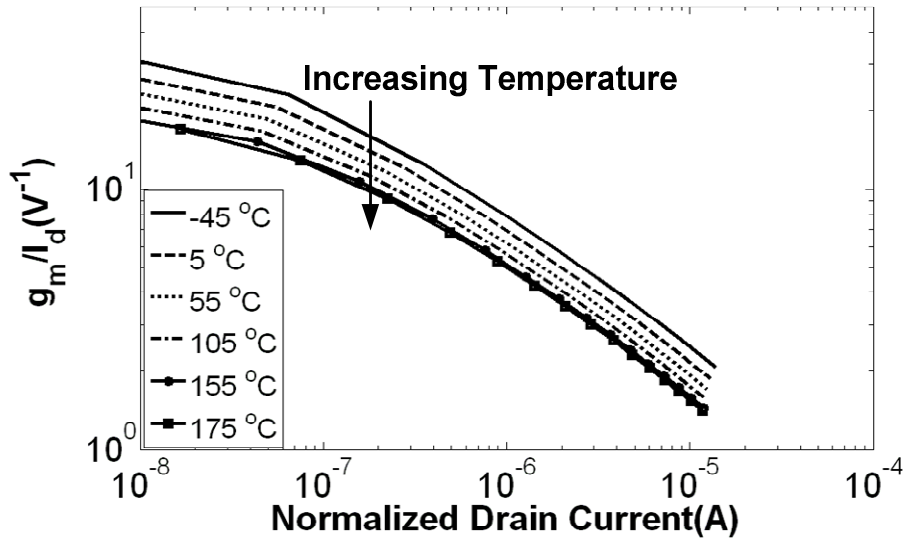


Figure 3.4 Simulation of LV PMOS g_m/I_d parameter over temperature $V_{SD}=2.5V, W/L=96\mu m/2\mu m$

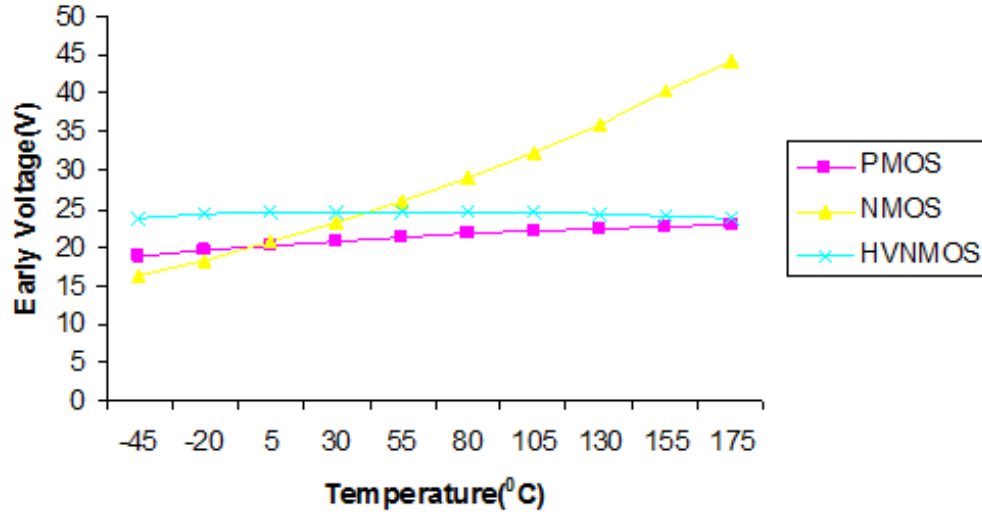


Figure 3.5 Equivalent early voltage of LV NMOS/PMOS, HVNMOS, $I_d=15\mu A$

Figures 3.3~3.5 show the g_m/I_d parameter of LVNMOS, LVPMOS, HV NMOS and the equivalent early voltage across temperature. From these figures, we can observe that the g_m/I_d parameter decreases when biasing current increases. This indicates that the devices are operating in saturation region. The g_m/I_d parameter drops down to only 1~2 at 10's μA of the normalized drain current.

When the bias current is given, by substituting the g_m/I_d value and the equivalent early voltage parameters observed from Figures 3.3~3.5, the voltage gain can be easily obtained and the power consumption can also be estimated. Meanwhile, the low power consumption in analog integrated circuit can be achieved by biasing the transistors in weak inversion region, but the transition frequency; f_T will decrease due to the low overdrive voltage. In addition, the conventional voltage gain representation $g_m r_o$ does not include temperature dependency effect of g_m and r_o . With the g_m/I_d curve, the temperature dependency effect is included (See Figures 3.3~3.5) and the designer can have better grasp of the performance of the amplifier at elevated

Table 3.1 Voltage gain of Simple Single Stage OTA

Temperature	g_m/I_d method	AC Simulation
25⁰C	37.73dB	39dB
50⁰C	37.5dB	38.9dB
100⁰C	36.9dB	38.69dB
150⁰C	36.4dB	38.45dB
200⁰C	36dB	38.2dB

temperatures. The g_m/I_d curve can be applied to bulk CMOS process and different amplifier topologies.

Table 3.1 tabulates the hand calculation of the voltage gain and the voltage gain values obtained from CADENCE simulation. AC simulation is performed by using ideal constant current source.

By applying g_m/I_d method to folded-cascode OTA, see Figure 3.1, equation (3.1) can be rewritten as,

$$\begin{aligned}
 A_v &= g_{m_in} \cdot (R_{o_ncascode} // R_{o_pcascode}) \\
 R_{o_ncascode} &\cong g_{m_M7} (r_{o_M5} // r_{o_M3}) r_{o_M7} \\
 &\cong \left(\frac{g_{m_M7}}{I_{d_M7}} \right) \frac{1}{I_{d_M7}} \left(\frac{V_{A_M7} V_{A_M5} V_{A_M3}}{2V_{A_M3} + V_{A_M5}} \right) \\
 R_{o_pcascode} &\cong g_{m_M9} r_{o_M9} r_{o_M11} \\
 &\cong \left(\frac{g_{m_M9}}{I_{d_M9}} \right) \left(\frac{V_{A_M9} V_{A_M11}}{I_{d_M9}} \right)
 \end{aligned} \tag{3.4}$$

$$R_{o_ncascode} // R_{o_pcascode} \cong \frac{1}{I_{d_M3}} \left(\frac{\left(\frac{g_{m_M7}}{I_{d_M7}} \right) \left(\frac{V_{A_M7} V_{A_M5} V_{A_M3}}{2V_{A_M3} + V_{A_M5}} \right) \left(\frac{g_{m_M9}}{I_{d_M9}} \right) (V_{A_M9} V_{A_M11})}{\left(\frac{g_{m_M7}}{I_{d_M7}} \right) \left(\frac{V_{A_M7} V_{A_M5} V_{A_M3}}{2V_{A_M3} + V_{A_M5}} \right) + \left(\frac{g_{m_M9}}{I_{d_M9}} \right) (V_{A_M9} V_{A_M11})} \right) \quad (3.5)$$

$$A_v \cong \left(\frac{g_{m_in}}{I_{d_M3}} \right) \cdot \left(\frac{\left(\frac{g_{m_M7}}{I_{d_M7}} \right) \left(\frac{V_{A_M7} V_{A_M5} V_{A_M3}}{2V_{A_M3} + V_{A_M5}} \right) \left(\frac{g_{m_M9}}{I_{d_M9}} \right) (V_{A_M9} V_{A_M11})}{\left(\frac{g_{m_M7}}{I_{d_M7}} \right) \left(\frac{V_{A_M7} V_{A_M5} V_{A_M3}}{2V_{A_M3} + V_{A_M5}} \right) + \left(\frac{g_{m_M9}}{I_{d_M9}} \right) (V_{A_M9} V_{A_M11})} \right) \quad (3.6)$$

where $V_{A_M\#}$ represents the Early voltage of the transistor $M_{\#}$

$$I_{d_M3} = I_{d_M9} = I_{d_M7} = \frac{I_{d_M5}}{2}$$

Equations (3.4) ~ (3.6) represents the voltage gain of folded-cascode OTA using g_m/I_d .

The Early voltage of the transistor is defined as $V_A = \frac{I_d}{g_{ds}}$, where g_{ds} is the output conductance of

a transistor. In the standard bulk CMOS process technology, g_{ds} of a MOSFET biased at saturation region is known to increase drastically at elevated temperatures (above 200°C). This is due to the leakage conductance, g_{rbd} , being increased to a comparable value of total output conductance, g_o [25]. Fortunately, the SOI process technology minimizes the leakage current at elevated temperatures.

Theoretically, the Early voltage of the SOI process MOSFET should remain constant over temperature [46] and can be obtained from OP (Operating Point) file of the DC simulation. Table 3.2 tabulates the Early voltage of the transistor M_3 , M_5 , M_7 , M_9 and M_{11} . (See Figure3.1) M_{11} is biased at moderate inversion region and its Early voltage is only 30% of M_9 (saturation

region). Table 3.3 lists the voltage estimated folded cascode voltage gain over temperature of 25°C, 50°C, 100°C, 150°C and 200°C by using g_m/I_d number extracted from simulation.

Figure 3.6 illustrates the AC simulation of the folded cascode OTA at 200°C, the phase margin is approximately 80° with 5pF load capacitance. Figure 3.7 compares different topologies of reported high temperature SOI OTAs. It is evident from this figure that the folded cascode topology OTA offers considerably higher gain over temperature variation.

Table 3.2 Early voltage of transistors used in folded cascode OTA

Temperature	M3	M5	M7	M9	M11
25°C	V _A =44.13V	V _A =22.65V	V _A =24.63V	V _A =20.63V	V _A =6.915V
50°C	V _A =44.96V	V _A =25.33V	V _A =24.7V	V _A =21.16V	V _A =7.081V
100°C	V _A =45.98V	V _A =31.54V	V _A =24.57V	V _A =22.02V	V _A =7.385V
150°C	V _A =46.25V	V _A =39.41V	V _A =24.15V	V _A =22.68V	V _A =7.645V
200°C	V _A =45.84V	V _A =50.02V	V _A =23.47V	V _A =23.19V	V _A =7.78V

Table 3.3 Voltage gain of the folded-cascode OTA

Temperature	g_m/I_d method
25°C	79.4480 dB
50°C	79.3280 dB
100°C	77.4156 dB
150°C	76.1504 dB
200°C	75.4079 dB

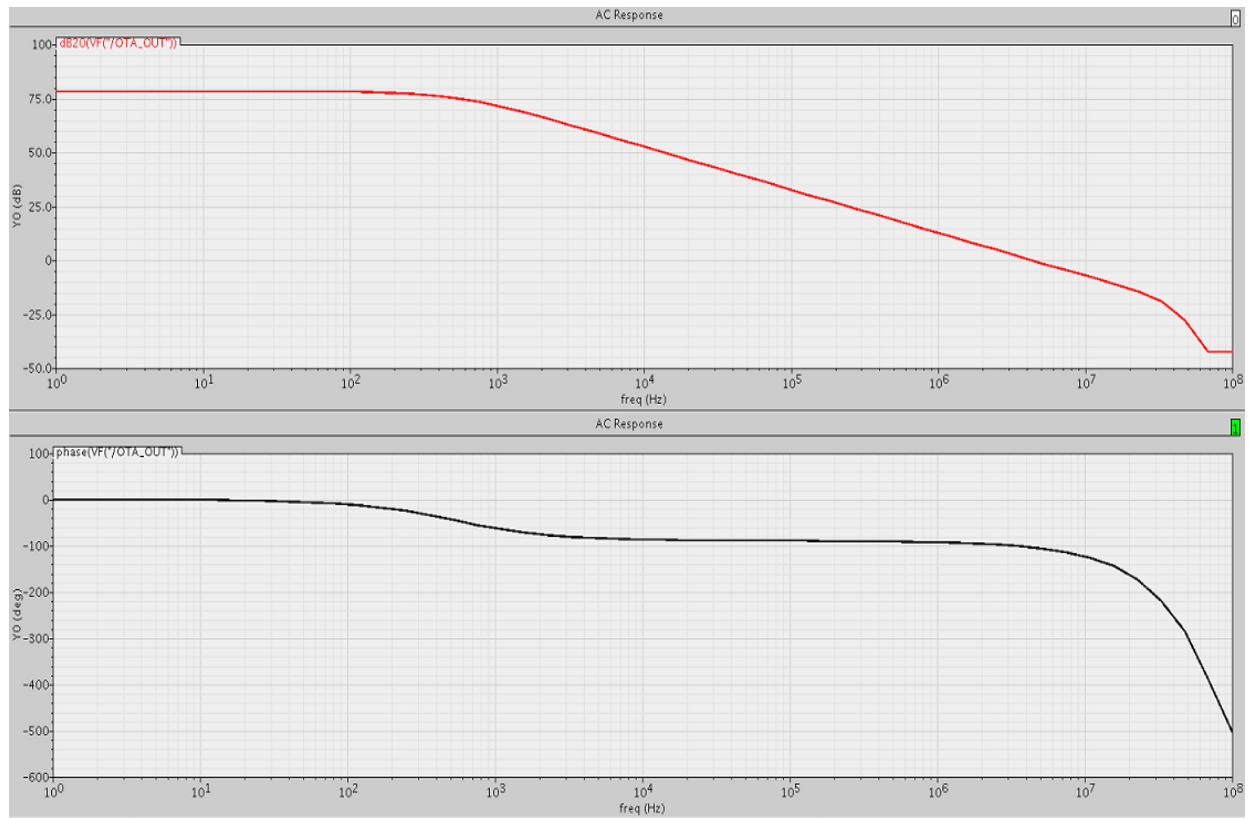


Figure 3.6 AC Simulation of the folded cascode OTA at temperature of 200°C. The top picture represents the voltage gain, bottom picture represents the phase.

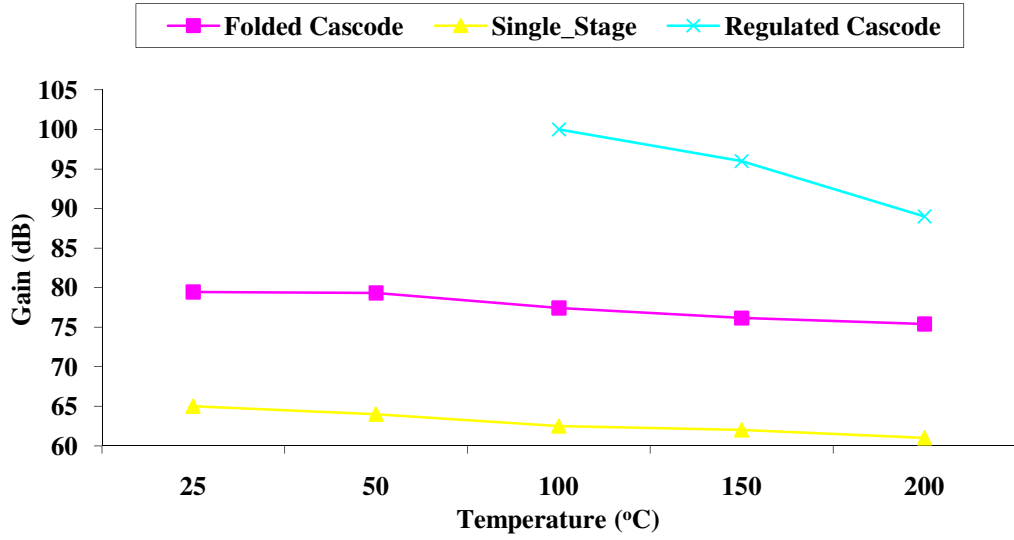


Figure 3.7 Comparison of high temperature SOI OTAs

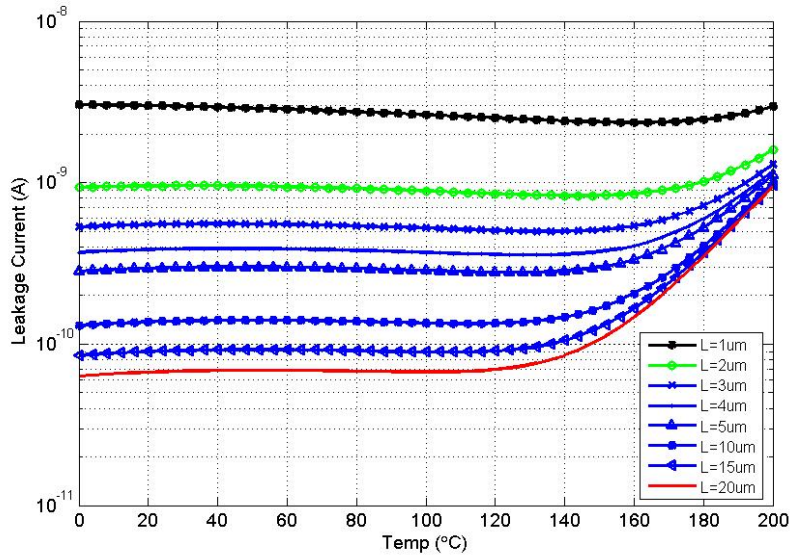


Figure 3.8 Simulation of LV NMOS leakage current with different Length, $V_{ds}=2.5V$, $V_{gs}=1.2V$

Figure 3.8 shows the simulation of the leakage current with respect to temperature and transistor channel lengths. From Figure3.8, it is obvious that while the LV NMOS operates at

temperature beyond 180°C the leakage current is independent of the device length if the device length is greater than 3μm.

From this figure it is clear that the large device length may help reduce the leakage current at temperature below 140°C. Therefore, the optimal device length is between 2μm~5μm. Table 3.4 lists the aspect ratios of folded cascode OTA scheme.

The device length of input pair of the OTA is chosen to be 5μm. According to the result of Figure3.8, the large width and the length of the input pair of OTA can minimize the threshold voltage mismatch due to the process variation. In addition, the device length for the cascode current mirror is chosen to be 2μm.

Table 3.4 Transistors size of the folded-cascode OTA

Transistor	W/L (μm)	Type
M1	100/2	LVP MOS
M2, M3	200/5	LVP MOS
M4, M5	48/2	LVNMOS
M6, M7	20/1.6	HVNMOS (25V)
M8~M11	96/2	LVP MOS_NB*

* NB represents neighboring box.

3.2.1. Inversion Coefficient

The inversion coefficient can offer the circuit designer a meaningful insight into the selection of MOSFETs operating in weak, moderate, and strong inversion regimes. Optimization of the circuit performance is easily achieved by utilizing the inversion coefficient [52, 53, 54]. In [54], moderate inversion optimizes the tradeoff between gain, speed and power consumption. Unfortunately, traditional BSIM3V3 models do not characterize moderate inversion operation

well. BSIM3V3 can show a 40% error in moderate inversion operation. However, the EKV 2.6 model offers more accurate modeling in moderate inversion operation [53].

The BCD-on-SOI process technology used in this work employs EKV models; hence, the inversion coefficient methodology is utilized in designing the error amplifier. The fixed normalized inversion coefficient(IC), can be defined as,

$$IC = \frac{I_D}{2n_0\mu_0C_{ox}'V_T^2\left(\frac{W}{L}\right)} \quad (3.7)$$

where I_D is drain current, n_0 is the sub-threshold slope factor, μ_0 is the mobility, C_{ox}' is the gate oxide capacitance, V_T is the thermal voltage, W and L represent the width and the length of the transistor, respectively.

Figure 3.9 shows the simulation result of the NMOS ($W=48 \mu m$, $L = 2 \mu m$) transconductance efficiency versus inversion coefficient from $-45^\circ C$ to $175^\circ C$. Figure 3.10 shows the simulation result of the PMOS ($W = 96 \mu m$, $L = 2 \mu m$) transconductance efficiency versus inversion coefficient from $-45^\circ C$ to $175^\circ C$. In Figures 3.9 and 3.10, the inversion coefficient represents all regions of operation of a MOSFET: the weak inversion (WI) region is represented by inversion coefficient less than 0.1; the moderate inversion (MI) lies between inversion coefficient ranging 1 to 10 and the strong inversion (SI) indicates inversion coefficient greater than 10.

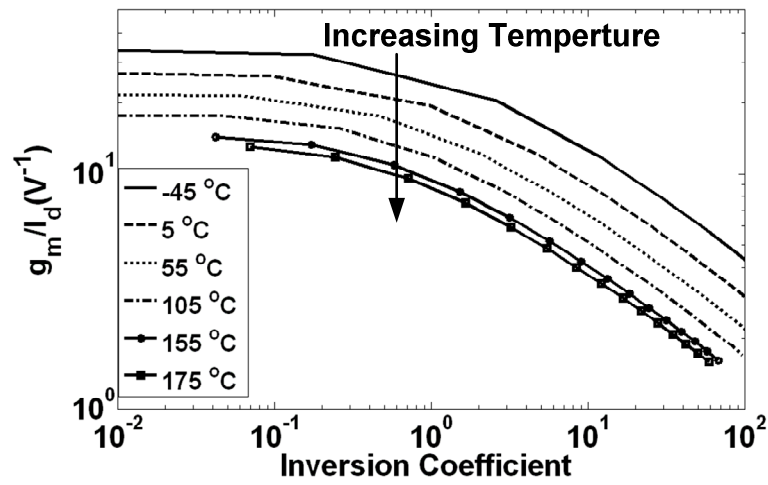


Figure 3.9 Simulation of NMOS transconductance efficiency versus inversion coefficient

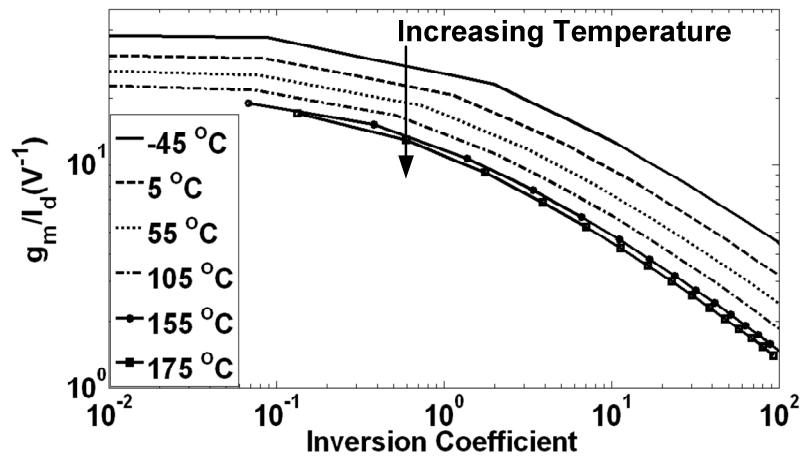


Figure 3.10 Simulation of PMOS transconductance efficiency versus inversion coefficient

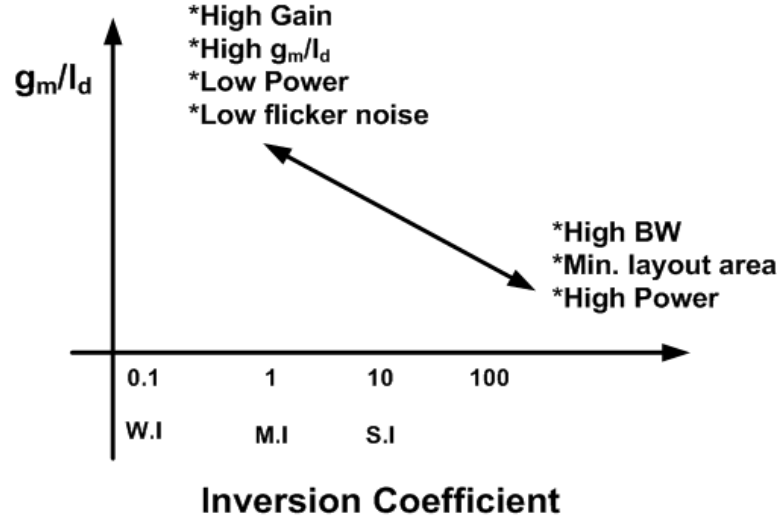


Figure 3.11 Design tradeoff using g_m/I_d vs. Inversion Coefficient [54]

Figure 3.11 shows when the MOSFET operates in weak inversion region circuit can have high transconductance efficiency, high gain, low power and low flicker noise, but with a tradeoff of large layout area and large parasitic capacitance.

When the MOSFET operates in the strong inversion region, the circuit can have high speed, high bandwidth, small layout area, small parasitic capacitance, but with a tradeoff of high power consumption and low voltage gain. Evidently, if the MOSFET is operated in the moderate inversion region, the circuit can have moderate speed, bandwidth, the layout area parasitic capacitance power consumption and voltage gain. In conclusion, the MOSFET operation region can be summarized as (1) WI, it represents V_{gs} is below V_{th} , and the channel is weakly inverted; (2) MI represents $V_{gs}-V_{th}$ is less than 225mv; lastly, (3) SI represents V_{DS_sat} greater than 225 mV.

This work aims to design an OTA operating at moderate inversion region during high temperature environment (i.e. 175°C). Table 3.5 lists the transistor size, IC and g_m/I_d at 175°C.

Figure 3.12 shows simulation result of g_m/I_d of NMOS/PMOS as function of temperature. In this figure, the transconductance efficiency (g_m/I_d) decreases with the increasing temperature. Figure 3.13 presents the simulation results of the DC voltage gain and the unity gain frequency of the OTA. From Figures 3.12 and 3.13, the gain (solid line with squared shape) and the unity gain (solid line with diamond shape) of both the OTA decrease with increasing temperature. This is due to the mobility degradation at elevated temperatures [4, 25].

Table 3.5 Transistors size, IC and g_m/I_d of folded-cascode OTA at 175°C

MOS	Type	W/L ($\mu\text{m}/\mu\text{m}$)	IC	g_m/I_d
M₁	PMOS	100/2	~4.75	~7
M₂, M₃	PMOS	200/5	~3	~6.5
M₄, M₅	NMOS	48/2	~3.25	~5
M₆, M₇	HVNDMOS	20/1.3	~5.5	~10
M₈~M₁₁	NMOS	96/2	~2.5	~7

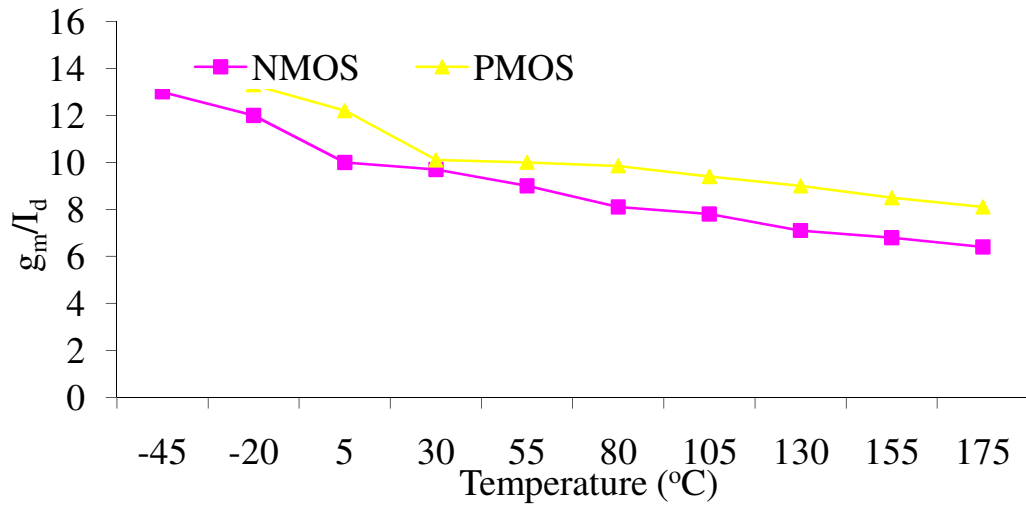


Figure 3.12 The g_m/I_d of NMOS/PMOS versus temperature

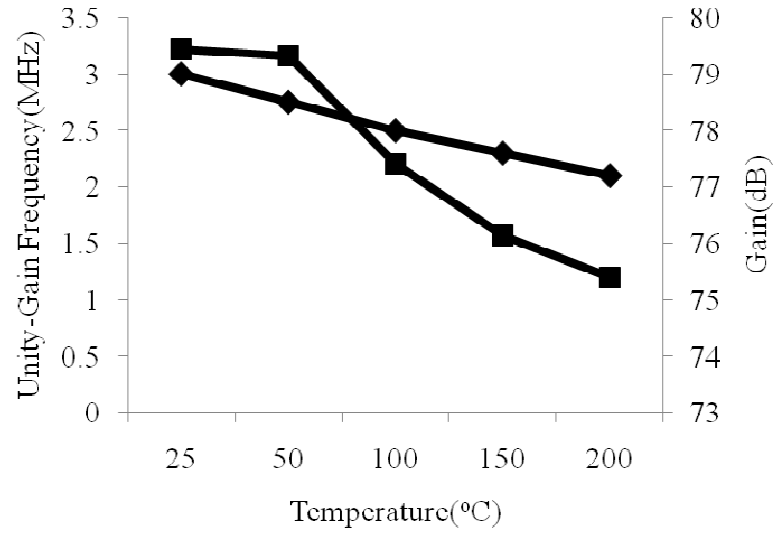


Figure 3.13 Simulated DC gain and unity-gain frequency of OTA as function of temperature (\blacksquare Unity-Gain Frequency; \blacklozenge Gain)

3.3 Mismatch and Offset Voltage of OTA

Mismatch limits the performance of the OTA. The mismatches arise from random process variations which is a time-independent random process. References, [56,57] offer mathematical and experimental analyses of the mismatch properties. The effect of mismatch in OTA design and the design tradeoff and methodologies to reduce the mismatches are also discussed in this section.

Due to its random nature, mismatch can be treated as the result of several random processes which occur during device fabrication. The variance of parameter ΔP between two devices with the same size (aspect ratio) can be expressed as [56],

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 \cdot D^2 \quad (3.7)$$

where A_P is a dimension parameter, S_P is the variation of parameter P , and D is the spacing between the two transistors. Reference [56] suggests that the spacing parameter S_P between the transistors can be neglected. Once the process-dependent proportionality constants A_P and S_P have been identified, this equation can be used to predict mismatch of a circuit.

MOSFETs suffer mismatches from threshold voltage and current factor β , where $\beta = \mu_{eff} \cdot C_{ox} \frac{W}{L}$. The threshold voltage mismatch comes from oxide thickness, doping concentration of substrate, charge in depletion region, etc. The variance of threshold voltage and the current factor can be expressed as [56],

$$\sigma^2(V_{TH}) = \frac{A_{VTH}^2}{WL} + S_{VTH}^2 \cdot D^2 \quad (3.8)$$

$$\frac{\sigma^2(\beta)}{\beta^2} \cong \frac{A_\beta^2}{WL} + S_\beta^2 \cdot D^2 \quad (3.9)$$

where $A_{V_{TH}}$ and A_β are process-related constants.

From the equation above, the mismatch can be reduced by increasing the size of the transistors, this is because the random variations will experience greater averaging and the magnitude of mismatch will be reduced [56].

Current mirror matching is very critical to analog integrated circuits. Current mirrors act as active load in folded-cascode OTA. The mismatches of the current mirror are caused by $\Delta \beta$ and ΔV_{TH} . The current mirror mismatch can be expressed as [56],

$$\frac{\sigma^2(I_d)}{I_d^2} = \frac{4\sigma^2(V_{TH})}{(V_{ov})^2} + \frac{\sigma^2(\beta)}{\beta^2} \quad (3.10)$$

When the current mirror is biased in the saturation region, the standard deviation of the current mirror mismatch can be written as,

$$\frac{\Delta I_d}{I_d} = \frac{2}{V_{GS} - V_{TH}} \Delta V_{TH} + \frac{\Delta \beta}{\beta} \quad (3.11)$$

The folded-cascode OTA as shown in Figure 3.1 consists of a PMOS input pair and the cascode current mirror. The input offset voltage of the PMOS input pair can be derived by applying KVL in the input loop, and it is expressed as [59],

$$V_{os,in} = \Delta V_{TH} + \frac{V_{GS,in} - V_{TH}}{2} \left(\frac{\Delta I_{d,in}}{I_{d,in}} + \frac{\Delta \beta_{in}}{\beta_{in}} \right) \quad (3.12)$$

where the subscript *in* represents the PMOS input pair. The total random offset voltage of the folded-cascode is the combination of the input pair offset voltage and the offset voltage caused by the current mirror mismatch, and can be written as [60],

$$\begin{aligned}
V_{os,tot} &= V_{os,in} + \frac{\Delta I_{d,cas}}{g_{m,in}} = \\
&\Delta V_{TH,in} + \frac{V_{GS,in} - V_{TH}}{2} \left(\frac{\Delta \beta_{in}}{\beta_{in}} \right) + \frac{V_{GS,in} - V_{TH}}{V_{GS,cas} - V_{TH}} \Delta V_{TH,cas} \\
&+ \frac{V_{GS,in} - V_{TH}}{2} \left(\frac{\Delta \beta_{cas}}{\beta_{cas}} \right)
\end{aligned} \tag{3.13}$$

where the subscript *cas* represents the cascode current mirror. Since all the parameter are treated as independent random variables with Gaussian distribution, by substituting equation (3.8) and (3.9) into (3.13), the variance of total offset voltage of folded cascode OTA can be approximated as,

$$\sigma^2(V_{os,tot}) = \left(\frac{A_{VTH}^2}{WL} \right)_{in} + \left(\frac{V_{ov,in}}{V_{ov,cas}} \right)^2 \left(\frac{A_{VTH}^2}{WL} \right)_{cas} + \left(\frac{V_{ov,in}}{2} \right)^2 \left[\left(\frac{A_{\beta}^2}{WL} \right)_{in} + \left(\frac{A_{\beta}^2}{WL} \right)_{cas} \right] \tag{3.14}$$

By applying g_m/I_d method into equation (3.14), we can get,

$$\sigma^2(V_{os,tot}) = \left(\frac{A_{VTH}^2}{WL} \right)_{in} + \left(\frac{\left(\frac{g_m}{I_d} \right)_{cas}}{\left(\frac{g_m}{I_d} \right)_{in}} \right)^2 \left(\frac{A_{VTH}^2}{WL} \right)_{cas} + \left(\frac{g_m}{I_d} \right)_{in}^{-2} \left[\left(\frac{A_{\beta}^2}{WL} \right)_{in} + \left(\frac{A_{\beta}^2}{WL} \right)_{cas} \right] \tag{3.15}$$

From equation (3.15), the increasing aspect ratio of the PMOS input pair will reduce the offset voltage caused by the threshold voltage mismatch. Reducing the g_m/I_d ratio of the cascode current mirror, biases the cascode current mirror in strong inversion region and biases the input pair near the weak or the moderate inversion regions and can also reduce the offset voltage.

After rewriting equation (3.14) by using g_m/I_d representation, it offers more detail of temperature effect on the offset voltage. Equation (3.15) indicates the optimum operation region of the input pair and the cascode current mirror for reducing the offset voltage. Nevertheless, the

threshold voltage mismatch remains a dominant source of the offset voltage. Table 3.6 lists the mean and the standard deviation of the offset voltage of the folded cascode OTAs from 100 iterations of Monte-Carlo simulation, Figure 3.14 shows the offset voltage for 25°C, 50°C, 100°C, 150°C and 200°C. Figure 3.15 shows the average offset voltage for 25°C, 50°C, 100°C, 150°C and 200°C.

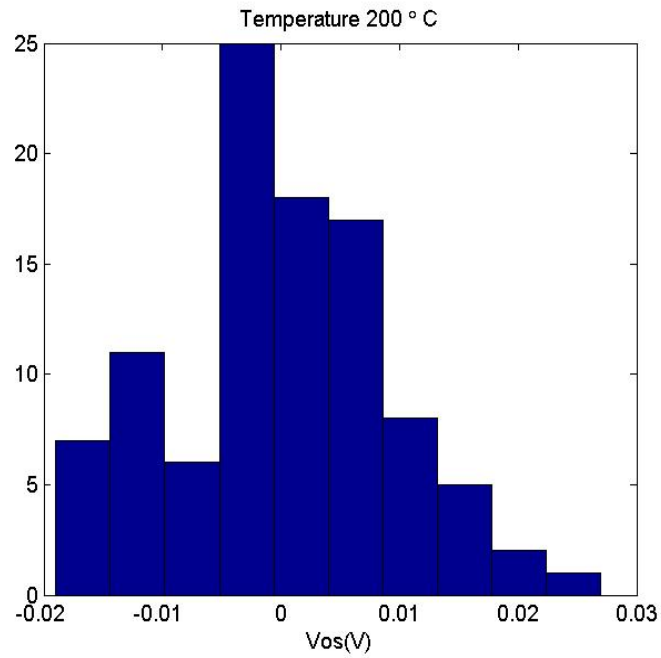


Figure 3.14 Monte-Carlo simulation of the folded cascode OTA offset voltage with $T=200^{\circ}\text{C}$ and 100 iterations

Table 3.6 Mean and standard deviation of offset voltage of the folded-Cascode OTA

Temperature	Mean (V)	Standard Deviation (V)
25°C	0.0082	0.0062
50°C	0.0081	0.0061
100°C	0.0078	0.0059
150°C	0.0076	0.0056
200°C	0.0073	0.0054

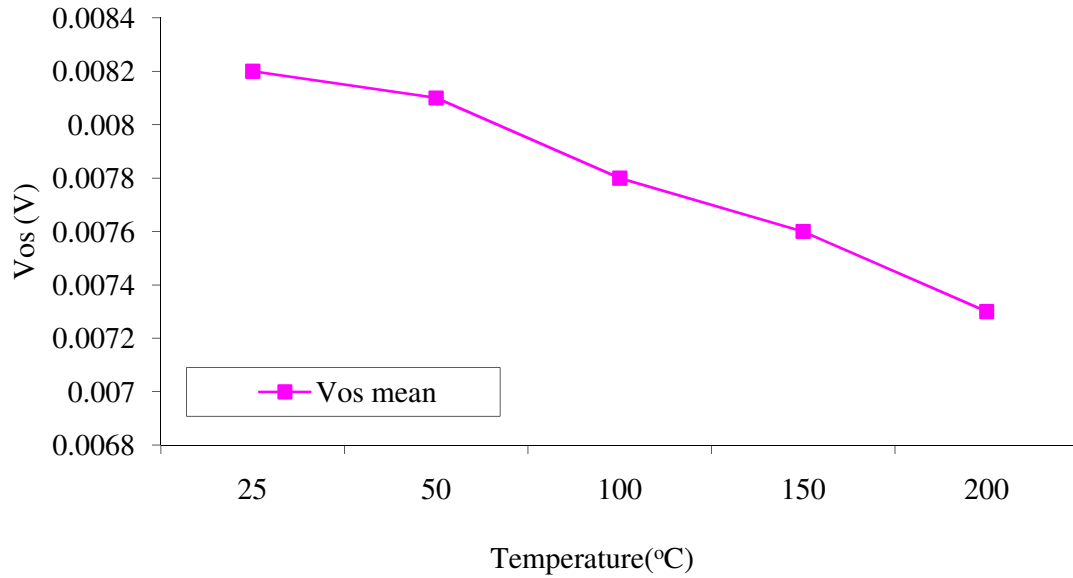


Figure 3.15 Mean of the folded cascode OTA offset voltage with $T = 25^{\circ}\text{C} \sim 200^{\circ}\text{C}$

3.4 Noise analysis of OTA

Noise degrades the performance of the amplifiers. In integrated circuits there exist two different types of noise: the device electronic noise and the environmental noise [58]. The device electronic noise in a MOSFET includes thermal noise and flicker noise. The MOSFETs exhibit thermal noise because of the presence of the resistive channel. The channel noise can be modeled by a noise current source in parallel with the drain and the source terminal of the MOSFET as shown in Figure 3.14. The noise contributions of the folded cascode OTA come from two sources: the thermal noise of the MOSFET and the flicker noise, which is closely related to the fabrication technology.

The noise analysis of a folded cascode amplifier is shown in Figure 3.17. The folded cascode OTA contributes larger noise than the conventional active load differential pair because the cascode current mirror (M_8 , M_9 , M_{10} and M_{11}) is employed to increase the voltage gain. Transistor M_6 , M_7 , M_8 and M_9 are the cascode devices. The noise contributed by the bias current source can be ignored [58].

In Figure 3.16, K represents Boltzmann constant, 1.38×10^{-23} J/K, the coefficient $\frac{2}{3}$ indicates a long-channel MOSFET.

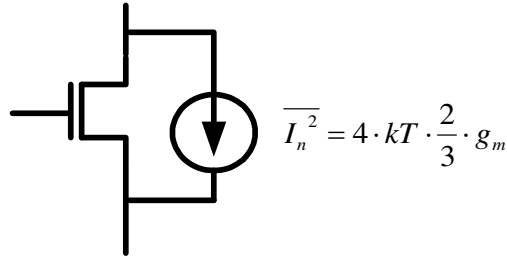


Figure 3.16 Thermal noise current of NMOSFET

The input-referred noise voltage of the folded cascode OTA can be expressed as,

$$\overline{V_{n,in}^2} = 2 \cdot \left[\overline{V_{n2}^2} + \left(\frac{g_{m4}}{g_{m2}} \right)^2 \cdot \overline{V_{n4}^2} + \left(\frac{g_{m10}}{g_{m2}} \right)^2 \cdot \overline{V_{n10}^2} \right] \quad (3.16)$$

Where $\overline{V_{n2}^2} = 4KT \left(\frac{2}{3} \right) \frac{1}{g_{m2}}$

In equation (3.16), the second and the third terms represent the noise contributions from the OTA NMOS cascode current mirror and the PMOS cascode current mirror, respectively. The transistors of the input pair and the cascode current mirrors are all matched in size and hence the noise contribution is doubled. For minimizing the overall noise, g_{m2} needs to be maximized, the

size of input pair needs to be larger than the current mirror load, the overdrive voltage of the input pair, and g_{m4} and g_{m10} should be as small as possible.

Table 3.7 summarizes the design considerations for minimizing the noise and the offset voltage.

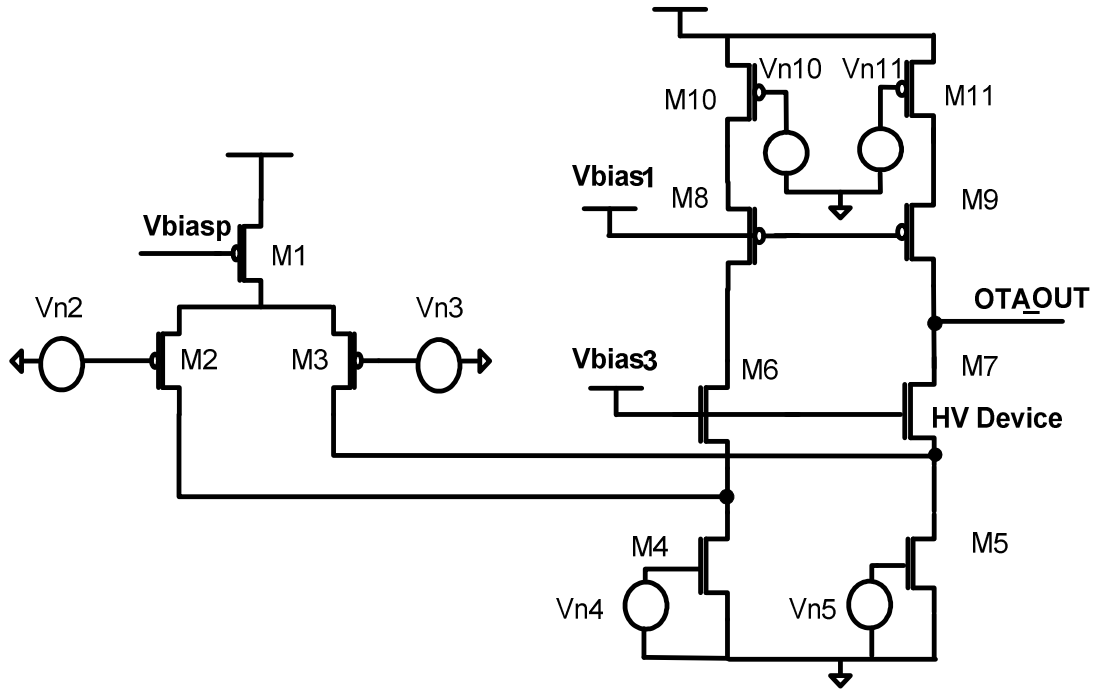


Figure 3.17 Noise analysis of the folded cascode OTA offset voltage

Table 3.7 Optimization of offset and noise of the folded cascode OTA

Optimization	Input Pair	Cascode Current Mirror
Noise	Large WL, Small V_{ovin}	Operates in saturation region; Small g_m
Offset	Large WL, Large g_{m2} Small V_{ovin}	Operates in saturation region; Small g_m

Flicker noise is not a temperature dependent noise and arises whenever the DC current flows in a discontinuous material. The flicker noise varies with different process technologies and the magnitude of input-referred flicker noise depends on the process technology. The flicker noise exhibits the highest noise level at low frequency, and it decreases with increasing frequency. The flicker noise is given by [58~62],

$$\overline{V}_{n, flicker}^2 = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \quad (3.17)$$

where K in (3.17) is a process dependent constant. The different process technology offers different K values. Taking flicker noise voltage (3.17) into consideration, equation (3.16) can be rewritten as.

$$\overline{V}_{n,in}^2 = 2 \cdot \left[\overline{V}_{n2}^2 + \left(\frac{g_{m4}}{g_{m2}} \right)^2 \cdot \overline{V}_{n4}^2 + \left(\frac{g_{m10}}{g_{m2}} \right)^2 \cdot \overline{V}_{n10}^2 + \frac{K_p}{C_{ox}(WL)_2} \cdot \frac{1}{f} + \left(\frac{g_{m4}}{g_{m2}} \right)^2 \cdot \frac{K_n}{C_{ox}(WL)_4} \cdot \frac{1}{f} \right. \\ \left. + \left(\frac{g_{m10}}{g_{m2}} \right)^2 \cdot \frac{K_p}{C_{ox}(WL)_{10}} \cdot \frac{1}{f} \right] \quad (3.18)$$

K_p , K_n represents the process dependent constant for the PMOS and the NMOS, respectively.

In conclusion, the folded cascade OTA with PMOS input pair is chosen as the error amplifier of the proposed high temperature linear voltage regulator. The flicker noise and random offset voltage of the input pair can be reduced by increasing the aspect ratio of the input transistor. The amplifier is design to provide a voltage gain of about 73 dB at the elevated temperature, and is utilized to drive the current efficiency voltage buffer. The detailed measurement and simulation results (i.e. Phase Margin, Slew Rate, Voltage Gain, and Unity-Gain Bandwidth) are provided in the Appendix.

CHAPTER 4

Temperature Stable Current Reference

A precision and wide temperature stable current reference is an important building block of many analog and mixed-signal circuits such as PLL (Charge Pump, VCO), filters, operational transconductance amplifiers (OTA) and data converters. The high temperature linear voltage regulator requires a high performance error amplifier (OTA) when operating at elevated temperatures. Therefore, biasing OTA with a constant current will stabilize its gain and maintain the power consumption relatively constant over temperature.

Reference [24] indicates that a stable current/voltage source is required in high temperature circuits. Thus, for achieving stable biasing current with respect to temperature and supply voltage variation, theoretically, both the external and the internal biasing can be utilized to bias the analog circuits. Reference [72] claims the excessive variation of the bias current with temperature and process tends to sacrifice the speed at the low extreme of the bias current, and the power dissipation and the output voltage swing at the high end. Furthermore, the variation of the bias currents with supply voltage results in poor power supply rejection (PSR).

This chapter reviews different current reference/generator topologies. An internal/on-chip temperature stable current reference is implemented for the purpose of stabilizing gain, current consumption and output pole of the OTA.

4.1 Zero Temperature-Coefficient Bias Point

In high temperature circuit design, there are three design techniques that can be applied in the design process. The 1st is ZTC (Zero Temperature-Coefficient), the 2nd is inversion

coefficient (g_m/I_d), and the 3rd is stable current and voltage reference [24]. A ZTC (zero temperature-coefficient) biasing technique was proposed in [24, 25]. A ZTC bias point exists in a MOSFET if the bias voltage is properly selected.

When the MOSFET operates in the saturation region, the drain current is given by the square law equation,

$$I_d = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (4.1)$$

Taking the derivative and evaluating the temperature coefficient of the square law equation we get,

$$\frac{1}{I_d} \cdot \frac{\partial I_d}{\partial T} = \left[\frac{1}{\mu} \frac{\partial \mu}{\partial T} - 2 \frac{1}{(V_{GS} - V_{TH})} \frac{\partial V_{TH}}{\partial T} \right] = 0 \quad (4.2)$$

$$(V_{GS} - V_{TH}) = 2\mu \frac{\frac{\partial V_{TH}}{\partial T}}{\frac{\partial \mu}{\partial T}} \quad (4.3)$$

$$V_{GS} = V_{TH} + (V_{GS} - V_{TH}) = V_{TH} + 2\mu \frac{\frac{\partial V_{TH}}{\partial T}}{\frac{\partial \mu}{\partial T}} \quad (4.4)$$

where the threshold voltage and the mobility can be expressed as,

$$V_{th}(T) = V_{th}(T_0) + TC_{VT}(T - T_0) \quad (4.5)$$

$$\mu(T) = \mu(T_0) \left(\frac{T}{T_0} \right)^{BEX} \quad (4.6)$$

Substituting equation (4.5) and (4.6) into equation (4.4), we can obtain,

$$V_{GS} = V_{TH}(T_0) + TC_{VT} \cdot T \left(1 + \frac{2}{BEX} \right) - TC_{VT} \cdot T_0 \quad (4.7)$$

In bulk CMOS process, BEX (Mobility exponent) could be equal to -2 or close to -2. BEX is related to the doping concentration [65]. Table 4.1 tabulates the BEX and the TC_{VT} (temperature coefficient of threshold voltage) of the low voltage NMOS/PMOS transistor.

When BEX equals -2, equation (4.7) results in a perfect cancellation. This voltage is called zero temperature coefficient voltage V_{ZTC} . If the gate voltage of the NMOSFET can be held at V_{ZTC} , the drain current drawn from this MOSFET is temperature independent. However, BEX of the low voltage NMOSFET does not equal to -2. It leads the equation (4.7) to be temperature dependent.

Figure 4.1 presents the simulation results of I_d vs. V_{GS} of the low voltage (5V) NMOS transistor when $V_{GS} = 1.475 \text{ V}$. The drain current is relatively insensitive to temperature and it confirms that when BEX is not equal to -2. The drain current variation will increase with increasing temperature. Meanwhile, only a 10mV shift of V_{ZTC} will create approximately 10% variations of the reference current. Generating a precision V_{ZTC} over wide temperature range adds to the circuit complexity and the possibly extra power consumption. Besides, the process variation makes ZTC biasing less attractive. Furthermore, the transistors using the ZTC biasing technique usually operate in the strong inversion region and thus have low transconductance efficiency and low gain.[24]

Table 4.1 Mobility exponent and temperature coefficient of MOSFET

BEX	TC_{VT}
-1.68 (NMOS)	-1.5mV(NMOS)
-1.15 (PMOS)	-1.8mV(PMOS)

Table 4.2 tabulates the normalized process variation of the threshold voltage with temperature at the three different process corners: nominal, SS and FF (nominal, slow slow, fast fast).

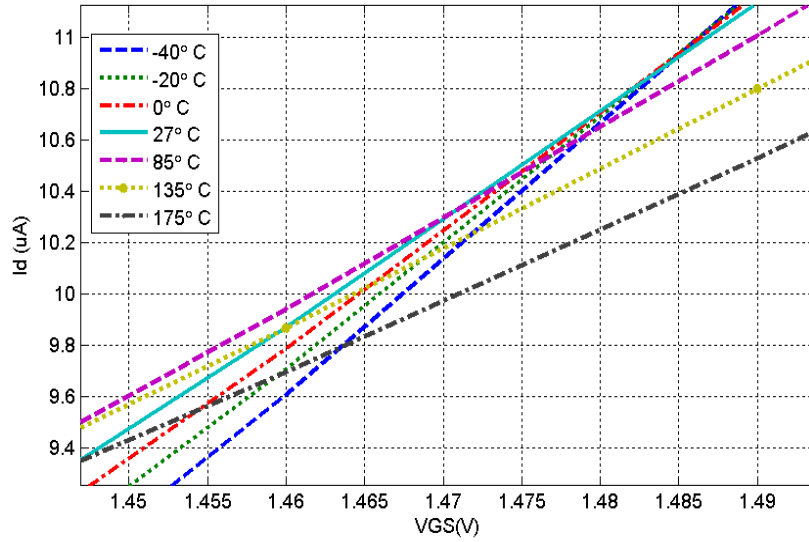


Figure 4.1 Simulation of I_d versus V_{GS} , 5V NMOS transistor ($W=30\mu m, L=20\mu m$)

Table 4.2 Process and temperature variation of the threshold voltage of the NMOS transistor

Process Corner	Threshold Voltage (V)	Normalized K_p'
Nominal(-40°C)	1.0766	1.5722
Nominal(27°C)	0.9658	1.0000
Nominal(175°C)	0.7367	0.4468
SS(-40°C)	1.1650	1.3231
SS(27°C)	1.0617	0.8975
SS(175°C)	0.8295	0.3996
FF(-40°C)	0.9569	1.8009
FF(27°C)	0.8643	1.2216
FF(175°C)	0.6243	0.5113

From the Table 4.2, it is evident that the threshold voltage of the NMOS transistor varies approximately 340 mV from -40°C to 175 °C. This threshold voltage variation is not desirable in high temperature integrated circuit design. This result into the operating point shift and contribute to the system performance degradation.

4.2 Beta-Multiplier Current Reference

A current reference insensitive to supply voltage and temperature is desired for biasing analog circuits, especially for the analog circuits operating at elevated temperature. A high temperature voltage regulator normally accepts higher input DC voltage compared to the commercial room temperature LDO (low dropout voltage regulator). In this research, the input DC voltage of the voltage regulator is varying from 10V to 30V. Because the bias current will set up the DC operating point of the analog circuits, a supply voltage insensitive current reference can be achieved by using the beta-multiplier biasing technique (also named constant g_m). As shown in Figure 4.2, the DC operating point is less sensitive with respect to the supply voltage variation.

Applying KVL in the loop consisting of the transistor M_1 , M_2 and R , the reference current of the beta-multiplier can be defined by,

$$I_{ref} = \frac{2}{R^2 \beta_1} \left(1 - \frac{1}{\sqrt{k}}\right)^2 \quad (4.8)$$

where β_1 is $\frac{\mu C_{ox} W_1}{L_1}$, $\beta_2 = K \cdot \frac{\mu C_{ox} W_1}{L_1}$, when K is equal to 4, and the transconductance g_m is independent of the process (constant g_m) [58~64].

The positive feedback will cause the system to be unstable and some oscillation in analog circuit. However, the beta-multiplier contains positive feedback. Inside the feedback loop of the

beta-multiplier circuit, a test source is included at the gate of the transistor M_2 . Two common source amplifiers in this loop offer no signal inversion, and the resistor R degenerates the gain of the NMOS common source amplifier while the loop gain is less than unity.

The temperature coefficient of the beta-multiplier current reference can be defined as,

$$TCI_{ref} = \frac{1}{I_{ref}} \frac{\partial I_{ref}}{\partial T} \quad (4.9)$$

$$\frac{\partial I_{ref}}{\partial T} = -4 \cdot R^{-3} \cdot \beta_1^{-1} \cdot \left(1 - \frac{1}{\sqrt{k}}\right)^2 \cdot \frac{\partial R}{\partial T} - 2 \cdot R^{-2} \cdot \beta_1^{-2} \cdot \left(1 - \frac{1}{\sqrt{k}}\right)^2 \cdot \frac{\partial \beta_1}{\partial T} \quad (4.10)$$

$$TCI_{ref} = -2 \cdot TCR + \frac{BEX}{T} \quad (4.11)$$

TCR is the temperature coefficient of the resistor used in beta-multiplier current reference; the temperature coefficient can be extracted from DC simulation across temperature. TCR in this case is approximately 1540 ppm/ $^{\circ}\text{C}$. The temperature coefficient of the beta-multiplier current reference can be obtained according to equation (4.11).

Figure 4.3 shows the simulation results of the beta-multiplier current reference. I_{ref} equals 36 μA at room temperature and increases with temperature which will also increase the power consumption at elevated temperatures. The current variation of the beta-multiplier current reference is approximately 36% from -50°C \sim 250°C ; Table 4.3 tabulates temperature coefficients of the beta-multiplier current reference with second order polyfit to the curve of Figure 4.3.

Applying the beta-multiplier current reference to the OTA can maintain the dominant pole frequency (f_{3db}) of the OTA effectively across wide temperature range. Table 4.4 lists the simulation results of the voltage gain, the unity gain frequency, the phase margin and the dominant pole frequency of an OTA which is biased by beta-multiplier current reference.

Table 4.3 Temperature coefficient of beta-multiplier current reference

$TCI_{ref}(Polyfit)$	$TCI_{ref}(\text{equation (4.11)})$
2200 ppm	2500ppm

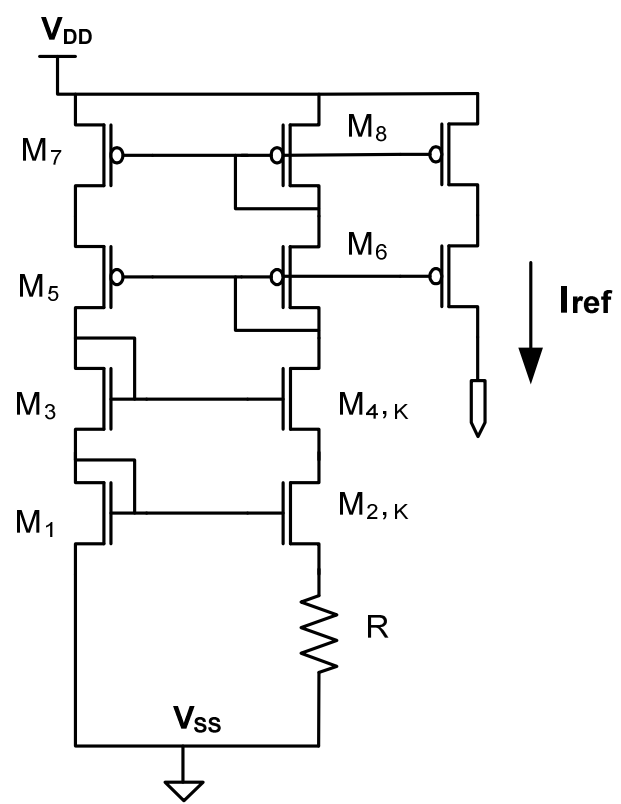


Figure 4.2 Beta-multiplier biasing circuit with $R = 9k\Omega$

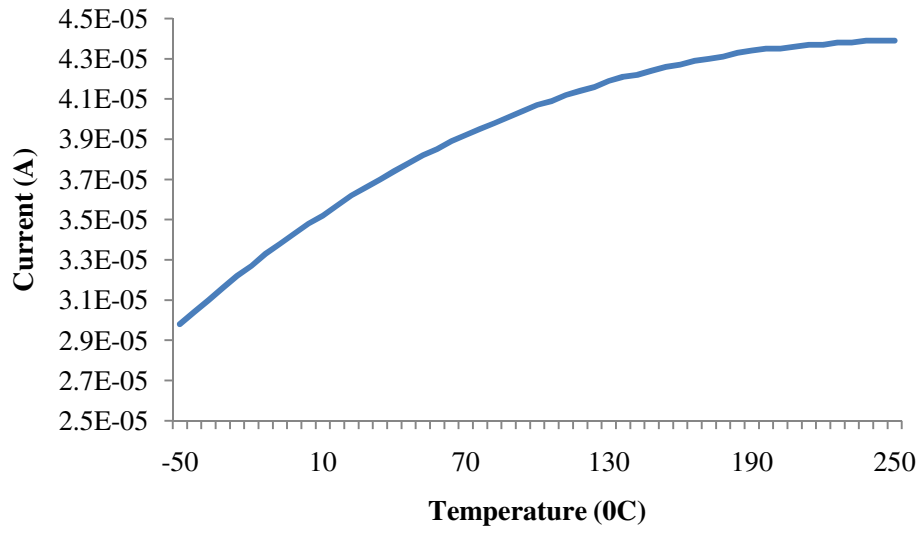


Figure 4.3 Simulation beta-multiplier (constant g_m) current reference

Table 4.4 Beta-multiplier current reference biases OTA with $C_L=5\text{pF}$

Temperature	Gain(dB)	f_{un} (MHz)	P.M ⁰	f_{3dB} (Hz)
25 ⁰ C	75.6	5.1	80 ⁰	870
50 ⁰ C	75.5	5	80 ⁰	840
100 ⁰ C	75.1	4.75	80 ⁰	825
150 ⁰ C	74.7	4.45	80 ⁰	815
200 ⁰ C	74.1	4.18	80 ⁰	818

4.3 PTAT (V_T) Reference

PTAT (proportional to absolute temperature) is another commonly used biasing circuit, (see Figure 4.4) where the reference current generated by this biasing technique linearly increases with temperature. The increased biasing current at elevated temperatures consumes more power and generates more heat on the die. References [24, 25] suggested that a stable current and voltage reference is desired in high temperature integrated circuits. The cascode device is utilized to improve the performance of the PTAT current reference. The reference current can be derived by applying KVL in the loop consisting of the transistor M_1 , M_2 , the diodes and the resistor R as,

$$I_{ref} = \frac{2 \cdot V_T \ln(N)}{R} \quad (4.12)$$

Where N denotes the numbers of diodes, V_T is the thermal voltage ($\frac{K \cdot T}{q}$). From the definition of equation (4.9), the temperature coefficient can be expressed as,

$$TCI_{ref} = -TCR + \frac{1}{T} \quad (4.13)$$

Table 4.5 lists the simulation results using PTAT current reference to bias the OTA. The dominant pole frequency (f_{3db}) of the OTA will increase with increasing temperature. When the dominant pole frequency is increasing with temperature, the system may tend to be unstable due to the dominant pole moving closer to the non-dominant pole which degrades the phase margin. The simulation results show that the dominant pole frequency deviates by 515Hz for temperature variation from 25°C to 200°C.



Temperature	Gain(dB)	f_{un} (MHz)	P.M ⁰	f_{3dB} (Hz)
25 ⁰ C	69.89	5.2	80 ⁰	1660
50 ⁰ C	69.23	5.15	80 ⁰	1760
100 ⁰ C	68.1	5	80 ⁰	1930
150 ⁰ C	67.2	4.75	80 ⁰	2050
200 ⁰ C	66.25	4.5	80 ⁰	2175

4.4 Temperature Stable Current Reference

References [67~88] introduce high performance current and voltage reference in bulk CMOS or SOI process technologies. Reference [85] presented a serial-parallel transistor layout technique to enhance the performance of the SOI based current references. References [8, 24, 25] indicate that a temperature stable current reference is needed for enhancing the performance of OTA at elevated temperatures. If the current reference can maintain a constant current over temperature, then the power dissipation of the OTA will essentially be independent of the temperature.

References [27, 28] report their work with quiescent current at 2.7mA and 2mA respectively. Reference [66] reports a reference circuit which consumes 9 mA of quiescent current. The higher quiescent current would degrade the current efficiency of the voltage regulator and dissipate more heat at high temperature. According to the simulation and the design specification, this work consumes total 0.55mA quiescent current at 175°C, approximately 20% of which is being consumed by the OTA, and the 45% is consumed by the pass transistor.

Several temperature stable current reference design topologies have been proposed and published. Reference [67] proposes an on-chip threshold voltage monitoring circuit to compensate the threshold voltage variation. Both the off-chip operational amplifier and the resistor are used to generate zero temperature coefficient voltage for biasing MOSFET. However, this work is targeted to reduce the usage of the off-chip component because the high temperature off-chip passive components are more expensive than the regular passive component. In addition, the off-chip passive devices add extra PCB real estate overhead and introduce more parasitic capacitances.

Table 4.6 Summary of the temperature stable current reference circuits

Reference	Reference Current(μ A)	Temperature Coefficient(ppm/ $^{\circ}$ C)	Process(μ m)	Supply Voltage(V)	Temperature Range($^{\circ}$ C)	Comment
Ueno[67]	17	46	0.35 CMOS	1.1~2.2	-10~70	Off-chip resistor and operational amplifier
Nissinen [68]	17	85	0.18 CMOS	1.1~2.2	-10~70	Simulation Only
Dehghani[69]	10	83	0.25 CMOS	1.4~3	-20~100	Simulation Only
Lee[70]	0.285	226	2 CMOS	5	0~75	Subthreshold region, square root circuit
Sansen[71]	0.774	375	3 CMOS	3.5	0~80	Weak inversion
Fiori[73]	13.65	28	0.35 BiCMOS	2.5	-30~100	2 nd order temperature compensated
De Vita[74]	0.00914	44	0.35 CMOS	1.5	0~80	Low voltage and low power
Terry[77]	0.39	580	0.35 SOI	3.3	0~100	PTAT current
Bendali[79]	144.3	185	0.18 CMOS	1	0~100	Temperature and Process Compensation
Badillo[80]	5	368	0.25 CMOS	1.5	-40~150	Negative T.C resistor
Radecker[81]	19.5	67	0.2 CMOS	3.3~10	-40~200	PTAT+ Negative TC Current
This Work	13 27	75.3 (Simulation) 227.3(Simulation)	0.8 SOI	10~45V	-50~175	PTAT +CTAT, High Temperature

Table 4.6 summarizes the published works of temperature stable current reference, most of works target temperature below 100°C and use bulk -CMOS processes.

However, CMOS process based temperature stable current reference is not suitable for elevated temperature applications due to the increase of leakage current at high temperature which affect the bias point, cause latchup and degrade overall performance of the temperature coefficient.

This research utilizes a SOI process technology to reduce the leakage current and extend the operating temperature beyond 175 °C. Nevertheless, the circuit design techniques need to be chosen for minimizing the temperature coefficient over wide temperature range and eliminating the usage of the off-chip passive device and reducing the complexity of the design approach.

This work proposes a temperature stable current reference circuit using PTAT current and CTAT (complementary to absolute temperature) circuits. The CTAT current references can be obtained using PN diodes. The voltage variation with respect to temperature of a diode is about -1.2mV/°C. Weighted summation of the PTAT and CTAT currents will generate a temperature stable current reference. Figures 4.5 and 4.6 illustrate the simulation result of the proposed current reference. Reference [79] also utilizes the same design technique to generate reference current where a negative temperature coefficient resistor has been used. This work does not require a negative temperature coefficient resistor, in other word; special process demand for negative temperature coefficient resistor can be avoided.

Due to two different supply voltages being applied to the input pair and the current mirror load of the OTA, two temperature stable current references are required to adapt different supply voltage. The input pair of the OTA is connected to the 5.6V output from a shunt pre-regulator. Lower voltage current reference is designed for biasing the input pair of the OTA as shown in

Figure 4.7. The PTAT current of the LV current reference can be mirrored from bandgap voltage reference because both circuits share the same supply voltage. CTAT current is created by two stack diodes. The effective temperature coefficient of low voltage current reference is 75.3 ppm/°C and the effective temperature coefficient can be expressed as,

$$TC_{eff} = \frac{1}{I_{ref}} \left(\frac{I_{ref,max} - I_{ref,min}}{T_{max} - T_{min}} \right) \quad (4.14)$$

Figure 4.8 shows the schematic of the high voltage current reference which is designed for biasing the current mirror load of the OTA. The supply voltage is connected to the 9V output of the shunt pre-regulator. Cascoding device has been used to prevent the MOSFETs from exceeding device breakdown voltage limitation. The effective temperature coefficient of the low voltage current reference is 227.3 ppm/°C.

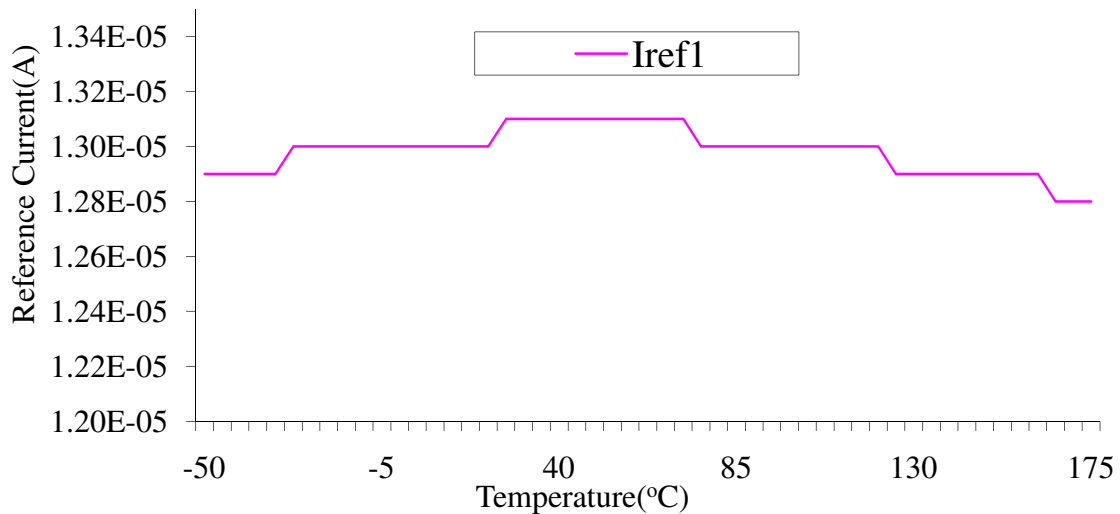


Figure 4.5 Simulation of low voltage reference current, 13μA

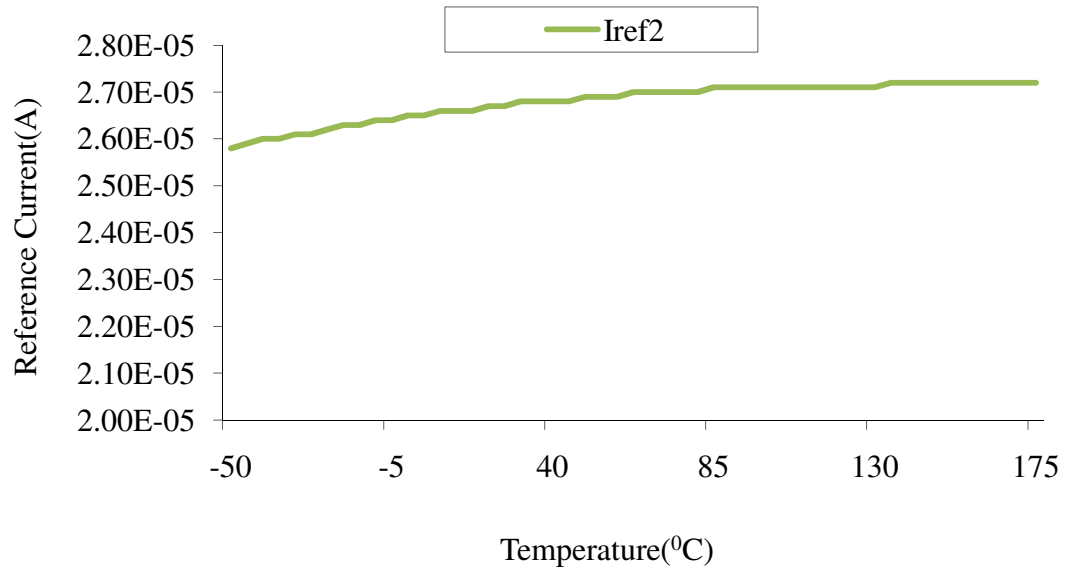


Figure 4.6 Simulation of high voltage reference current, 27 μ A

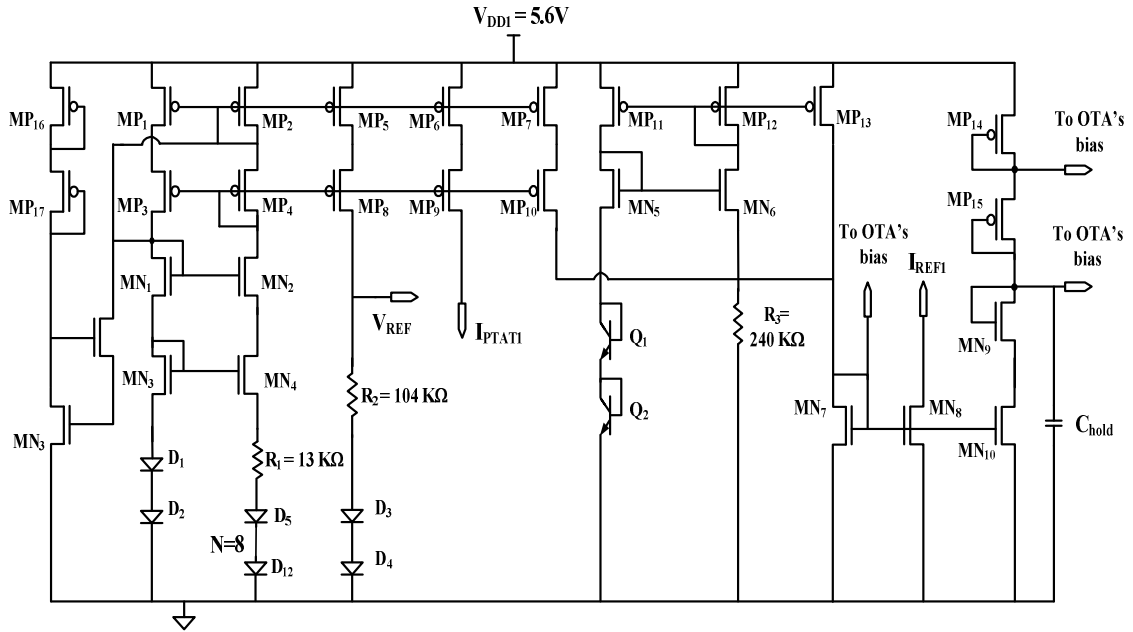


Figure 4.7 LV reference current, 13 μ A

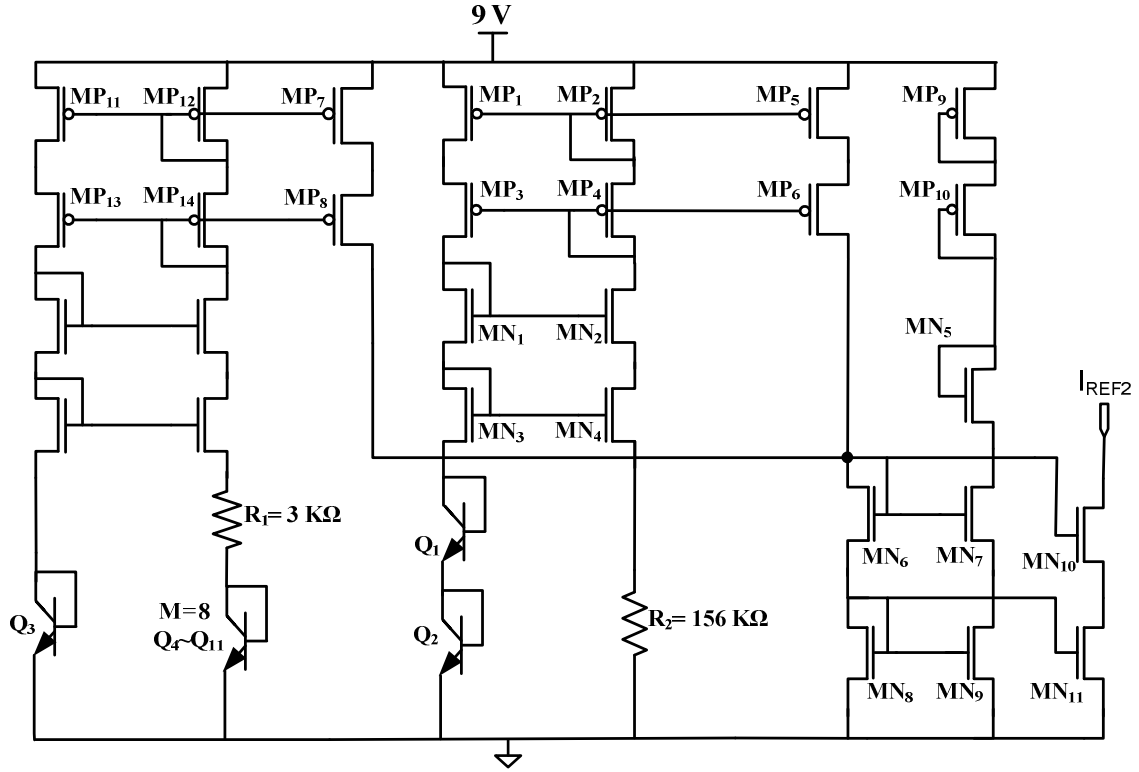


Figure 4.8 HV reference current with 27μA

From the Figure 4.7, the temperature coefficient of the proposed temperature stable current reference can be represented as,

$$I_{ref} = \frac{2 \cdot V_T \ln(N)}{R_1} + \frac{2 \cdot V_{BE}}{R_2} \quad (4.15)$$

Where N is the number of the diodes used in the PTAT leg, R_1 and R_2 represent the resistor in PTAT and CTAT leg, respectively, the ratio of $\frac{R_2}{R_1}$ is defined as K. The equation (4.15) can be rewritten as,

$$I_{ref} = \frac{2 \cdot V_T \ln(N)}{R_1} + \frac{2 \cdot V_{BE}}{K \cdot R_1} \quad (4.16)$$

Rearranging the equation (4.16) we get,

$$I_{ref} = \frac{2 \cdot V_T \ln(N) + 2 \cdot V_{BE}}{R_1 \cdot (1 + K)} = \frac{2}{R_1 \cdot (1 + K)} (V_T \ln(N) + V_{BE}) \quad (4.17)$$

Taking the derivative of equation (4.17) with respect to temperature,

$$\frac{\partial I_{ref}}{\partial T} = \frac{2}{R_1 \cdot (1 + K)} \left[\frac{-(K \cdot V_T \ln(N) + V_{BE})}{R_1^2} \cdot \frac{\partial R}{\partial T} + \frac{1}{R_1} \cdot \frac{\partial V_{BE}}{\partial T} + \frac{K \cdot V \ln(N)}{R_1} \cdot \frac{\partial V_T}{\partial T} \right] \quad (4.18)$$

Recalling the definition of temperature coefficient, $TCI_{ref} = \frac{1}{I_{ref}} \frac{\partial I_{ref}}{\partial T}$

Where I_{ref} is defined in equation (4.17), the temperature coefficient of the proposed temperature stable current reference is given by,

$$TCI_{ref} = -TCR + \frac{1}{V_T \ln(N) K + V_{BE}} \left(\frac{\partial V_{BE}}{\partial T} + \frac{\partial V_T}{\partial T} \cdot 2 \cdot K \right) \quad (4.19)$$

Where $\frac{\partial V_{BE}}{\partial T} = -1.2 \text{ mV} / ^\circ \text{C}$, $\frac{\partial V_T}{\partial T} = 0.085 \text{ mV} / ^\circ \text{C}$, $K = 18.46$, $N = 8$, the temperature coefficient obtained from equation (4.19) is approximately 60 ppm/ $^\circ \text{C}$, Table 4.7 compares the simulation results with the hand calculations of the temperature coefficient of the proposed temperature stable current reference.

From equation (4.19), if the temperature coefficient of the resistor R_1 is known, theoretically, by optimizing the ratio of K and N , the zero temperature coefficient temperature stable current reference can be achieved.

Tables 4.8 and 4.9 tabulate the dominant pole frequency, the gain, the phase margin and the unity gain bandwidth of the OTA using temperature stable current reference with and without

the PAD frame, respectively. The PAD frame contributes to the parasitic capacitance to lower dominant pole frequency.

Table 4.7 Comparison of the temperature stable current reference circuit

$TCl_{ref}(simulation)$	$TCl_{ref}(equation (4.19))$
75 ppm	60ppm

Table 4.8 Temperature stable current reference biases OTA with PAD frame

Temperature	Gain(dB)	f_{un} (MHz)	PM ⁰	f_{3dB} (Hz)
25°C	75	3	83.3 ⁰	514
50°C	74.85	2.75	83.3 ⁰	500
100°C	74.45	2.5	83.7 ⁰	470
150°C	73.8	2.3	83.4 ⁰	465
200°C	71.7	2.1	83.4 ⁰	545

Table 4.9 Temperature stable current reference biases OTA without PAD Frame

Temperature	Gain(dB)	f_{un} (MHz)	PM ⁰	f_{3dB} (Hz)
25°C	75	4.8	800	850
50°C	74.8	4.55	800	820
100°C	74.45	4.1	800	778
150°C	73.9	3.75	800	753
200°C	73.34	3.45	800	735

Figure 4.9 shows the simulation results of the output pole frequency variation of the OTA by using different biasing techniques. f_{3dB} represents the simulation of 3 dB frequency of the temperature stable biasing over temperature, f_{3dB_IPTAT} , $f_{3dB_constgm}$ represent PTAT biasing and , constant gm biasing, respectively. From Figure 4.9, it is evident that both the constant-gm biasing and the temperature stable biasing can maintain the dominant pole frequency effectively across a wide temperature range.

From Figure 4.10, one can easily identify that the temperature stable biasing can maintain the current and power consumption independent of the temperature. The constant- g_m biasing consumes more current and power at elevated temperatures. Figure 4.11 shows the comparison of the proposed temperature stable current reference with other publications which have been tabulated in Table 4.5, the X-axis represents the temperature and the Y-axis is the temperature coefficient. The red squares in Figure 4.11 represent the simulated temperature coefficient of the proposed current reference circuit.

Lastly, as mentioned in the previous section, the proposed temperature current reference circuit is utilized to bias operational transconductance amplifier. The I_{ref1} provides the bias current to the tail of the OTA while I_{ref2} provides the bias current to the cascade current mirror load. The quiescent current of OTA is governed by the temperature stable current reference.

Quiescent current consumption of OTA is expressed as $I_{OTA} = 4.8 * I_{ref1} + I_{ref2}$.

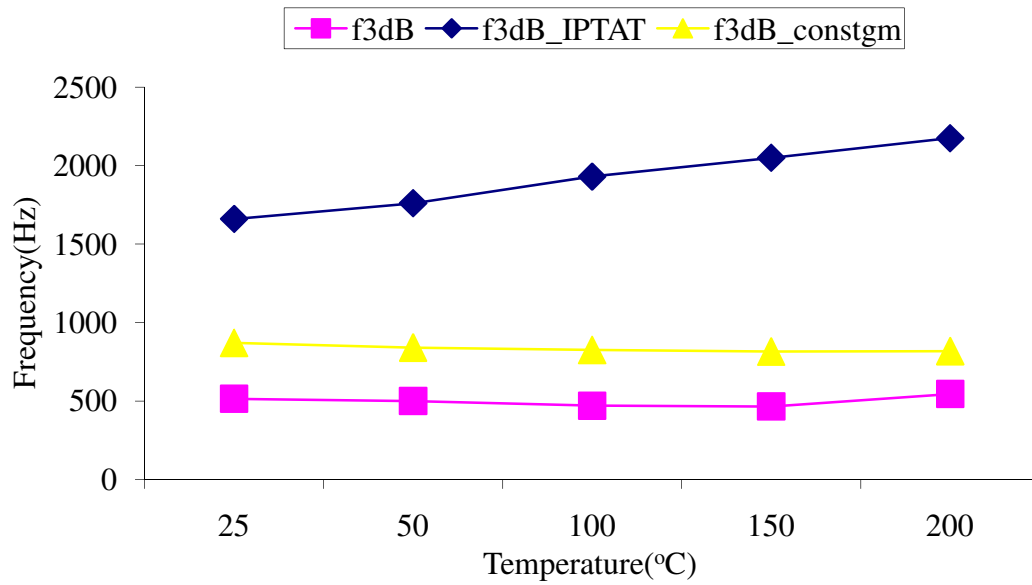


Figure 4. 9 Comparison of OTA output pole frequency

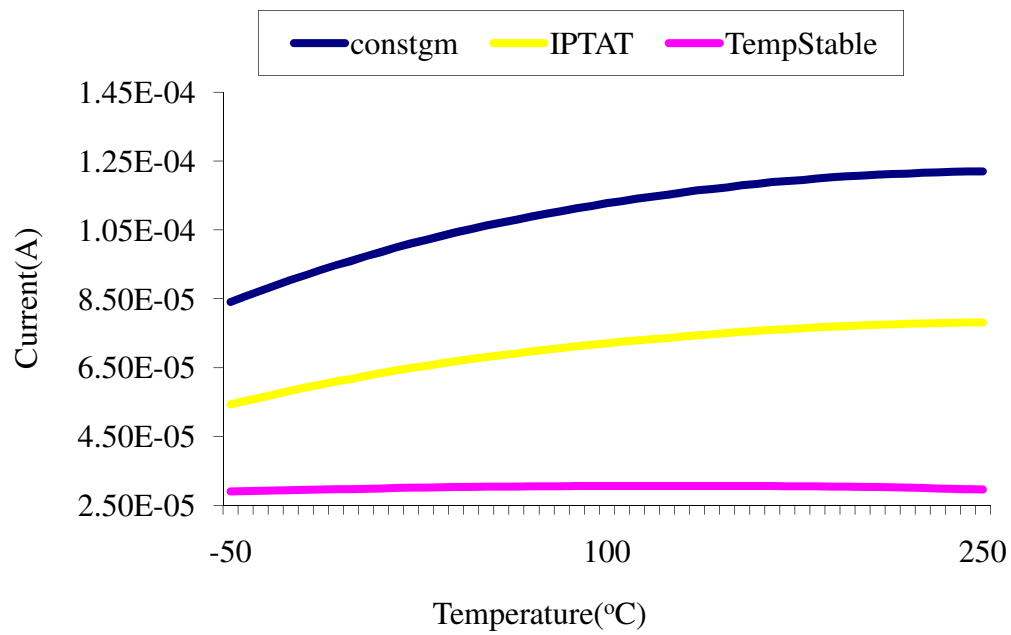


Figure 4.10 Simulation of different current reference circuit

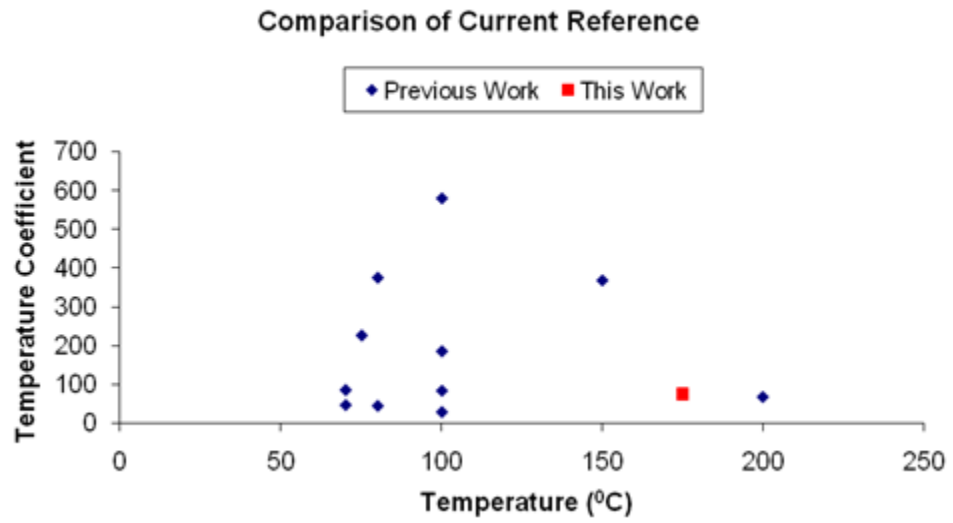


Figure 4.11 Comparison of current reference circuits, TC versus temperature

CHAPTER 5

Feedback, Stability and Compensation

In a linear voltage regulator, the negative feedback is applied to regulate the output voltage variation according to the load current variations. Therefore, the stability of a negative feedback amplifier is a very important issue to the overall system performance. An unstable negative feedback amplifier generates oscillation voltage. Meanwhile, a compensation technique is needed to guarantee stability. This chapter will discuss negative feedback, stability, frequency response analysis and compensation.

5.1 Negative Feedback and Stability

A negative feedback amplifier consists of four basic blocks [89]; a high gain amplifier, feedback network, sampling network and summing network. (see Figure5.1) The transfer function of negative feedback amplifier can be expressed as.

$$TF = \frac{Y}{X} = \frac{A_{OL}}{1 + \beta \cdot A_{OL}} \cong \frac{1}{\beta} \quad (5.1)$$

Both the summing and the sampling networks can sum and sample current or voltage signals. Four different negative feedback topologies are introduced as voltage amplifier (voltage sampled, voltage summed), current amplifier (current sampled, current summed), transimpedance amplifier (voltage sampled current summed) and transconductance amplifier (current sampled voltage summed). The properties of the four negative feedback amplifiers are listed in Table 5.1.

From the perspective of the negative feedback topologies, the linear voltage regulators can be considered as a voltage amplifier (voltage summed, voltage sampled), with theoretically infinite input impedance and zero output resistance. A fraction of the output voltage is sampled and fed back to the input of the error amplifier. The error amplifier will compare the feedback signal with the reference voltage. If the feedback signal is smaller than the reference voltage, the output voltage of the amplifier will increase. The NMOS pass transistor sources more current to the output node until the output voltage reaches the desired value.

For a negative feedback amplifier, the polarity of the loop gain βA_{OL} is always negative. The open loop gain A_{OL} can be calculated and simulated by breaking the feedback loop without disturbing the DC bias of the regulator. Figure 5.2 illustrates the AC simulation set up for A_{OL} of the regulator. The DC bias and the operating point should not be disturbed during the AC simulation.

Table 5.1 Summary of negative feedback topologies

Topology	Input Impedance	Output Impedance	Summing Network	Sampling Network
Voltage amplifier	Increased	Decreased	Voltage(Series)	Voltage(Shunt)
Current amplifier	Decreased	Increased	Current (Shunt)	Current(Series)
Transimpedance Amplifier	Decreased	Decreased	Current(Shunt)	Voltage(Shunt)
Transconductance Amplifier	Increased	Increased	Voltage(Series)	Current(Series)

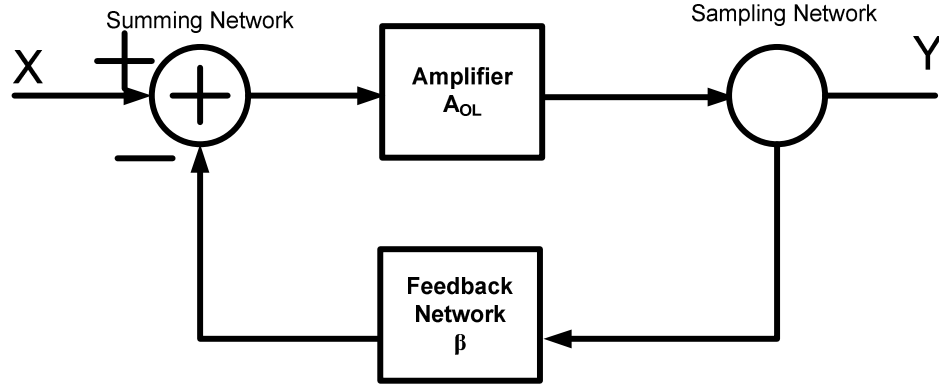


Figure 5.1 Simplified block diagram of negative feedback system

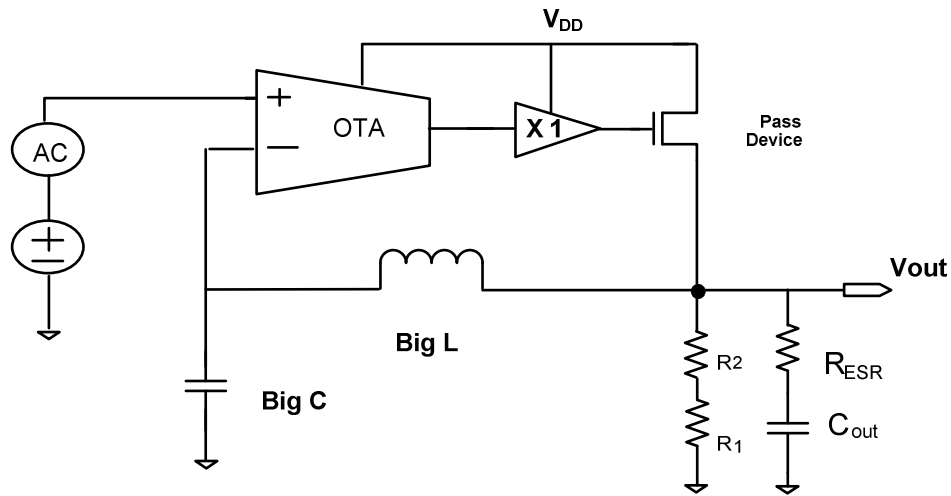


Figure 5.2 AC simulation configuration of the open loop gain of the regulator.

In Figure 5.2, the AC test source is added on the top of the DC voltage. The AC test signal will not disturb the DC operating point of regulator. Typically, the DC voltage comes from the band-gap voltage reference. A large L (large inductance) and a large C (larger capacitance) break the feedback loop and stabilize the DC bias and the operating point during simulation. The Bode plot is used to determine the frequency response of the regulator. According to Bakhausen's criteria, if the phase shift of the loop gain, βA_{OL} , equals 180° at unity gain, equation (5.1) goes to infinity and the system tends to oscillate [58].

5.2 Review of AC Analysis and Frequency Compensation

A single pole system is an unconditionally stable system because the single pole only contributes 90° phase shift and a slope of -20dB/decade in magnitude. In addition, a zero will contribute $+20\text{dB/decade}$ increment in the magnitude. (See Figure 5.3) But from the phase perspective, the LHP (Left Half Plane) zero contributes positive 90° phase shift from $0.1f_z \sim 10f_z$, the RHP (Right Half Plane) zero contributes negative -90° phase shift from $0.1f_z \sim 10f_z$. This is because in the mathematical representation, the LHP zero can be written as $(1 + S/\omega_z)$ and the RHP zero can be written as $(1 - S/\omega_z)$, as shown in Figures 5.4 and 5.5.

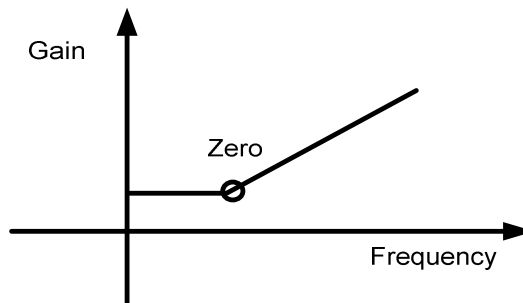


Figure 5.3 Gain Bode plot of zero (RHP and LHP)

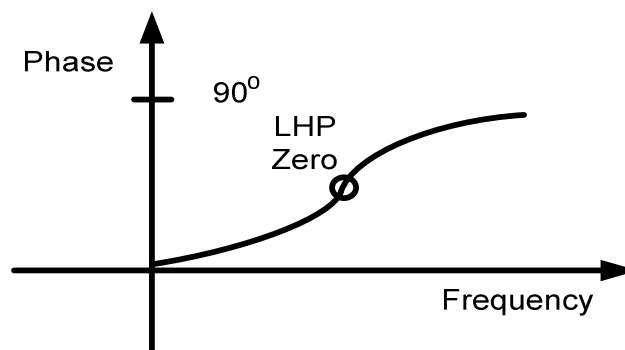


Figure 5.4 Phase Bode plot of zero (LHP)

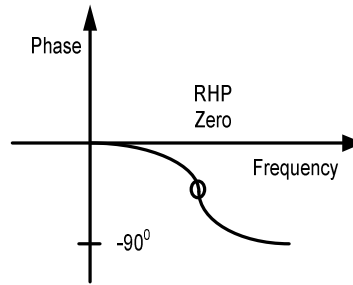


Figure 5.5 Phase Bode plot of zero (RHP)

Obviously, the RHP zero is an undesired effect in negative feedback amplifier design, because it adds extra phase shift. One can intentionally introduce LHP zero to compensate the 2nd pole inside the loop and improve the phase margin which can prevent amplifier from being unstable. The phase margin of a negative feedback amplifier needs to be greater than 45° at unity gain frequency. References [90~93] introduce the compensation technique and stability of linear voltage regulator.

Techniques for removing RHP zero can be found in literatures [58~64]. References [90~93] have reviewed fundamental concept of stability and frequency compensation for LDO voltage regulator. Recalled the Rincon-Mora's LDO regulator in chapter 2, the pole and zero location is listed in Table 5.2. The dominant pole of literature [16] is located at the output node of the voltage regulator. A frequency shaping amplifier is utilized to generate a pole/zero pair at the output of an error amplifier. The ESR zero is introduced to compensate the pole created by the by pass capacitor, and the current efficiency buffer will push P_3 to a higher frequency based on the loading condition.

Since the PMOS pass transistor has large output resistance, r_o , when the regulator is operating at very light load condition, the dominant pole is located at very low frequency due to large resistance seen at the output voltage node. Therefore, the unity gain bandwidth is a function of the dominant pole frequency.

Table 5.2 Pole and zero location of [14], from [14]

Pole and Zero	Location	Comment
P_d	Output of Voltage Regulator	Load Current Dependent
P_2	By pass capacitor	R_{esr} and by pass capacitor
P_3	Output of Voltage Regulator	At high frequency
Z_{esr}	Output Capacitor	R_{esr} and output capacitor
Unity Gain Frequency	Unity gain	Load Current Dependent

The low dominant pole frequency will slow down the transient response time. Reference [31] proposed a new frequency compensation technique to improve the transient response of P-type pass transistor LDO, both current buffer compensation and dynamic shunt feedback buffer are utilized to minimize the parasitic capacitance at the output of error amplifier. The loop is stable under no load condition because the 2nd pole (non-dominant pole) is pushed out of the unity gain bandwidth. In literature [31], the ESR zero does not require to enhance the phase margin]. Since all the non-dominant poles are outside of the unity gain frequency, this compensation method only has one pole (output pole) inside the feedback loop. The transient response, the phase margin and the stability are improved when the load current increases. The dynamic shunt feedback buffer greatly reduces the output resistance of the voltage buffer by using shunt feedback. This dynamic shunt feedback buffer is also called super source follower [59].

The output resistance of the dynamic shunt feedback buffer can be expressed as,

$$R_o \cong \frac{1}{g_{m1} + g_{mb}} \left(\frac{1}{g_{m2} r_{o1}} \right) \quad (5.2)$$

Since all the non-dominant poles are outside of the unity gain bandwidth, the doublet [94] created by imperfect pole/zero cancellation is avoided. The doublet is undesired in the feedback amplifier design as it slows down the transient response time of the amplifier.

Reference [26] reports two zero for the frequency compensation. A conventional compensation scheme for N-type pass transistor voltage regulator, the pole and zero frequency are listed in Table 5.3. The dominant pole frequency is fixed and is located at the output of the error amplifier. Hence, the unity gain bandwidth is limited and the transient response time is slow.

This compensation technique may have stability issue at ultra light load condition, because P_2 is load current dependent pole, moves lower than 4.8 KHz (200mA). The ESR zero is ineffective at ultra light load condition (10's μ A). A large value passive component will improve the stability at ultra light load condition at the cost of increased chip area.

Figure 5.7 illustrates the pole and zero location of [26], from this figure; one can observe the dominant pole is fixed regardless of loading condition.

Table 5.3 Pole and zero location of Bontempo's design [26]

I_{Load}	200 mA	5A
P_1	70 Hz	70 Hz
P_2	4.8KHz	41 KHz
Z_{esr}	8 KHz	8 KHz
Z_{comp}	1.6 MHz	1.6 MHz
Unity Gain Frequency	60 KHz	200 KHz

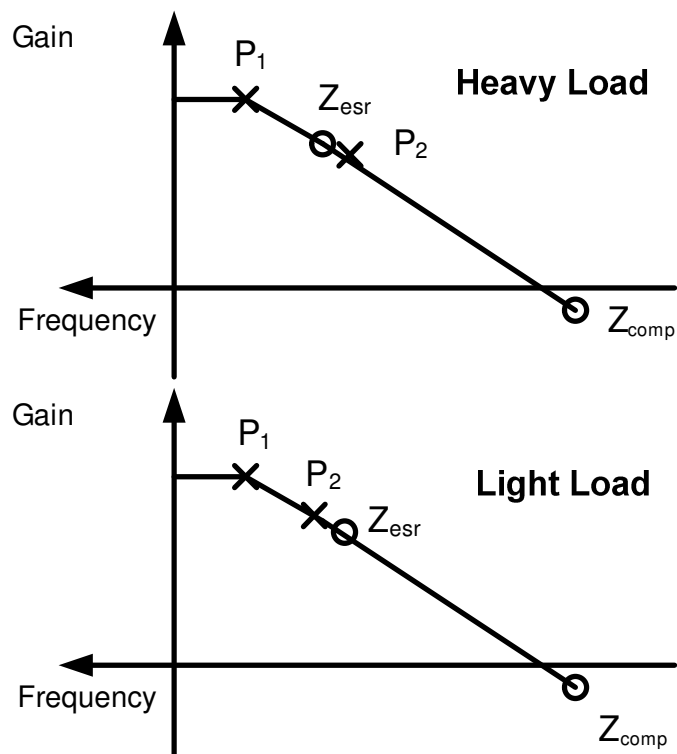


Figure 5.6 The Pole and zero location of [26]

5.3 Pole Swap Compensation Technique

A synchronized digital system (i.e. gate driver circuit) results in wide load current variation due to it switches at the clock edge. Meanwhile, the load current profile of the synchronized digital system is a fast impulse current waveform and it can be considered as the worst case load profile.

The fast load-dump complicates the load regulation of the regulator and thus requires fast recovery and settling times from the regulator to alleviate transient voltage variation at the regulator output. Without good load regulation, the synchronized digital system may result in digital fault. In addition, the high temperature environment places another limitation in designing analog integrated circuit (i.e. mobility degradation, gain bandwidth reduction...etc.). Therefore, a pole swap technique is proposed to tackle these problems.

Figure 5.7 shows the block diagram for AC frequency analysis. The feedback of regulator is intentionally broken for AC/Frequency analysis. Due to the NMOS pass transistor being utilized in the design, this topology offers no signal inversion, and RHP zero is avoided. The pass transistor stage can be seen as a common-drain amplifier (voltage buffer) and the V_{ref} is connected to the non-inverting (positive) terminal of the PMOS folded-cascode OTA while V_{fb} is connected to the inverting (negative) terminal. On the other hand, typical LDO (Low-Dropout) voltage regulator utilized PMOS as pass transistor and the connection of V_{ref} and V_{fb} to the input of OTA is reversed (V_{ref} to positive, V_{fb} to negative,). The transfer function of the regulator can be derived from this AC model.

In order to analyze the frequency response of the entire linear voltage regulator, it can be broken into three stages: the first stage being the OTA stage, and the voltage gain of OTA stage

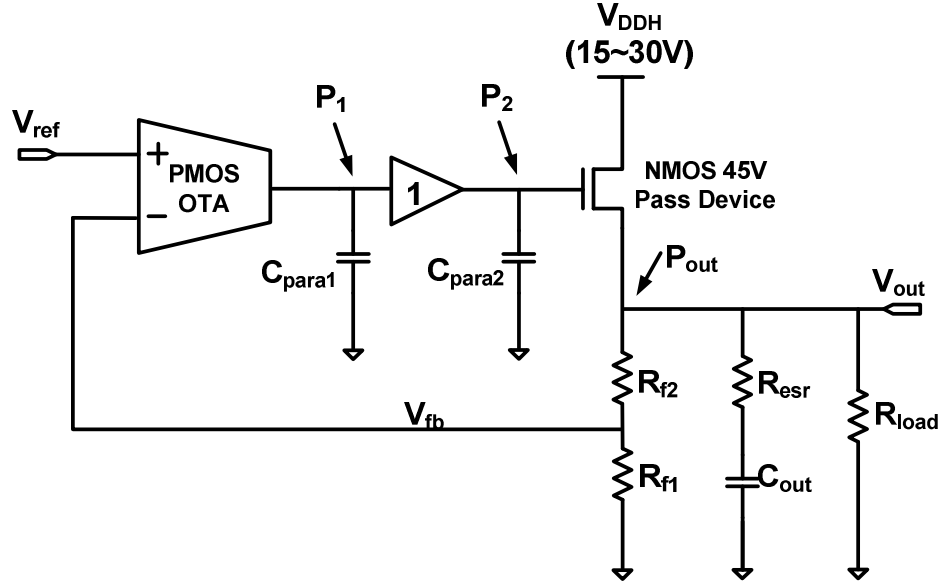


Figure 5.7 High temperature linear voltage regulator block diagram for AC/Frequency analysis

is represented by,

$$A_{v_{OTA}} = g_{m_{OTA}} \times \left(R_{o_{OTA}} \parallel \left(\frac{1}{sC_{para1}} \right) \right) \quad (5.3)$$

Where $g_{m_{OTA}}$ represents the transconductance of the OTA, $R_{o_{OTA}}$ is the output resistance of the OTA. C_{para1} is the parasitic capacitance at the output of the OTA. This parasitic capacitance and the output resistance $R_{o_{OTA}}$ form the pole P_1 , which is expressed as,

$$P_1 \cong \frac{1}{2\pi R_{o_{OTA}} C_{para1}} \quad (5.4)$$

The second stage is the voltage buffer stage. This buffer is added for frequency compensation purpose. Without this voltage buffer, the output resistance from the OTA and the parasitic capacitance from the huge pass transistor will create a pole at low frequency where the

regulator's output is located close to the pole. Two poles exist inside the loop and the voltage regulator may result in instability. The voltage gain of voltage buffer is expressed as,

$$Av_{buffer} = g_{m_buffer} \times \left(R_{o_buffer} // \left(\frac{1}{sC_{para2}} \right) \right) \quad (5.5)$$

Where g_{m_buffer} represents the transconductance of the voltage buffer, R_{o_buffer} is the output resistance seen from the voltage buffer (Common Drain Amplifier), which is $\frac{1}{g_{m_buffer}}$, C_{para2} is

the parasitic capacitance seen at the gate terminal of the pass transistor. This parasitic capacitance is proportional to C_{ox} of the pass transistor, typically, $C_{para2} \cong \frac{2}{3} C_{ox_pass}$,

$C_{para2} \cong 40 \cdot C_{para1}$ because the pass transistor is approximately 40 times larger than the transistor of voltage buffer. In addition, the current efficient buffer [14, 15, 16] topology is utilized. The BJT voltage buffer cannot be implemented in this work because the large input voltage exceeds the breakdown voltage limitation of the BJT. Therefore, HV NMOS (DMOS) buffer is utilized instead of BJT voltage buffer, and the transconductance of voltage buffer,

$$g_{m_buffer} = \sqrt{2\beta_{buffer} (I_{d_buffer} + 0.02 \cdot I_{Load})} ,$$

P_2 can be expressed as,

$$P_2 \cong \frac{g_{m_buffer}}{2\pi C_{para2}} \cong \frac{\sqrt{2\beta_{buffer} (I_{d_buffer} + 0.02 \cdot I_{Load})}}{2\pi (40) C_{para1}} \quad (5.6)$$

The third stage is the pass transistor; this transistor needs to be large enough to source hundreds of milliamperes of current during heavy load conditions. A 45V high voltage NMOSFET (DMOS) is utilized as pass transistor (W=24,000 μ m; L=1.5 μ m), the drain terminal of the pass

device is connected to V_{DDH} , which is varying from 10V~30V. The source terminal of the pass device is represents the output of the regulator. The voltage gain of the pass transistor stage is expressed as,

$$A_{v_{pass}} = g_{m_{pass}} \times \left(R_{o_{pass}} // (R_{f1} + R_{f2}) // R_{load} // \left(R_{esr} + \frac{1}{sC_{out}} \right) \right) \quad (5.7)$$

Where $g_{m_{pass}}$ represents the transconductance of the pass transistor, $R_{o_{pass}}$ is the output resistance looking into the source terminal of pass device, which is $\frac{1}{g_{m_{pass}}}$, R_1 and R_2 is the feedback resistor, R_{load} is the load resistor which is a function of the loading condition (heavy/light load), R_{esr} is the electrical series resistance of the output capacitor C_{out} , The above equation contains one pole, P_{out} , and one zero, Z_{esr} ,

$$P_{out} \cong R_{o_{pass}} // (R_{f1} + R_{f2}) // R_{load} \times \left(\frac{1}{2\pi C_{out}} \right) \quad (5.8)$$

$$Z_{esr} \cong \left(\frac{1}{2\pi R_{esr} C_{out}} \right) \quad (5.9)$$

The system transfer function (loop gain) of the regulator can be obtained by multiplying stage 1 through stage 3 and the feedback factor. The loop gain is expressed as,

$$LoopGain = A_{v_{OTA}} \times A_{v_{buffer}} \times A_{v_{pass}} \times \frac{R_{f1}}{R_{f1} + R_{f2}} \quad (5.10)$$

$$= g_{m_OTA} \left(R_{o_OTA} // \left(\frac{1}{sC_{para1}} \right) \right) g_{m_buffer} \left(R_{o_buffer} // \left(\frac{1}{sC_{para2}} \right) \right) g_{m_pass} \left(R_{o_pass} // (R_1 + R_2) // R_{load} // \left(R_{esr} + \frac{1}{sC_{out}} \right) \right) \frac{R_1}{R_1 + R_2} \quad (5.11)$$

$$LoopGain \cong (g_{m_OTA} \times R_{o_OTA}) \times \frac{\left(1 + \frac{s}{\omega_{z_esr}} \right)}{\left(1 + \frac{s}{\omega_{out}} \right) \cdot \left(1 + \frac{s}{\omega_1} \right) \cdot \left(1 + \frac{s}{\omega_2} \right)} \times \frac{R_1}{R_1 + R_2} \quad (5.12)$$

From equation (5.12), the negative feedback loop contains three poles and one zero, the locations of poles and zero are listed in Table 5.4

The pole P_1 is placed at the output of the OTA and the frequency of P_1 is approximately at 3 KHz when the regulator operates at heavy load condition (~100mA). P_1 is the dominant pole; P_{out} is the 2nd pole inside the unity gain frequency (non-dominant pole).

Table 5.4 Pole and zero location of high temperature linear voltage regulator

Pole and Zero	Location	Frequency
P_1	Output of OTA	3KHz~6KHz (C_{para1} is function of MOS operation region)
P_2	Output of Voltage Buffer	800KHz~30MHz (at relatively high frequency, Load Dependent)
P_{out}	Output of Voltage Regulator	80Hz~7KHz(Load Dependent, $C_{out}=10\mu F$)
Z_{esr}	Output Capacitor	15.9KHz
Unity Gain Frequency	Unity Gain	70KHz~5MHz

Figure 5.8 illustrates the pole and zero locations of a linear voltage regulator using the proposed pole swap technique. Z_{esr} compensates P_{out} , increases the phase margin. P_2 is located far away from the unity gain frequency which lessens its effect on the unity gain frequency. This enhances transient response time which is inversely proportional to closed loop bandwidth [15] as,

$$\Delta T_1 \cong \frac{0.37}{BW_{CL}} + C_{para2} \left(\frac{\Delta V_{para2}}{I_{buffer}} \right) \quad (5.13)$$

When the regulator is operating at a light loading condition (about 50 μA), P_{out} becomes the dominant pole because P_{out} is proportional to load current. As a result, P_{out} is located at a low frequency (~80 Hz). In the meantime, P_1 (~6 KHz, $C_{para1} \approx 0.8$ pF) becomes the second pole inside the unity gain frequency. (See Figure 5.9) When Z_{esr} compensates for P_1 , the unity gain bandwidth under light loading conditions moves down to approximately 70 KHz.

This pole swap technique will enhance transient response time (extended closed loop bandwidth) due to the dominant pole not being fixed at a certain frequency. As the load current magnitude increases, the unity gain bandwidth becomes wider. Meanwhile, the large output capacitor can also help to reduce the voltage droop during load current switching.

In addition, an increase in the value of the output capacitor and its ESR can also enhance the stability of the regulator by moving P_{out} and Z_{esr} to a lower frequency (Z_{esr} moves closer to P_1). AC simulation (Bode Plot) of light/heavy loading conditions across the temperature needs to be performed to ensure that the system is stable at elevated temperature (175°C) (see Figure 5.9 and Figure 5.10).

Figure 5.11 shows the phase margin (PM) of the high temperature linear voltage regulator as a function of the load current and the temperature. The PM increases with increasing temperature during heavy loading conditions.

Assuming the parasitic pole P_2 is a decade away from unity gain frequency, equation (5.12) can be simplified as a 2nd order system, and (5.12) can be rewritten as,

$$T(s) \cong \frac{A_{OL} \left(1 + \frac{s}{\omega_{z_esr}} \right)}{\left(1 + \frac{s}{\omega_{out}} \right) \cdot \left(1 + \frac{s}{\omega_1} \right)} \quad (5.13)$$

$$P.M = -a \tan \left(\frac{\omega}{\omega_{z_esr}} \right) + a \tan \left(\frac{\omega}{\omega_{out}} \right) + a \tan \left(\frac{\omega}{\omega_1} \right) \quad (5.14)$$

According to equation (5.13), the behavioral model can be developed in MATLAB, the frequency dependency of the output pole, P_{out} , and closed loop bandwidth can be plotted out. As shown in Figure 5.12 the loop bandwidth is increasing with the output pole frequency.

In conclusion, the pole swap technique offers feedback stability with wide load current range (10's μA ~ 100's mA), and adaptively optimize the loop bandwidth of the regulator for improving transient loading condition. In the meantime, the bandwidth of PSRR (power supply rejection ratio) is adaptively optimized with load current condition, this is because the PSRR is inversely proportional [16, 18, 19] to the open loop gain of the error amplifier. Theoretically, the frequency characteristic of the error amplifier will dictate the PSRR of the regulator.

On the other hand, the commercially available high temperature capacitors are made of ceramic and tantalum. The ceramic capacitor has low ESR compared to the tantalum capacitor, which can improve the voltage excursion during load-dumps. However, higher dielectric

constant ceramics (X7R, X8R, X9U) has a significant decrease in capacitances between 125°C~150°C [21], and it is not cost effective. Therefore, tantalum capacitor is utilized in this research, which offers moderate ESR, ($< 1 \Omega$) high capacitance (μF) and are cost effective.

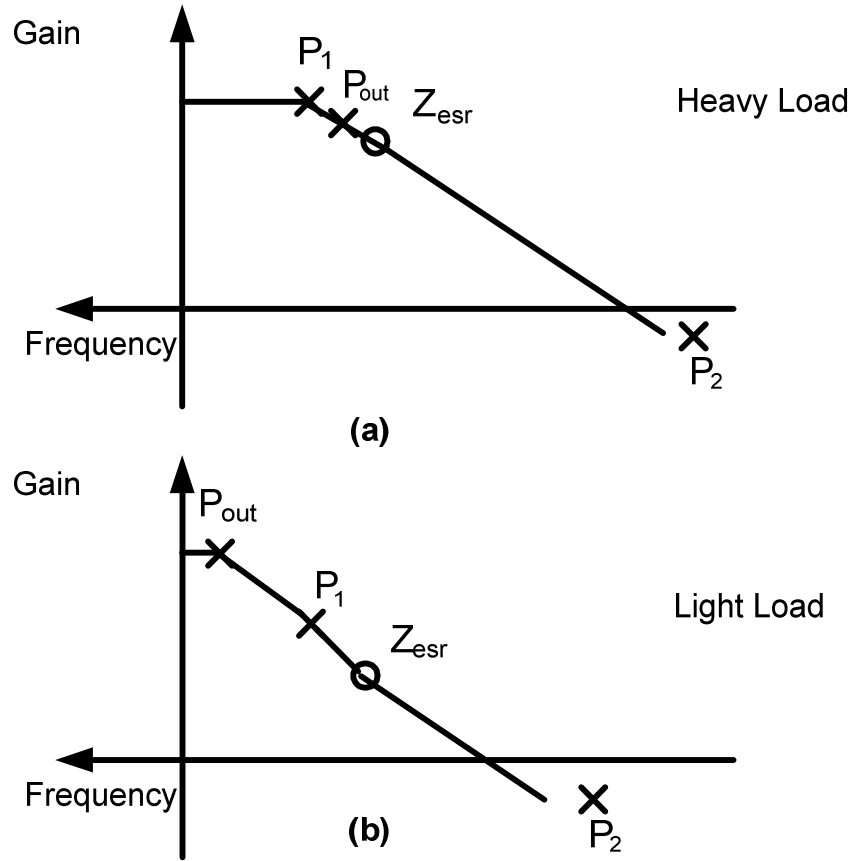


Figure 5.8 Pole and zero location of linear voltage regulator using the pole swap technique

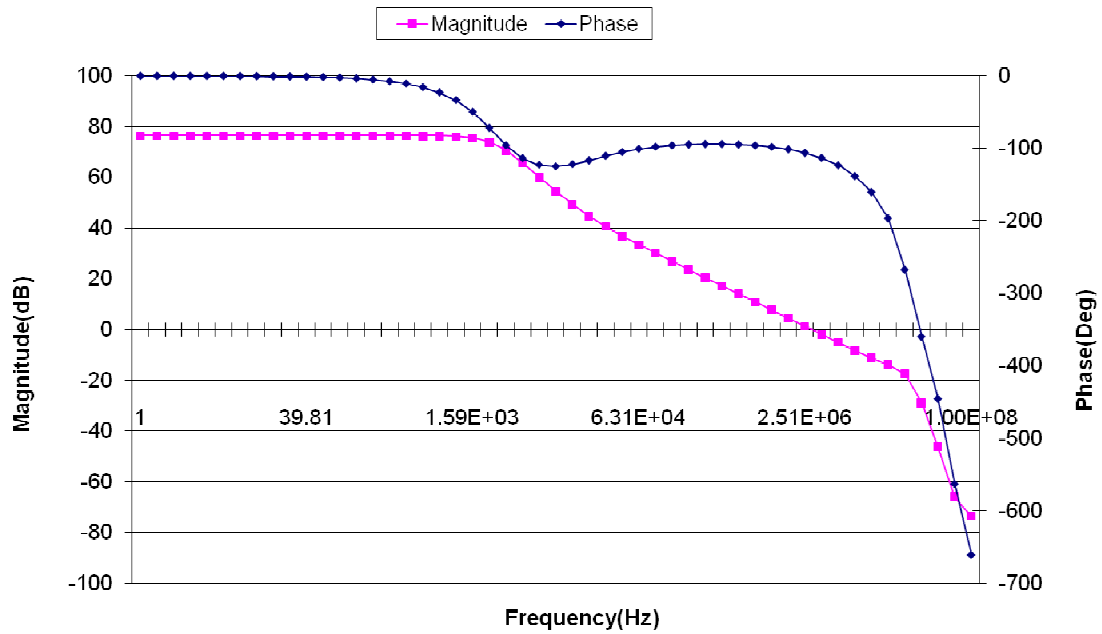


Figure 5.9 Bode plot of voltage regulator operates at heavy load (53mA), $T=175^{\circ}\text{C}$

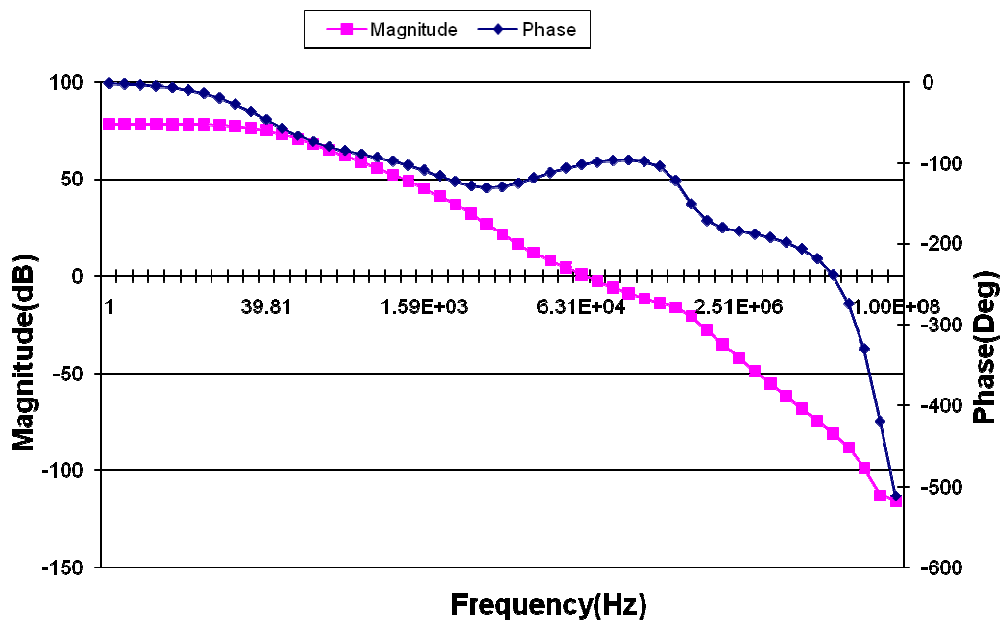


Figure 5.10 Bode plot of voltage regulator operates at light load (53 μA) , $T=175^{\circ}\text{C}$

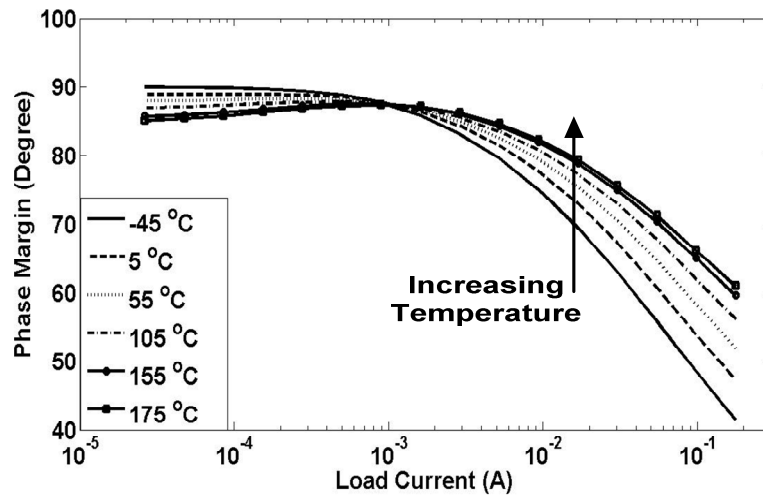


Figure 5.11 Simulation of Phase Margin as function of load current and temperature

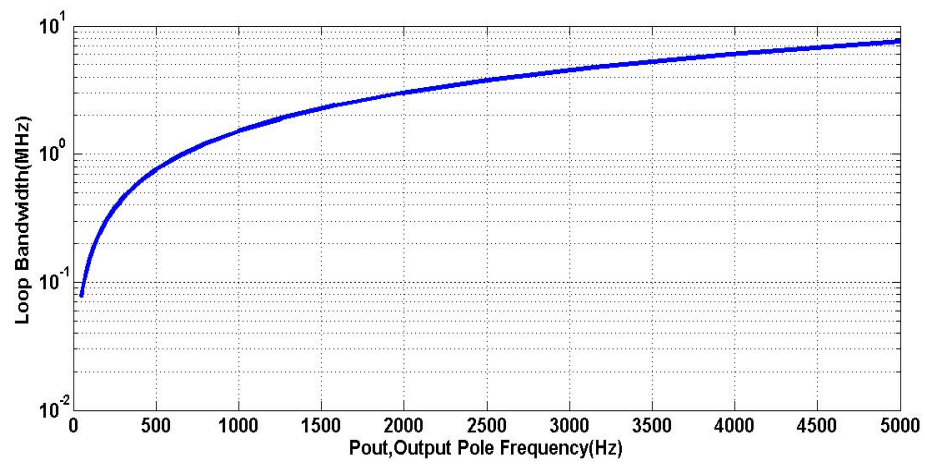


Figure 5.12 The location of P_{out} versus the loop bandwidth

CHAPTER 6

Prototype Implementation and Measurement

The circuit implementation of high temperature linear regulator is discussed in section 6.1. Figure 6.1 illustrated the block diagram of the high temperature linear voltage regulator. The circuit implementation of band-gap voltage reference, pre-regulator and voltage buffer are introduced in section 6.1. In section 6.2, the measurement environment setup is introduced and the regulator chip is tested up to 200°C. The data obtained from the measurements were compared with simulation results. Finally, the performance of high temperature linear voltage regulator is summarized in 6.3.

6.1 Circuit Implementation

The circuit block diagram of high temperature linear voltage regulator is shown in Figure 6.1. Previous chapters have presented the high temperature operational transconductance amplifier and the temperature stable current reference. Therefore the rest of circuit implementations are presented in this section. First, the implementation of shunt pre-regulator is introduced,

In addition, the final layout of the proposed high temperature linear regulator is shown in Figure 6.7. The micrograph of the chip is shown in Figure 6.8.

The reference current generation (high voltage) circuit. The 5.6 V (V_{DD1}) supplies voltages to the BGR (bandgap reference), the reference current generation (low voltage) and the input pair of the OTA. The purpose of the pre-regulator is to lower the V_{DDH} (10V ~ 30V) to 5.6 V and 9 V for preventing it from using HV NMOS/PMOS.

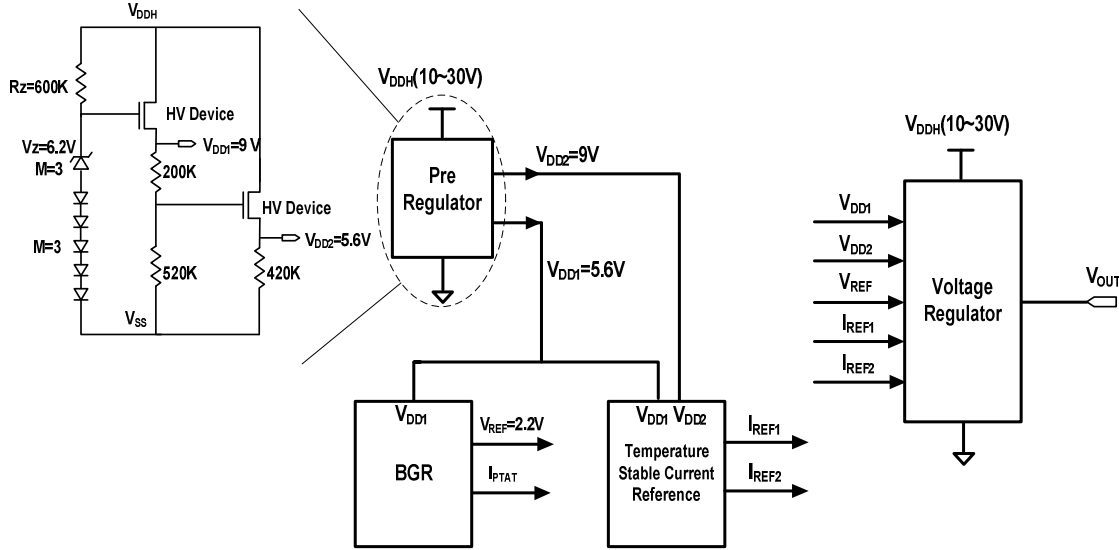


Figure 6.1 Block diagram of the high-temperature linear voltage regulator

With the lowered power supply, usage of the high voltage devices can be minimized; the regular devices are a factor of three times smaller than the high voltage device and provide better matching when designing the current mirror and the amplifier. In addition to the chip area efficiency, lower V_{DDH} will prevent the gate-source breakdown (maximum 5.5V) which occurs when using regular MOSFET. This pre-regulator can be seen as a reverse-battery protection circuit as well, due to the Zener diodes only provides a reference voltage (V_z) in reverse bias condition.

The shunt pre-regulator consumes $285\mu A$ at $175^{\circ}C$ as shown Figure 6.3. The 45V high voltage transistor is employed to source the current for the BGR, the temperature stable current reference and the OTA. The aspect ratio of the 45 V high voltage transistors is $500\mu m/1.6\mu m$. Three Zener diodes are paralleled together for sharing the current flow into each device. This is because the Zener voltage is stabilized at 6.2 V when I_z is between $0.1\mu A \sim 100\mu A$ at $-50^{\circ}C$. The Zener voltage (V_z) is a function of temperature, as well as the current flow into Zener diode (I_z). At $27^{\circ}C$, the stabilized output Zener voltage range is 6.4V when I_z between $0.3\mu A \sim 100\mu A$.

At 175°C, the stabilized output Zener voltage occurs at biasing I_z between 3 μ A~30 μ A, as shown in Table 6.1. Therefore a careful design selection of I_z is required. Biasing I_z in the range of 10's μ A will increase the quiescent current consumption. According to the I-V characteristic of the Zener diode, the minimum I_z for stabilized Zener output voltage is 3 μ A over -50°C ~175°C.

The Zener diode could be an option for implementing a reference voltage. The disadvantages of using a Zener diode as reference voltage are : the temperature dependence of the Zener voltage is the noisy and susceptible to surface charges [96].

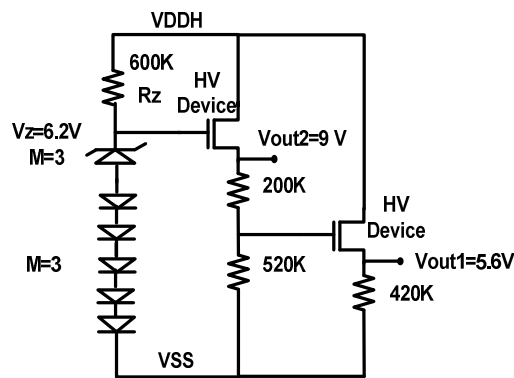


Figure 6.2 Schematic of shunt pre-regulator

Table 6.1 Temperature dependence of Zener diode

Temperature	I_z
-50°C (6.2V)	0.1 μ A ~ 100 μ A
27°C(6.4V)	0.3 μ A~100 μ A
175°C(6.8V)	3 μ A~30 μ A

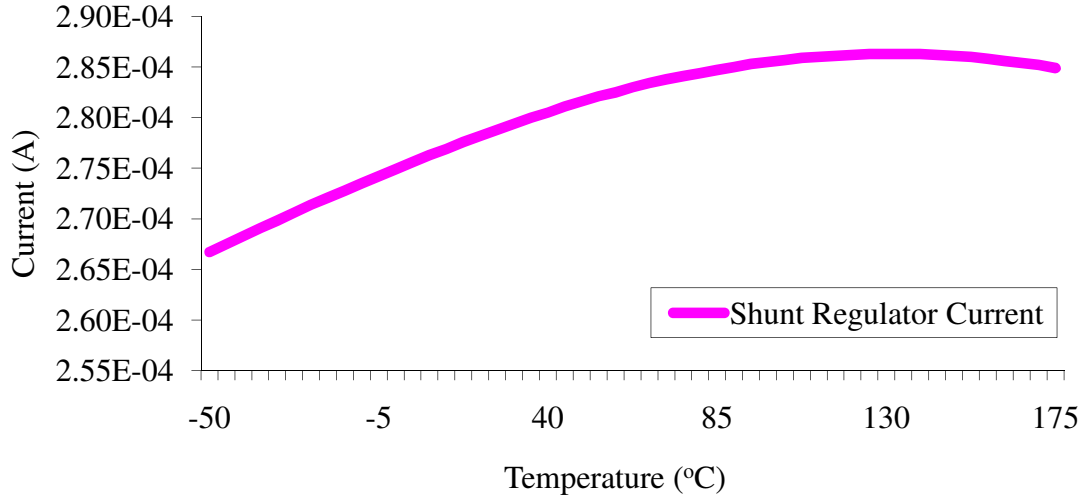


Figure 6.3 Current consumption of shunt pre-regulator

6.2.1. Band-Gap Voltage Reference

Figure 6.4 illustrates the schematic of the band-gap reference (BGR) circuit which provides the reference voltage to the non-inverting terminal of the folded-cascoded operational transconductance amplifier (OTA). The V_{ref} is designed to be at 2.2 V due to the feedback factor β which equals 0.415 (maximum feedback factor is 1). As discussed earlier in chapter 1, the load regulation is inversely proportional to the feedback factor. If the feedback factor can be maximized, the load regulator will be improving. A typical band-gap voltage reference utilizes 1.25 V which will further reduce the feedback factor. V_{ref} can be expressed as [64],

$$V_{ref} = 2V_{BE} + 2 \frac{R_2}{R_1} V_T \ln(K) \quad (6.1)$$

Here, V_{BE} is the base-emitter voltage of the bipolar junction transistor, V_T is thermal voltage, and K is the number of diodes in parallel; R_1 and R_2 are the resistors in the proportional to absolute temperature (PTAT) leg and the output reference voltage leg of the BGR circuit. The

second term of (6.1) can be used to cancel the negative temperature coefficient (TC) of the diodes, it is determined by the PTAT current generated by stacked diode voltage variation $2\Delta V_{BE}$.

Bandgap voltage reference is widely employed in linear voltage regulator and analog circuits and offers a temperature insensitive voltage which is suitable for high temperature or wide temperature application. Band-gap voltage reference is superior to the Zener diode voltage reference. Figure 6.5 shows the simulation of the BGR across temperature from -50°C to 175°C .

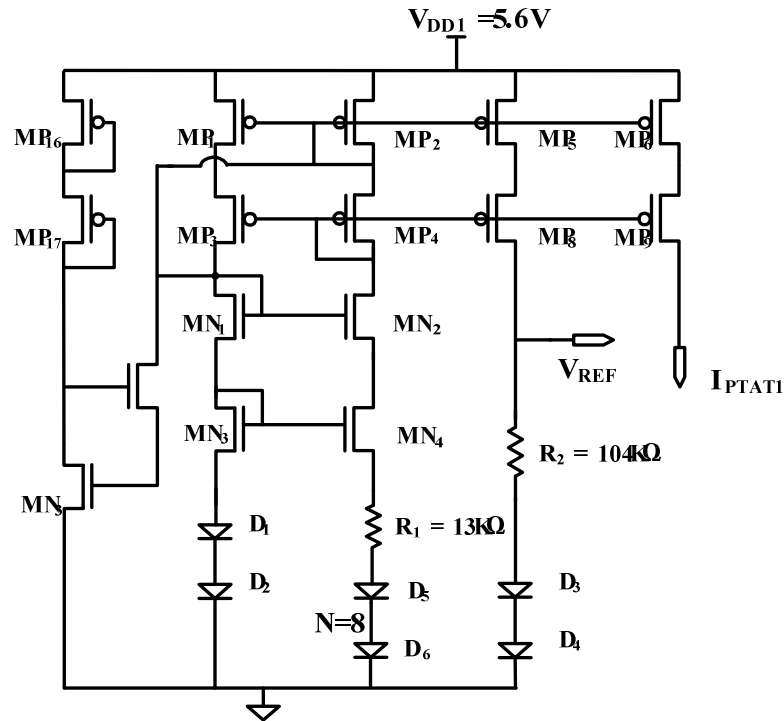


Figure 6.4 Schematic of bandgap voltage reference

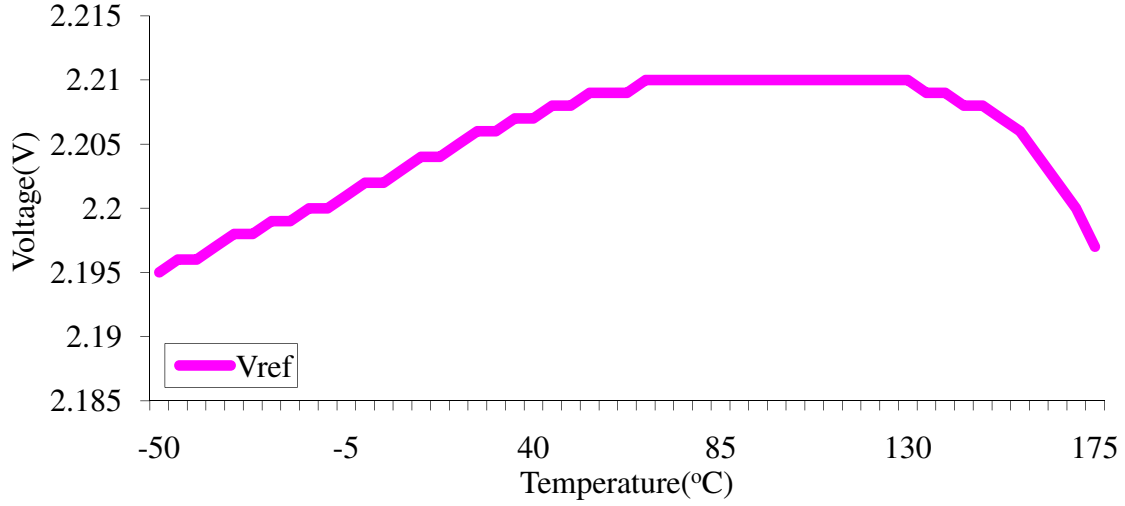


Figure 6.5 Simulation results of the bandgap voltage reference

6.2.2. Buffer, Pass Transistor and Chip Layout

Figure 6.6 illustrates the schematic of voltage buffer and the pass transistor, both the drain terminal of the voltage buffer and the pass transistor are directly connected to V_{DDH} . The voltage buffer is inserted to isolate the pole at the output of the OTA and the input of the pass transistor. As shown in Figure 6.6, N is a fractional number of the aspect ratio of the pass transistor which equals 0.02. When the voltage regulator sources large current to the load, the current consumption of the voltage buffer increases proportionally ($0.02I_{load}$), due to the effective current mirroring [14, 15, 161]. This will push the parasitic pole (P_2) location at the input of the pass transistor to higher frequency during large load current condition. In conclusion, the voltage buffer separates the output pole of the OTA and the parasitic pole at the gate-source terminal of the pass transistor pushes the parasitic pole to away during heavy load condition.

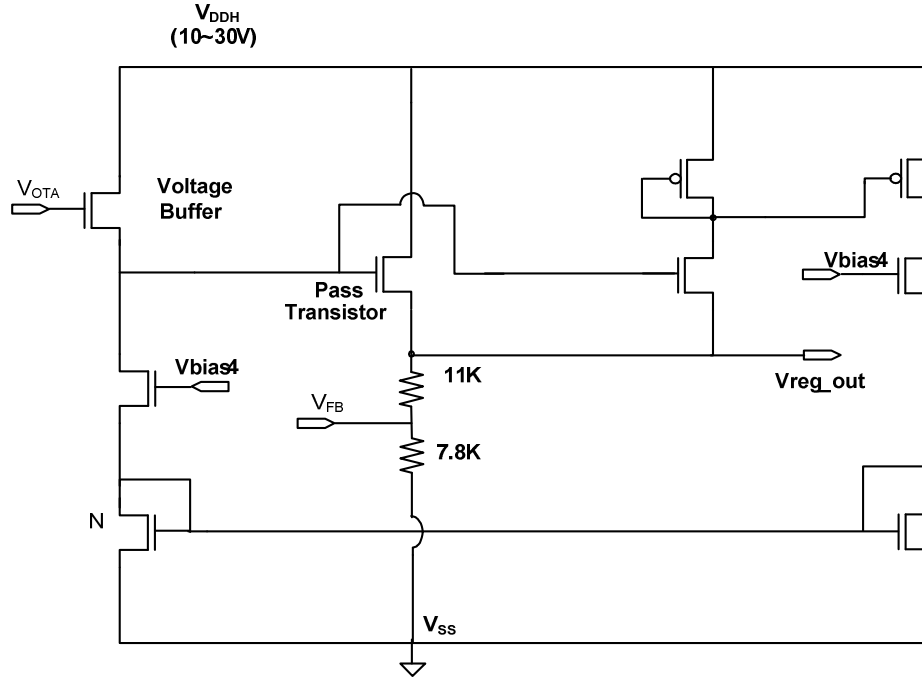


Figure 6.6 Schematic of the voltage buffer and the pass transistor

The size of the pass transistor is $24000\mu\text{m}/1.6\mu\text{m}$ which presents a large parasitic capacitance. The size of voltage buffer is $600\mu\text{m}/1.6\mu\text{m}$ and the large voltage buffer is utilized to drive parasitic capacitance at the gate of pass transistor, and speed up the transient response.

In a high temperature linear voltage regulator, a pass transistor is operated at elevated temperature and at high current. The layout of pass transistor requires special care and attention. References [95, 96, 97] present the layout rules of analog integrated circuits. A modular transistor structure is utilized in the layout of the pass transistor. A total of 1,200 transistors with aspect ratio of $20\mu\text{m}/1.6\mu\text{m}$ are employed as pass transistor. In addition, the pass transistor generates heat while sourcing hundreds mA to the load, it will cause severe thermal gradients within the chips [95].

Reference [95] suggests that the pass transistor is desired to be placed along one edge of the chip. Meanwhile, the others analog circuits on the chip are along the same isothermal contour. Figure 6.7 shows the layout of high temperature linear voltage regulator.

Figure 6.8 shows the chip micrograph of the high temperature linear voltage regulator. The core area of the voltage regulator is 3.24 mm^2 ($1700 \text{ } \mu\text{m} \times 1800 \text{ } \mu\text{m}$). To alleviate electro-migration at high temperatures, metal interconnections were drawn 1.5X wider than the requirement of the foundry design rules. Each individual sub-block is surrounded by a trench, and the chip was packaged in a Kyocera DIP40 ceramic package. The ceramic package is suitable for high temperature application.

In addition, reference [4] indicates the latchup immunity can be enhanced by utilizing special layout design rule. These include adequate spacing between the p-active and the n-active areas, majority and minority carrier guard structures; multiple, butted, source-to-well and source-to-substrate contacts and separated p- and n-devices [4].

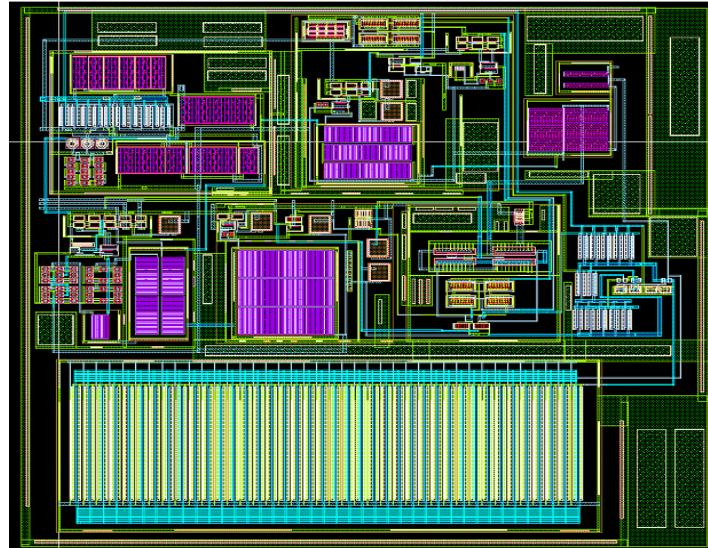


Figure 6.7 Chip layout of high temperature linear voltage regulator(chip layout area is 1.7mm x 1.8mm)

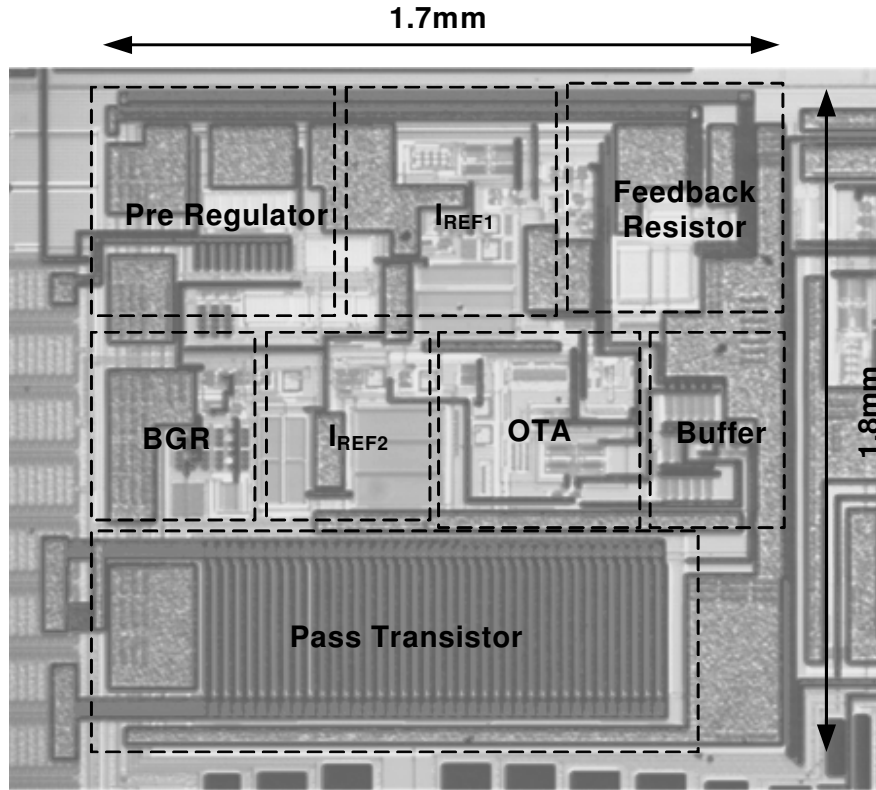


Figure 6.8 Chip micrograph of high temperature linear voltage regulator

6.2 Prototype Measurement

In this section, the measurement environment setup is introduced; the high temperature measurement is performed in a temperature chamber. High temperature solder and wires with Teflon jacket are used during the high temperature testing. In addition, a two layer polyimide PCB test board was built for sustaining high temperature testing environment as well.

The experimental result of line regulation, load regulation, transient response, quiescent current, reference voltage, current reference of high temperature linear regulator chip are presented in this section. Table 6.2 tabulates the test instruments used in prototype measurement. Figure 6.9 shows the high temperature testing setup. The polyimide PCB test board and regulator chip is inside the high temperature chamber where the maximum temperature is 200°C.

Table 6.2 Test Instruments

TYPE	Features
Agilent E3620A Dual Output DC Power Supply	0~6V; 0~25V
Agilent 33220A Waveform Generator	Maximum 20 MHz Sinewave.
Keithley 2400 source meter	μ A current measurement
Agilent 34401A Digit Multimeter	6.5 bits
Topward Dual-Tracking DC Power Supply 6302D	5V; 0~35V
Lenovo Laptop	With Matlab ,MS Office
Delta Design Temperature Chamber	High temperature chamber
Agilent MSO6034A Mixed Signal Oscilloscope	300MHz Bandwidth, 2 G sample per second.

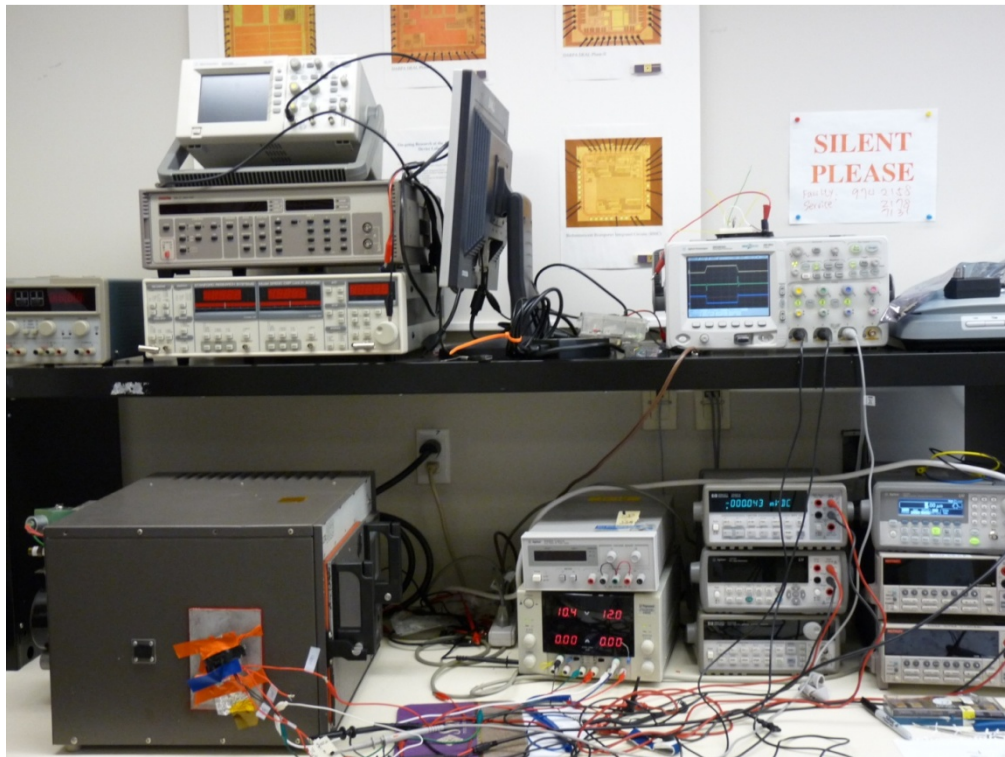


Figure 6.9 High temperature testing setup of high temperature line voltage regulator

6.2.1. Quiescent current test

The quiescent current test is performed while the regulator is operated at no load condition. The current consumption measured from the current meter is the quiescent current of the regulator. During the quiescent current testing, the input DC voltage is varying from 10V to 30V. Figure 6.10 shows the quiescent current of regulator chip 1 thru chip 4 at room temperature of 25°C. Figure 6.11 shows the quiescent current of the regulator chip at temperature of 25°C, 55°C, 105°C, 155°C, 175°C and 200°C. The input DC voltage has been varied from 12 V to 30 V.

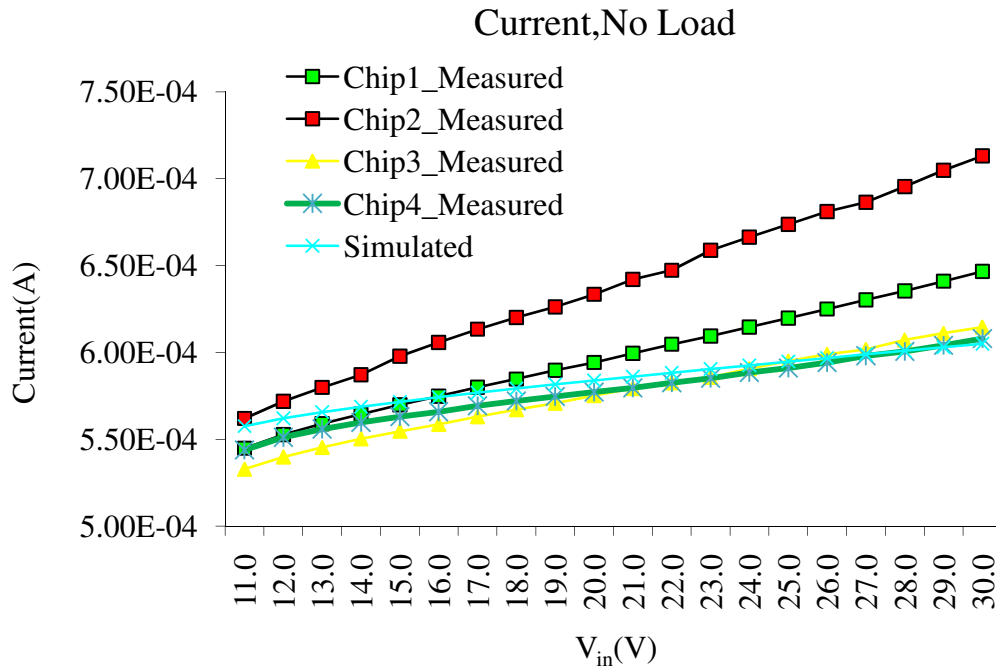


Figure 6.10 Quiescent current of high temperature line voltage regulator Chip1~Chip4 at room temperature

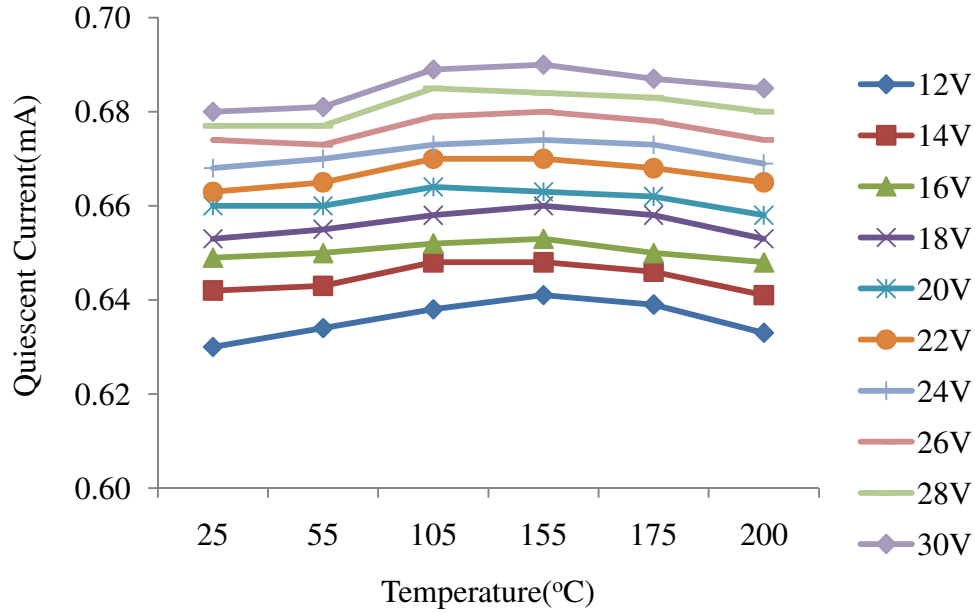


Figure 6.11 Quiescent current of regulator at different temperatures

6.2.2. Load regulation test

The load regulation is an important specification to evaluate the performance of a voltage regulator. The lower output voltage variation between the no load condition and the loading condition represents the better regulator performance. The load regulation test is performed while the regulator is operated at no load condition and regulator is operated at a pure resistive load condition. During the load regulation testing, the input DC voltage is varying from 10V to 30V. Figure 6.12 shows the load regulation of the regulator chip 1 and chip 4 at room temperature of 25°C. Both the chip1 and the chip2 were tested with a maximum of 11 mA of load current. The ΔV_{out} shown in the Y-axis of Figure 6.12 represents the load regulation. The average load regulation of chip1 and chip2 are 300 μ V/mA, 350 μ V/mA, respectively.

Figure 6.13 shows the load regulation of regulator chip at temperature of 25°C, 55°C, 105°C, 155°C, 175°C and 200°C. The input DC voltage has been varied from 10 V to 30 V. In Figure 6.13, the load regulation degrades with increasing temperature and increasing input DC

voltage due to the effect of reduced DC voltage gain at elevated temperature and increasing R_{on} of the pass transistor and due to the ambient temperature reaching the device limitation. Figure 6.14 illustrates the line regulation at room temperature with heavy load (55mA, 116mA, 188mA). When the maximum DC current is 188mA, the ΔV_{out} is approximately 100 mV.

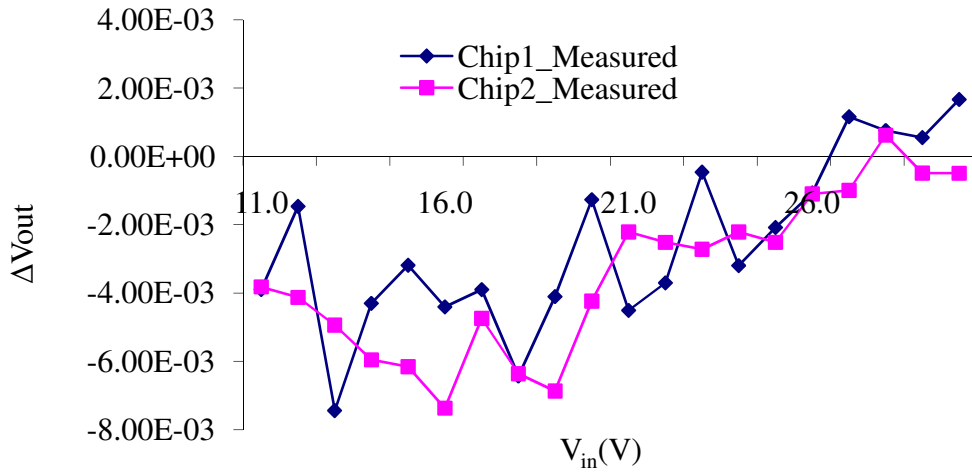


Figure 6.12 Load regulation at 25°C, 1mA-11mA

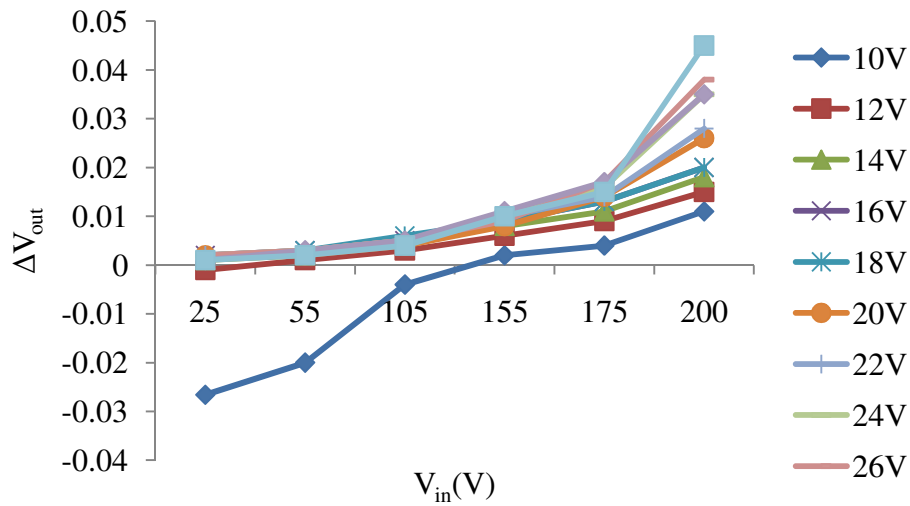


Figure 6.13 Load regulation at different temperature, 0mA-12mA

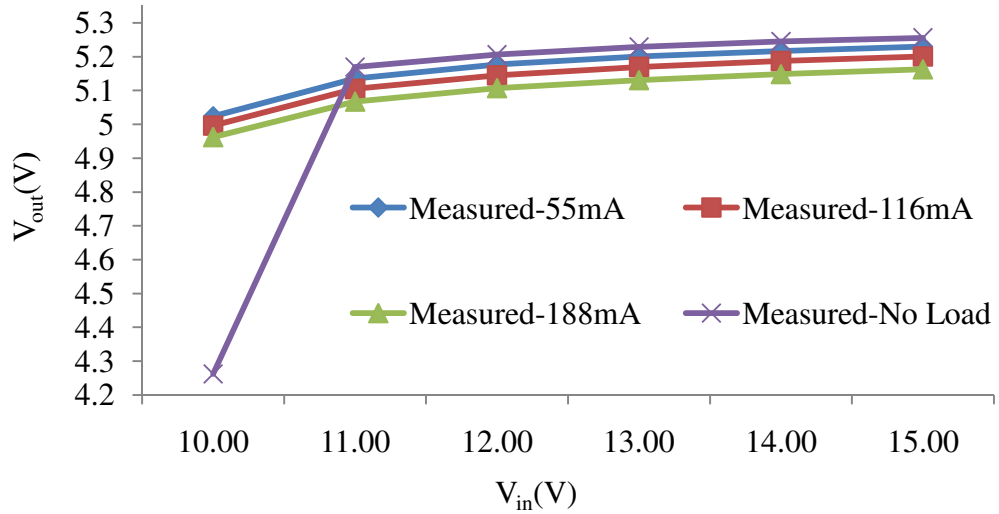


Figure 6.14 Load regulation (55mA, 116mA, 188mA), 25°C

6.2.3. Line regulation test

The line regulation test is performed while the regulator is operated at no load condition or the regulator is operated at a pure resistive load condition. During the line regulation testing, the input DC voltage is varying from 10V to 30V. The lower output voltage variation with the increasing input DC voltage represents the better line regulation performance.

Figure 6.15 shows the line regulation of regulator chip at temperature of 25°C, 55°C, 105°C, 155°C, 175°C and 200°C. When the regulator is operated at 200°C, the line regulation is 3.83mV/V ($V_{in} = 12V \sim 30V$), This represents the output voltage of regulator only varies 3.83 mV per volt over input DC voltage. Furthermore, the line regulation can be reduced to approximately 0.7 mV/V when input voltage (V_{in}) is between 20V ~30V.

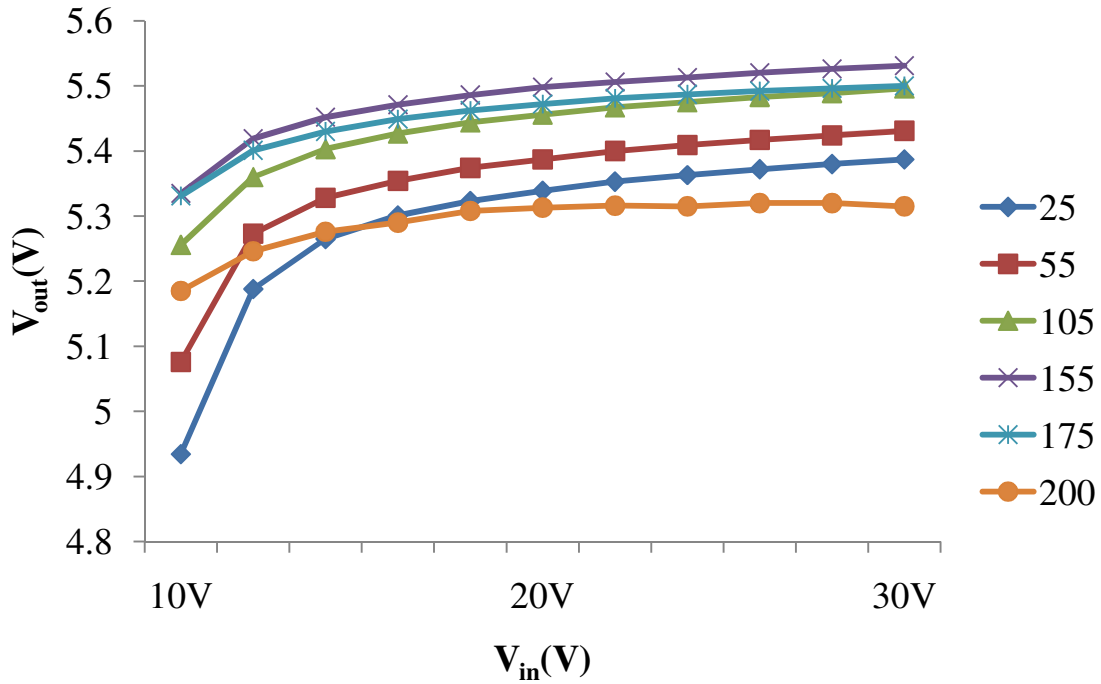


Figure 6.15 Line regulation at different temperature, $I_{Load}=12mA$

6.2.4. Transient response test

The transient response test is performed while the regulator is operated at a switching load condition. During the transient response measurement, the input DC voltage is varied from 10V to 30V. The output node of the regulator is connected to a 50 mA switching load current with 2 μs pulse width at 25 °C. The rise time of switching current profile is 100 ns, this current profile mimics the load current profile of a synchronized digital system (i.e. gate-driver).

The transient response test is performed at temperature of 25°C, 55°C, 105°C, 155°C, 175°C and 200°C. Figure 6.16 shows the transient response test at room temperature. The middle trace in Figure 6.16 is the output voltage waveform measured at the output node of the regulator and the measured transient response time is less than 150 ns. The top trace is the input voltage with a pulse changing from 0 V to 5 V and the bottom trace represents the drain voltage change

of the test NMOS. Under this condition, the output just has a voltage fluctuation of about 200 mV, which is less than 4% of the output voltage.

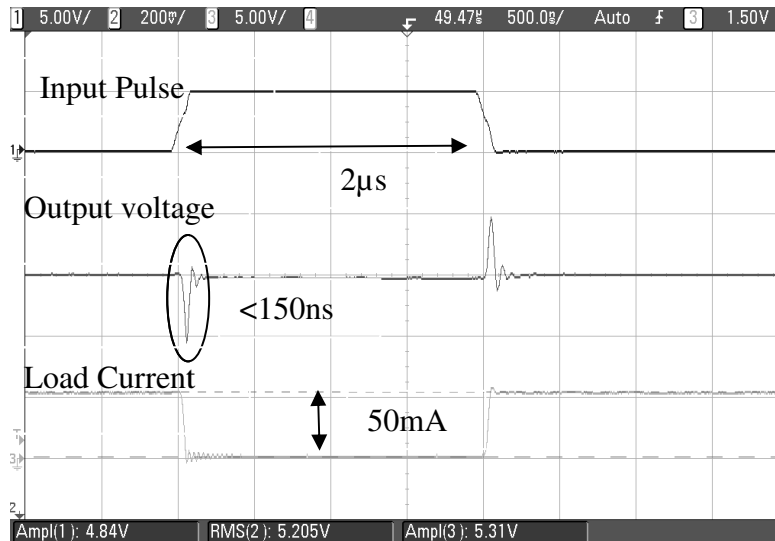


Figure 6.16 Transient response test at 25°C, $I_{Load}=0\sim50\text{mA}$

Figure 6.17 Transient response test at 200°C, $I_{Load}=0\sim50\text{mA}$

Figure 6.17 shows the measurement result at 200°C under the same test condition while the transient response time remains unchanged. In Figure 6.17, the transient voltage variation of the output of the regulator increases at least fourfold compared to Figure 6.16. This is due to the long wire being used to bring the test point outside of the temperature chamber. The long wires contribute huge parasitic and deteriorate the measured transient response. A high-temperature probe may help reduce the measured transient response.

On the other hand, Figure 6.14 shows the test results at room temperature. A long wire can be avoided in bringing the test point out of the high temperature environment. Hence the test point of Figure 6.14 is very close to the output voltage node of the regulator. Figure 6.18 shows the measurement result at 175°C under the same test condition, the transient response time still remains unchanged.

Figure 6.19 is the output voltage waveform measured at the output node of the regulator and the measured transient response time is roughly less than 250 ns. The upper trace is the output waveform while regulator is connected to a 181 mA switching load, and the bottom trace represents the input voltage with a pulse changing from 0 V to 4.38 V.

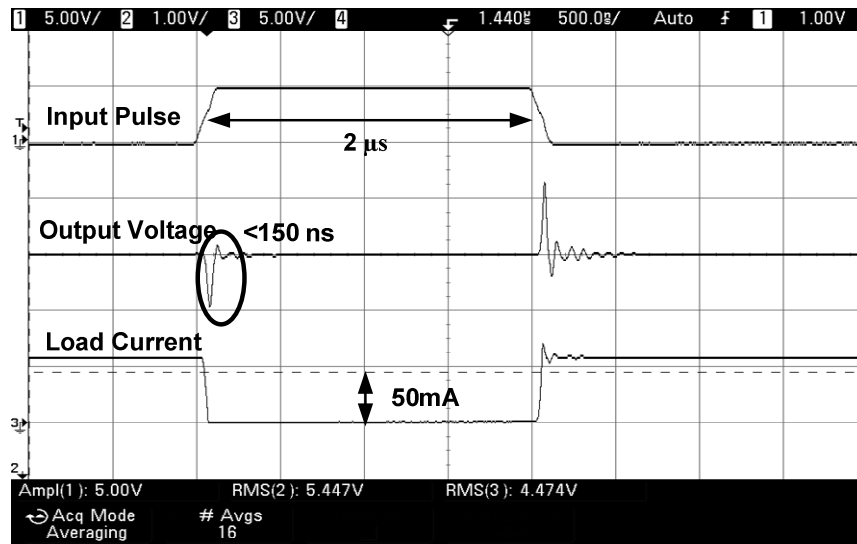


Figure 6.18 Transient response test at 175°C , $I_{\text{Load}}=50\text{mA}$

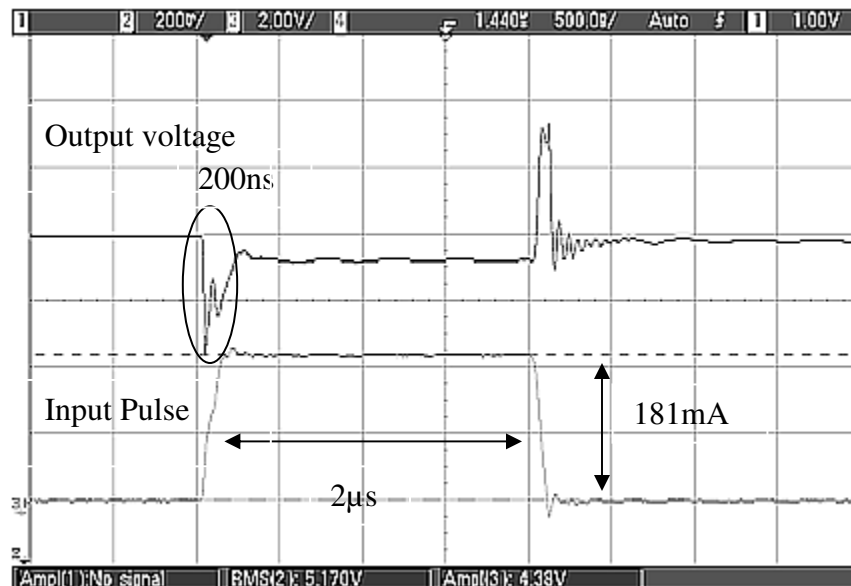


Figure 6.19 Transient response test at 25°C , $I_{\text{Load}}=181\text{mA}$

6.2.5. Bandgap voltage reference test

The bandgap reference circuit is the core of the linear regulator. The bandgap reference (BGR) circuit provides the reference voltage to the input of the OTA (error amplifier). During the voltage reference measurement, the input DC voltage is varied from 10V to 30V. Figure 6.20 shows the measured reference voltage variations over temperature from 25°C to 200°C. The maximum reference voltage variation is about 3% from 25°C to 200°C.

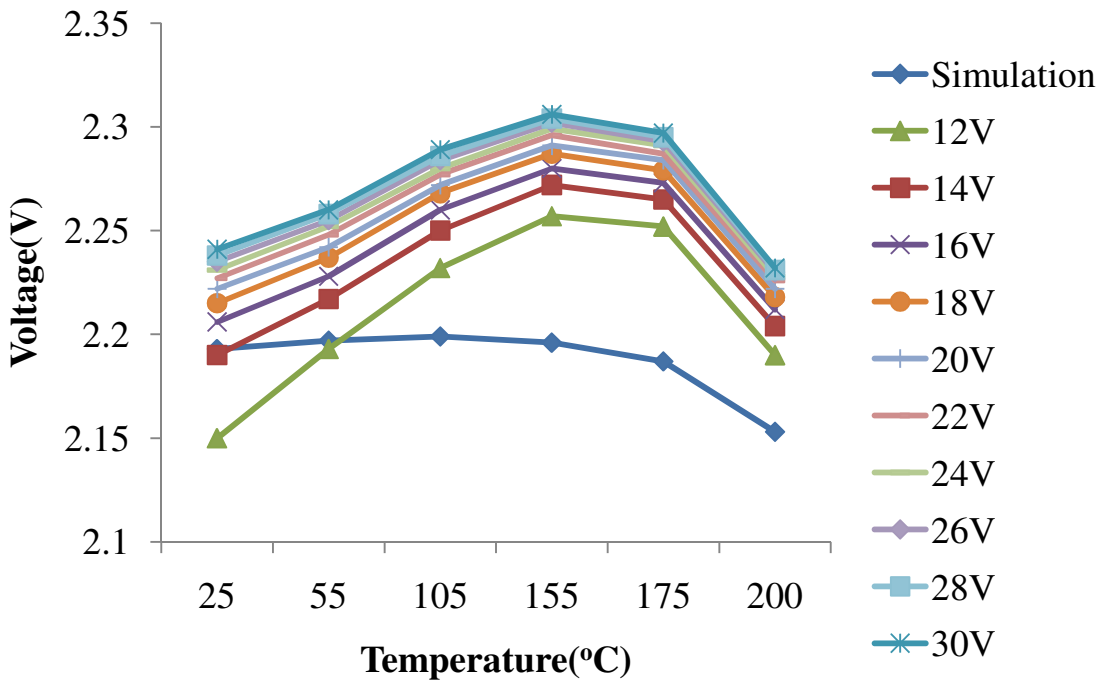


Figure 6.20 Measured results of the bandgap voltage reference

Figure 6.21 shows the measured reference voltage variations with varying input DC voltage from temperature of 25°C to 200°C. At 200°C, the reference voltage variation respect to input DC voltage is approximately 70 mV from $V_{in} = 10V \sim 30V$. The reference voltage variation will be further reduced to 10 mV at 200°C when V_{in} is between 20V \sim 30V. In conclusion, the line regulation of reference circuit can be normalized as 3.5 mV/V and 1mV/V, respectively. It is obvious that the bandgap voltage reference circuit shows better voltage

variation with respect to V_{in} . This voltage reference circuit is targeted for high temperature environment at the beginning of design process.

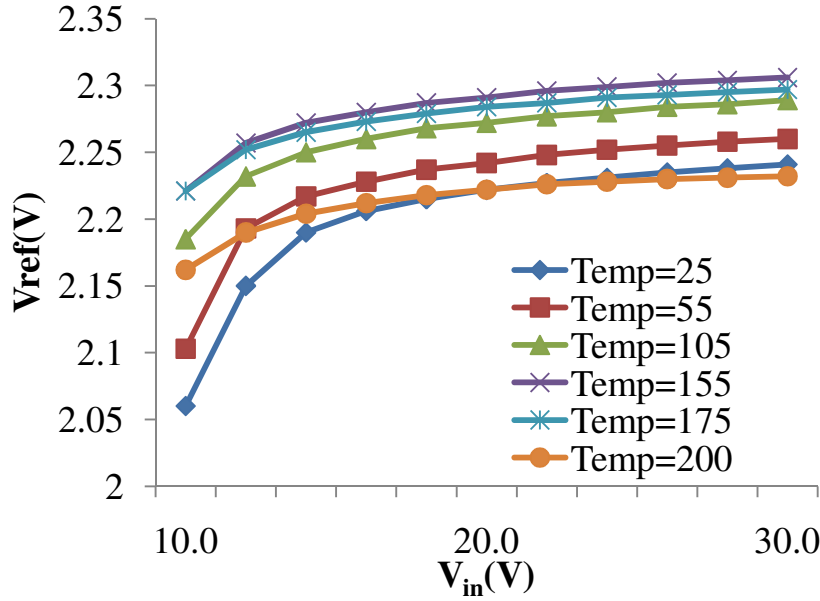


Figure 6.21 Measured results of the bandgap voltage reference respect to the input voltage

6.2.6. Temperature stable Current Reference Test

The temperature stable current reference circuit provides the biasing current to the input of the OTA (error amplifier). During the current reference measurement, the input DC voltage is varying from 10V to 30V. Figure 6.22 and Figure 6.23 show the measured reference current (I_{ref1} and I_{ref2}) variations over temperature from 25°C to 200°C. The maximum reference voltage variation of I_{ref1} and I_{ref2} is less than 1.5 μ A and 2.5 μ A, respectively, from 25°C to 200°C. The current variation over temperature can be reduced if the measurement is performed from 25°C to 175°C. Figure 6.24 depicts the measured reference current variations over temperature when the input voltage is fixed at 12V.

Figure 6.25 illustrates the measured reference current variations over input supply voltage when the temperature is 200°C. Figure 6.26 illustrates the measured reference current variations over the drain-to-source voltage (V_{DS}) when the temperature is 25°C. In the SOI process, the channel length modulation effect is superior to that of the bulk CMOS process [98]. Figure 6.26 shows approximately 6% current variations over V_{DS} from 0.5 V to 2 V.

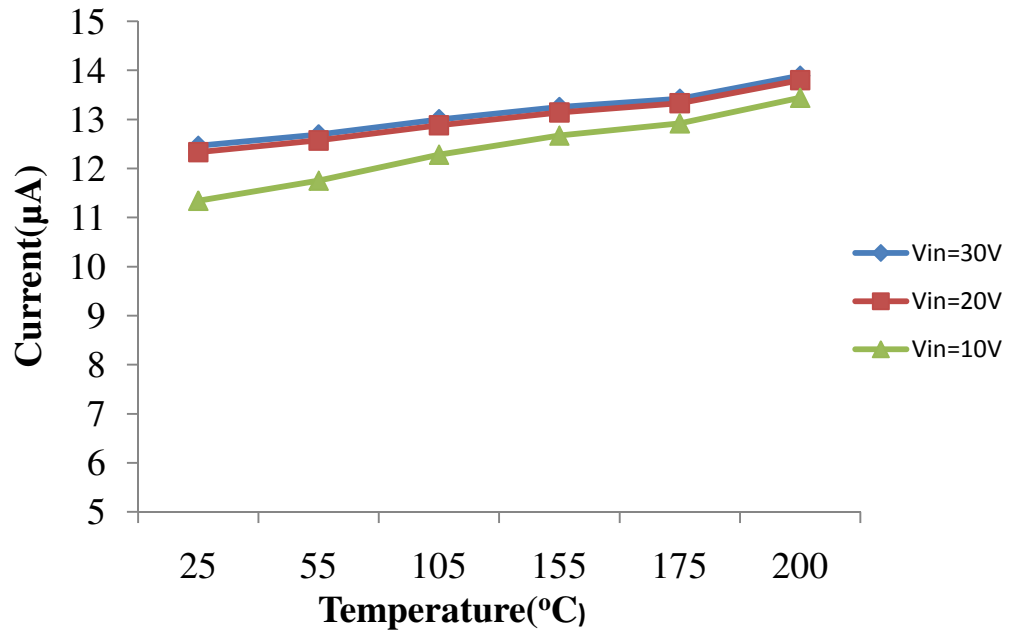


Figure 6.22 Measured current reference (I_{ref1}) over temperature

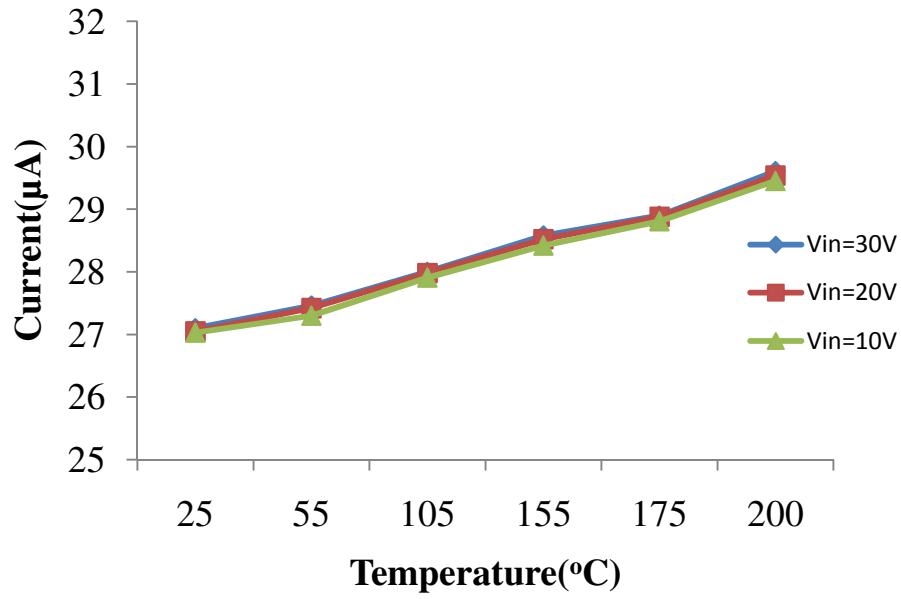


Figure 6.23 Measured current reference (I_{ref2}) over temperature

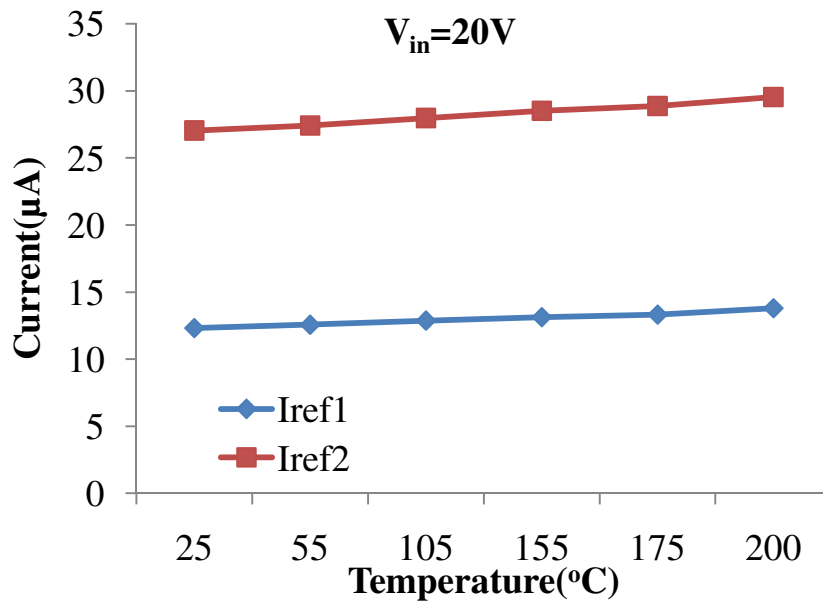


Figure 6.24 Measured current reference (I_{ref1} and I_{ref2}) over temperature

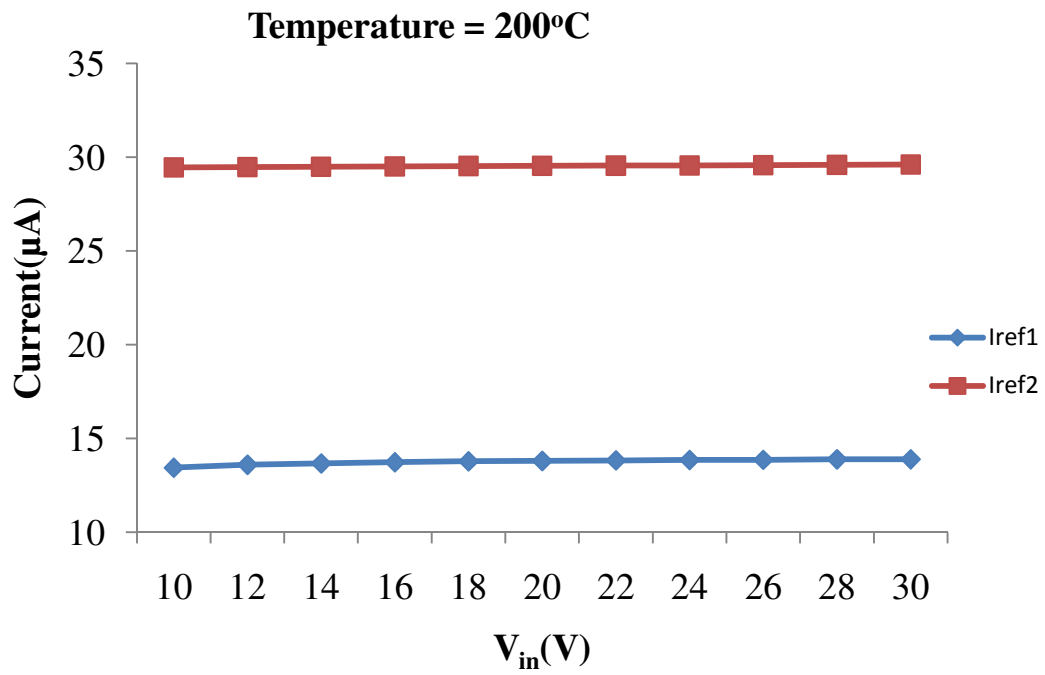


Figure 6.25 Measured current reference (I_{ref1} and I_{ref2}) over supply voltage

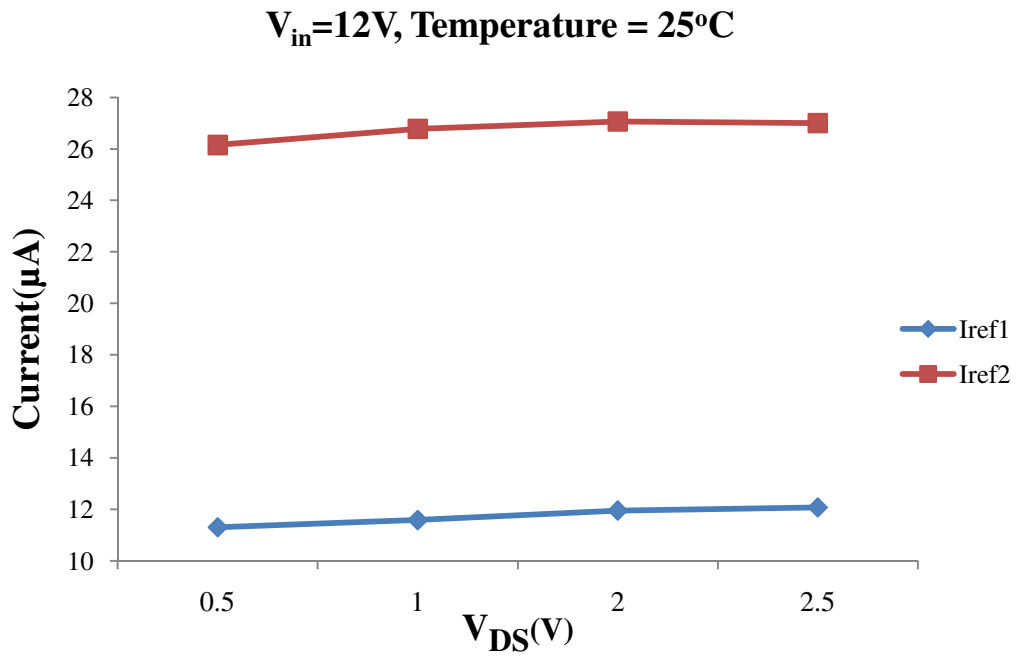


Figure 6.26 Measured current reference (I_{ref1} and I_{ref2}) variation over V_{DS}

6.3 Performance Summary

Table 6.3 summarizes the measurement results of the high-temperature linear voltage regulator. The best load regulation performance is obtained at temperatures below 105°C. The load regulation degrades significantly at temperature beyond 175°C. At elevated temperatures the mobility of MOSFET decreases with temperature which causes the transconductance degradation and the reduction of DC open-loop gain of the OTA. The FOM1 (Figure of Merit) is computed by using the measured transient response time multiplies the ratio of quiescent current by maximum load current. Meanwhile, FOM2 is utilized here to remove the process dependence of FOM1 [29].

Figure 6.27 and Figure 6.28 show the FOM1 and FOM2 of the high temperature linear voltage regulator compared with other works reported in literatures. The lower FOM1 and FOM2 represent the better regulator performance. Equation (2.2) defines the FOM1 for evaluating the performance of linear voltage regulator. The measured transient response time, 150 ns, is utilized to compute the FOM1 and FOM2. The FOM1 based on measurement result is 0.45 ns and it can be improved by increasing maximum load current or reduced quiescent current consumption.

As shown in Figure 6.27 and 6.28, the FOM1 of this work ranks in the top 40% of reviewed literatures, and ranks in top 25% when solely compared in terms of the transient response time. Among of the reviewed literatures, only this work has been designed and fabricated in BCD-on-SOI process technology, and tested up to 200°C.

Table 6.3 Summary of the performance of the regulator

Parameter (test condition)	Measured value
V_{in}	10 V ~ 30 V
$I_q (V_{in} = 12V)$	633 μA @ 200°C
I_{Load_max}	181 mA @ 25°C
C_{out}	10 μF , 25 μF
ESR of C_{out}	0.6 Ω ~ 1 Ω
Testing Temperature	25°C~200°C
$V_{out}(V_{in} = 12 V)$	5.328 V@ 200°C
Transient voltage variation ($\Delta I_{Load} = 50mA, V_{in} = 12V$)	≤ 200 mV @ 25°C ≤ 1 V (long wire)@ 200°C
Transient response time ($\Delta I_{Load} = 50mA, V_{in} = 12 V$)	≤ 150 ns @ 200°C
Load Regulation ($I_{Load} = 12mA, V_{in} = 12 V$) ($I_{Load} = 188mA, V_{in} = 15 V$)	≤ 1 mV @ 25°C(long wire) 15 mV @ 200°C(long wire) ≈ 100 mV @ 25°C(long wire)
Line Regulation ($I_{Load} = 12mA, V_{in} = 12 V \sim 30 V$) ($I_{Load} = 12mA, V_{in} = 20V \sim 30V$)	≈ 3.83 mV/V@ 200°C(long wire) ≈ 0.7 mV/V @ 200°C(long wire)
FOM1	0.45 ns @200°C
FOM2	2.25 @200°C
Current Reference ($V_{in} = 20 V$) ($V_{in} = 20V$)	$I_{ref1} \approx 7.7\%$ @25°C~175°C $I_{ref2} \approx 6.6\%$ @25°C~175°C
Quiescent Current Variations ($V_{in} = 20 V$) ($V_{in} = 30V$)	$\approx 0.6\%$, 4 μA @25°C~200°C $\approx 1.45\%$ 10 μA @25°C~175°C

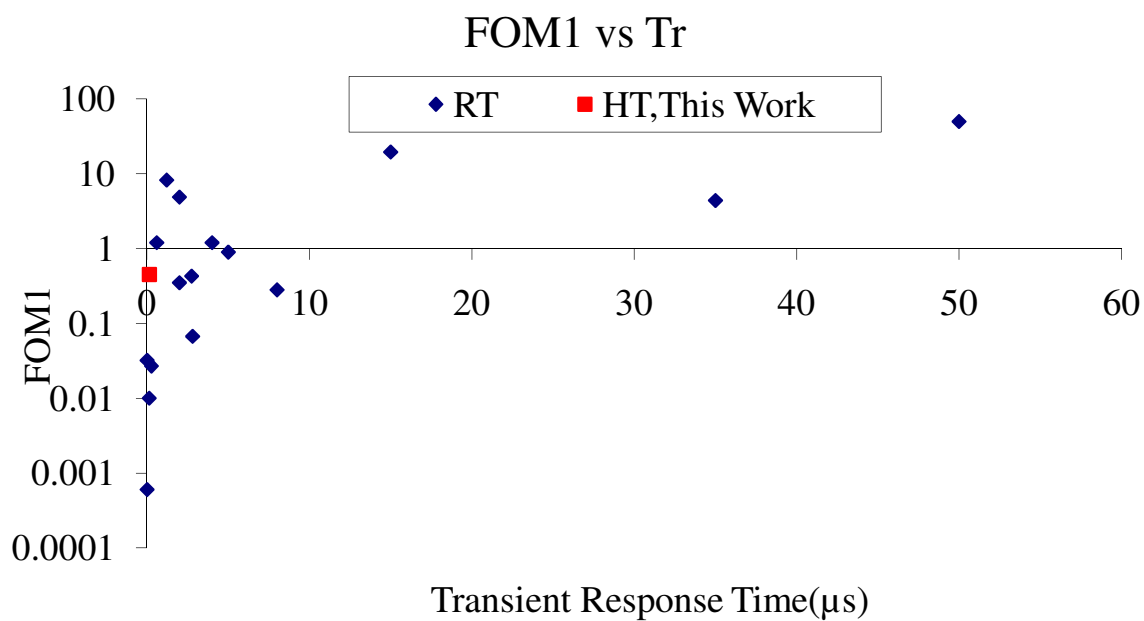


Figure 6.27 Measured FOM1 versus transient response time

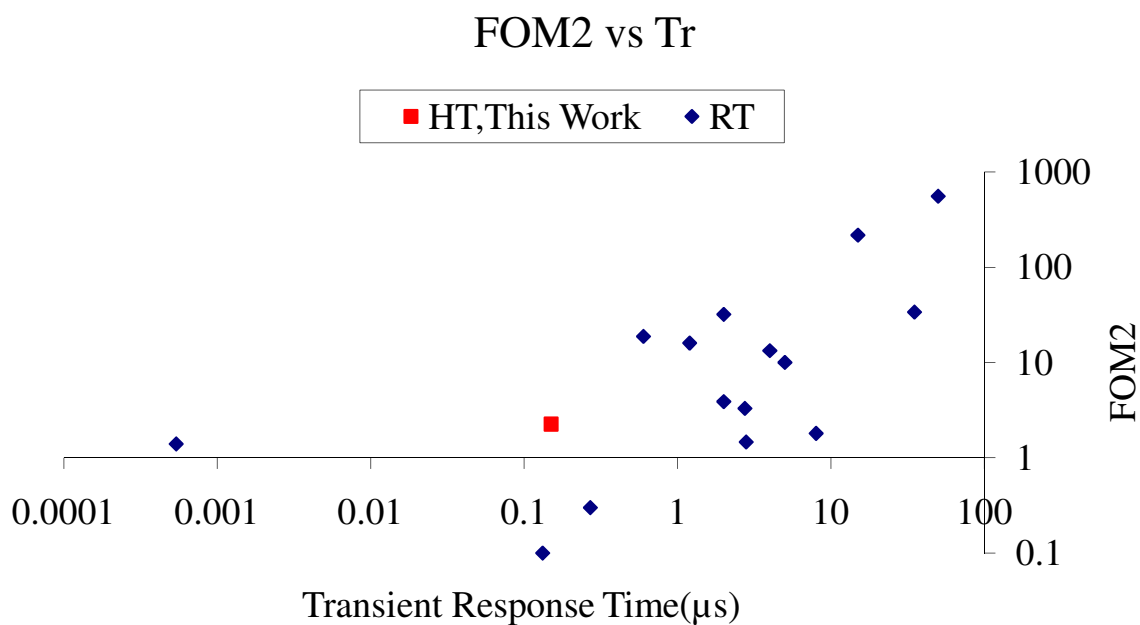


Figure 6.28 Measured FOM2 versus transient response time

CHAPTER 7

Conclusion and Future Works

The prototype implementation and measurement result of high temperature linear regulator is presented in previous chapter. This chapter concludes the research of the high temperature linear voltage regulator in BCD-on-SOI process technology. The conclusion of this work is drawn in Section 7.1. In Section 7.2, the list of future works and recommendations are introduced.

7.1 Conclusion

A high-temperature and high-voltage linear voltage regulator chip has been designed, fabricated and tested. A detailed description of the high-temperature design techniques and the implementation of the high-temperature, high-voltage linear voltage regulators realized in BCD-on-SOI process are presented in this work. This high-temperature linear voltage regulator provides a 5.3 V rail voltage to the low-side buffer of the gate driver circuit [19]. It consumes a total of 0.63 mA quiescent current during zero load current condition at 200°C, which is much lower compared to the commercial available SOI process based high-temperature linear voltage regulators. The low quiescent current can improve the efficiencies of both the regulator and the gate driver.

The pole swap technique proposed in this work can extend the range of the system stability to four decades of the load current (tens of μA to 200 mA) variations. This is particularly important in this research since the worst case load current profile is an impulse current waveform which comes from the switching “on” transition of the low-side buffer of the

gate driver. The peak-to-peak value of this current impulse may reach 200 mA in only 10's ns. In addition, the proposed pole swap technique is CMOS compatible and thus can be implemented in any CMOS processes.

This voltage regulator circuit can be integrated with the gate driver ICs that are required inside the power converter modules of a HEV. The voltage regulator can also be utilized in other high-temperature electronics (i.e. sensors, data converters, and oscillators) where typical bulk-CMOS regulators cannot provide regulated output voltage beyond 125°C.

Figure 6.9 shows the measurement result of the quiescent current of the regulator. From this figure it is evident that the quiescent current consumption varies by less than 2% over the temperature range of 25°C to 200°C. The temperature stable current reference circuit helps stabilize the quiescent current consumption, hence, the power efficiency of the regulator is independent of temperature.

A high-temperature folded cascade operational transconductance amplifier chip has been designed and fabricated as well. A detail description of the high temperature design techniques and the implementation of the high temperature/voltage folded cascade OTA in BCD-on-SOI process are presented in Chapter 3. The amplifier consumes a total of 95 μ A bias current at 175°C and the lower bias current can reduce the power dissipation at elevated temperature. In addition, a temperature stable current reference stabilizes the gain of the OTA across temperature. This folded cascode amplifier is utilized as an error amplifier of a high temperature linear voltage regulator. The amplifier can also be utilized in other high temperature electronics (such as sensors, data converters, etc.) whereas a typical bulk-CMOS amplifier cannot provide the circuit performance as that achievable in SOI [50] beyond 125°C. The AC measurement result of

the folded cascode amplifier is presented in the Appendix. The simulation and the measurement results show excellent agreement. The amplifier is tested up to 200°C with 3.65 MHz bandwidth.

The SOI process technology offers several advantages over bulk-CMOS process which include latch-up immunity, higher noise immunity, reduced short channel effect, reduced parasitic capacitance, and reduced leakage current.[98, 99] These advantages make SOI based integrated circuit become attractive in high-temperature, high-voltage, low-power and automotive applications.

7.2 Future Works

The proposed SOI based high temperature linear voltage regulator chips are successfully tested up to 200°C, there are several improvements which can be recommended for future research works. The first recommendation is to implement the on-chip protection circuits; although the voltage and the current compliance of measurement instrument can be set during the measurement, the on-chip protection circuits will prevent the regulator chips from man-made catastrophic damage. Therefore, the reliability and life of regulator chip can be extended.

7.2.1. Protection Circuit

The on-chip over-current protection can limit the regulator from overloading condition. An on-chip protection circuit can improve the reliability of the regulator as well. The safe operating area (SOA) is utilized to design the over-current protection circuit [9, 11, 95, 96]. The on-chip over-current protection circuit can be classified into fixed over-current protection and fold-back over-current protection [11]. The high temperature effect occurs to the devices (i.e. diode, MOSFET, BJT, resistor...etc.) may result in design challenge and complexity.

7.2.2. Low-Power

The SOI offers reduced leakage current, reduced parasitic capacitance and higher transconductance than bulk CMOS process. These advantages make SOI process technology an ideal candidate for low-power, low quiescent current design [98, 99]. The quiescent current of the regulator can be further reduced by applying inversion coefficient (g_m/I_D) methodology. The trade-off between speed and power consumption can be optimized. The total quiescent current consumption of regulator core could be reduced down to 100 μ A by biasing analog circuits in the border of moderate inversion and weak inversion.

7.2.3. Current and Voltage Reference

The current and voltage references are the core of an analog integrated circuit, especially for the high-temperature applications. The precision voltage and current references are desired to provide improved performance. The current and voltage reference needs to be independent of the process variations. The on-chip resistor is utilized in this work which tends to create variations due to process and mismatch. The performance of current and voltage reference circuit can be improved by either adapting an innovative design topology without utilizing on-chip resistor or with on-chip resistor trimming.

References [84, 86, 87] proposed a CMOS based bang-gap voltage reference circuit, [87] utilized a transimpedance amplifier to improve the precision of reference voltage. An amplifier can be inserted into a conventional band-gap voltage reference for minimizing the reference voltage variation over temperature.

7.2.4. PCB Layout

The better PCB layout will improve the performance of line regulation, load regulation, transient voltage droop and facilitate the measurement setup. The shorter trace will reduce the parasitic effect.

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Appendix

The operational transconductance amplifier (OTA) is the most versatile analog integrated circuit component in analog circuitry. The measurement result of proposed operational transconductance amplifier is presented in the appendix.

The high temperature open loop gain measurement result and unity-gain bandwidth measurement results are compared with the simulation result. Literature [100,101] introduced the measurement techniques of operational transconductance amplifier.

The temperature testing is performed at temperature of 25°C, 55°C, 105°C, 155°C, 175°C and 200°C. The input signal is a sine wave with 4 V DC voltages, 20 mV AC amplitude. The frequency of input signal is varied from 100 Hz, 300 Hz, 1 KHz, 5 KHz and 10 KHz.

The load capacitance loaded the proposed amplifier is approximately 50 pF, 100 pF, 250 pF and 1050 pF.

Figure A.1 and Figure A.2 illustrated the measured open loop gain at room temperature and 200°C, respectively. The load capacitance is 1050 pF.

Figure A.3 depicted the measured open loop gain compared with simulation result as function of temperature. The measured result shows excellent agreement with simulation result. The -20dB/dec roll-off represents the single pole system. Figure A. 4 shows the comparison of measured unity-gain bandwidth and simulated unity-gain bandwidth as function of temperature. The unity gain bandwidth of proposed operational transconductance amplifier is express as

$$f_{un} = \frac{g_{m_in}}{2\pi C_L}$$

Where g_{m_in} represents the transconductance of input pair of OTA; C_L is the load capacitance.

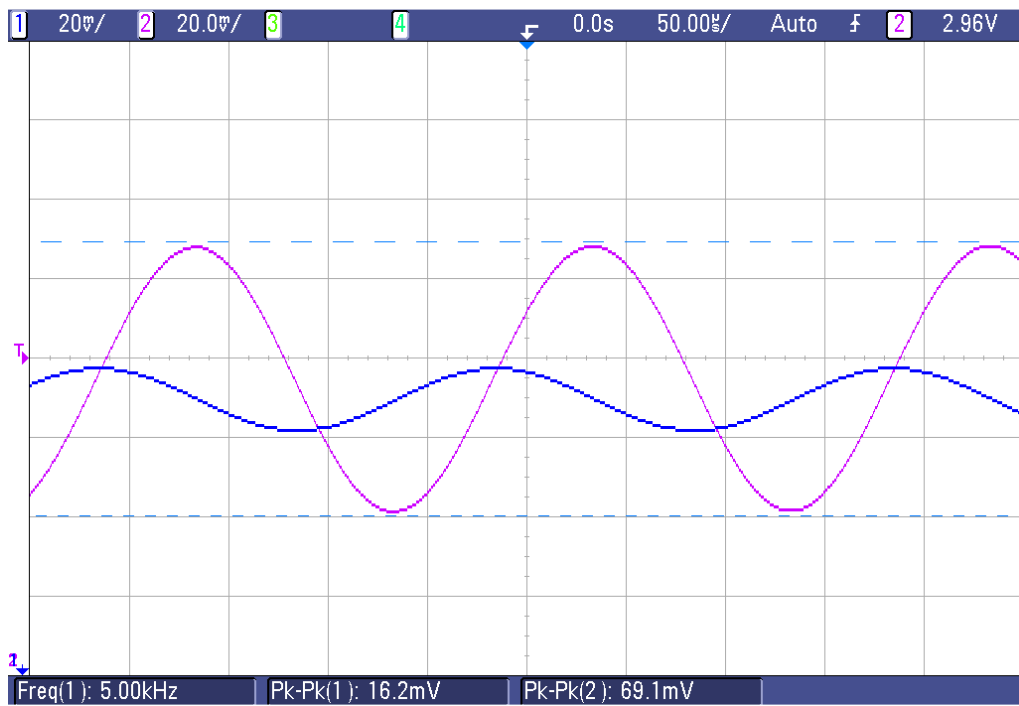


Figure A.1 The measured open loop gain at room temperature, $f_{in} = 5$ KHz.

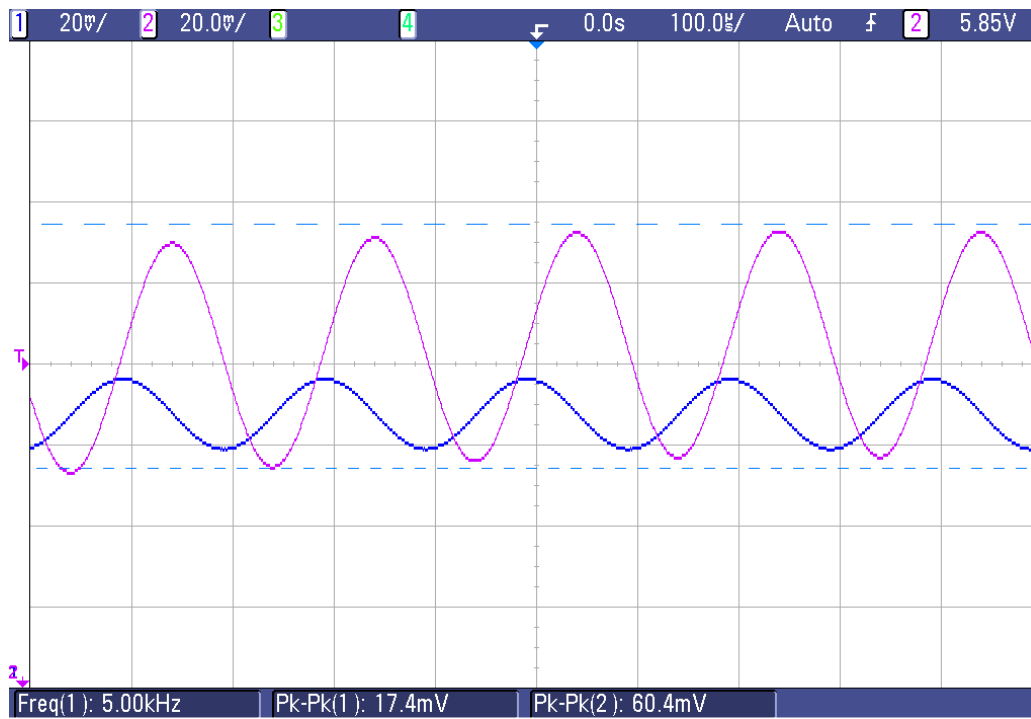


Figure A.2 The measured open loop gain at 200°C, $f_{in} = 5$ KHz.

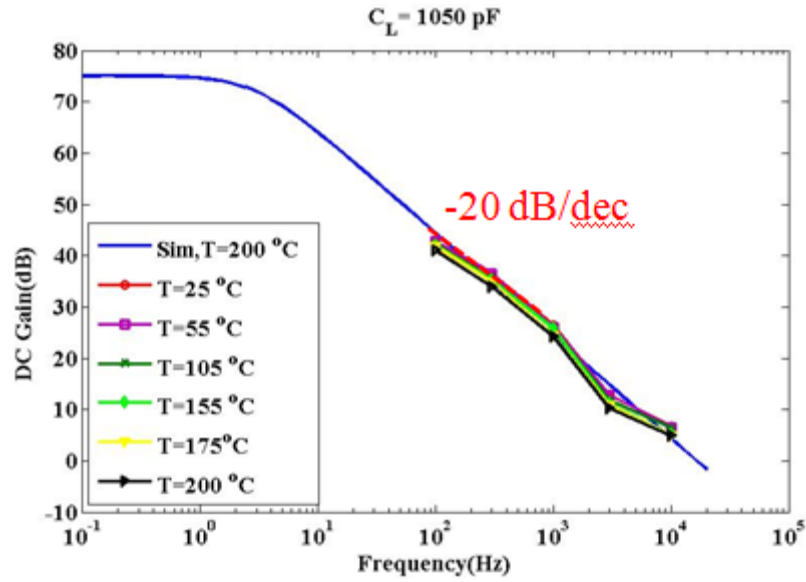


Figure A.3 The measured open loop gain compared with simulation result as function of temperature.

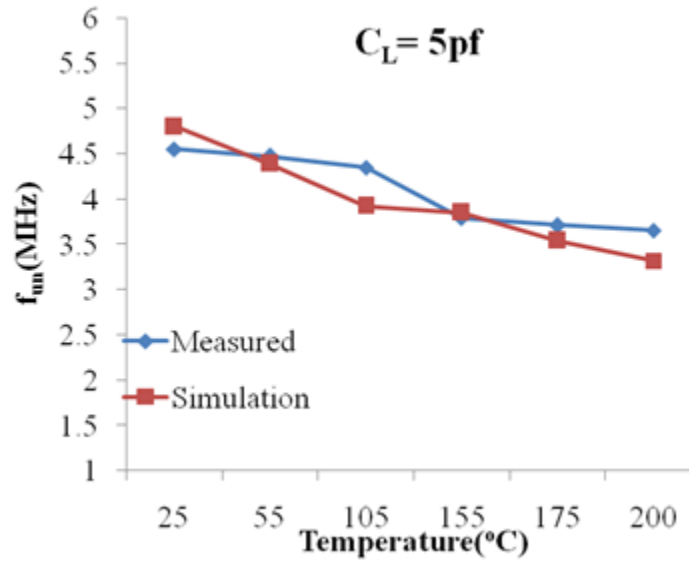


Figure A.4 The measured/simulation Unity-Gain bandwidth as function of temperature.

Table A.1 The summary of OTA's performance.

Temperature(°C)	25	55	105	155	175	200
f_{un} (KHz) @ C_L (1050 pF)	21.7	21.3	20.7	18	17.7	17.4
f_{un} (MHz) @ C_L (5 pF)	4.55	4.47	4.35	3.79	3.71	3.65
Gain (dB) @100 Hz, Measured	42.52	42.76	42.19	42.08	41.76	41
Gain (dB) @100Hz, Simulation	46.34	45.81	44.97	44.1	43.88	43.49
Gain (dB) @DC Simulation	75	74.8	74.4	73.8	73.64	73.3

Table A.1 summarized the performance of the proposed OTA. From this table, the unity-gain bandwidth is 3.65 MHz at temperature of 200°C when the load capacitance is 5pF. The bandwidth can be further increased if the OTA is driving a smaller capacitance. The Figure A. 5 shows unity-gain frequency as function of load capacitance at room temperature. The unity-gain bandwidth can be extended to approximately 9 MHz if the load capacitance of the OTA is at 2 pF range.

The Figure A.6 shows the measured phase margin of the OTA at the room temperature. Literature [62, 89, 101] indicated the percentage of the overshoot can be used to estimate the phase margin. From the Figure A. 6, the measured phase margin of OTA is about 75°.

The Figure A. 7 depicts the measured slew rate of the OTA at the 200°C. When the OTA is loaded with 1 nF capacitor, the measured slew rate at room temperature is approximately 13.5 V/ms. On the other hand, The simulation result is about 15 V/ms.

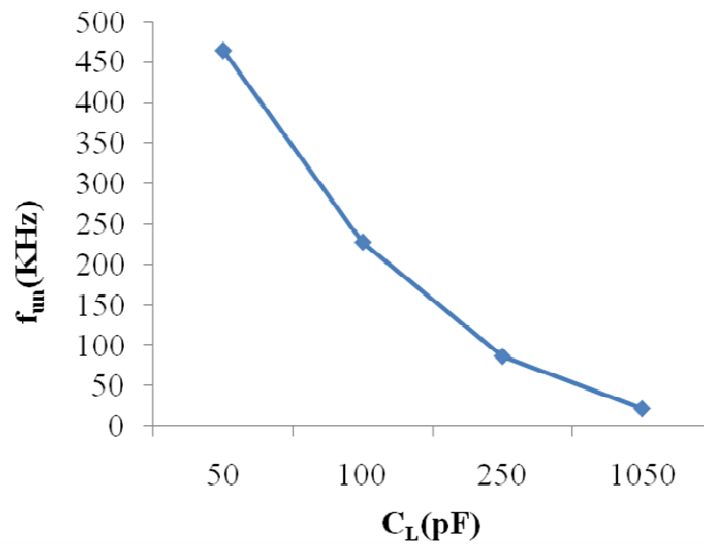


Figure A.5 The measured unity-gain frequency as function of load capacitance.

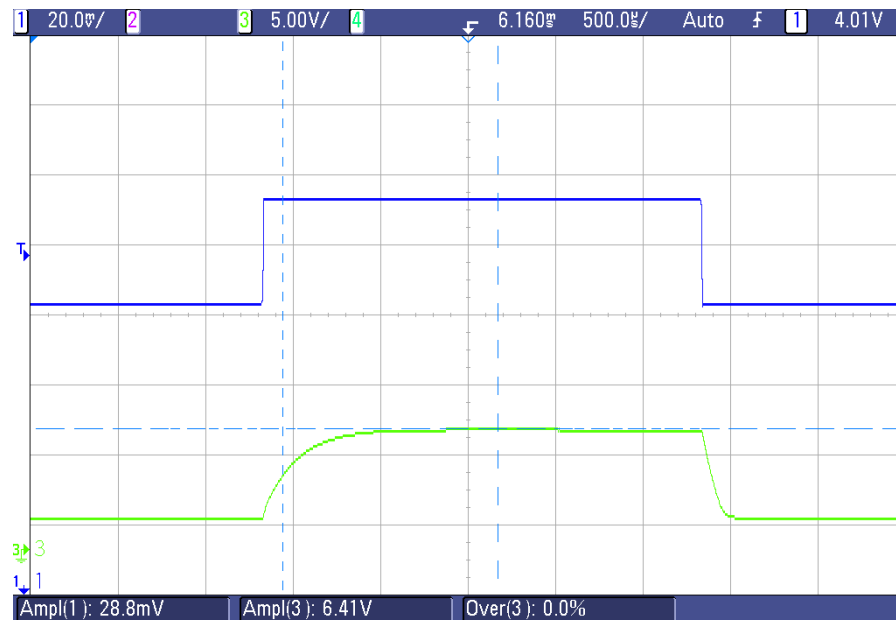


Figure A.6 The measured Phase Margin at room temperature.

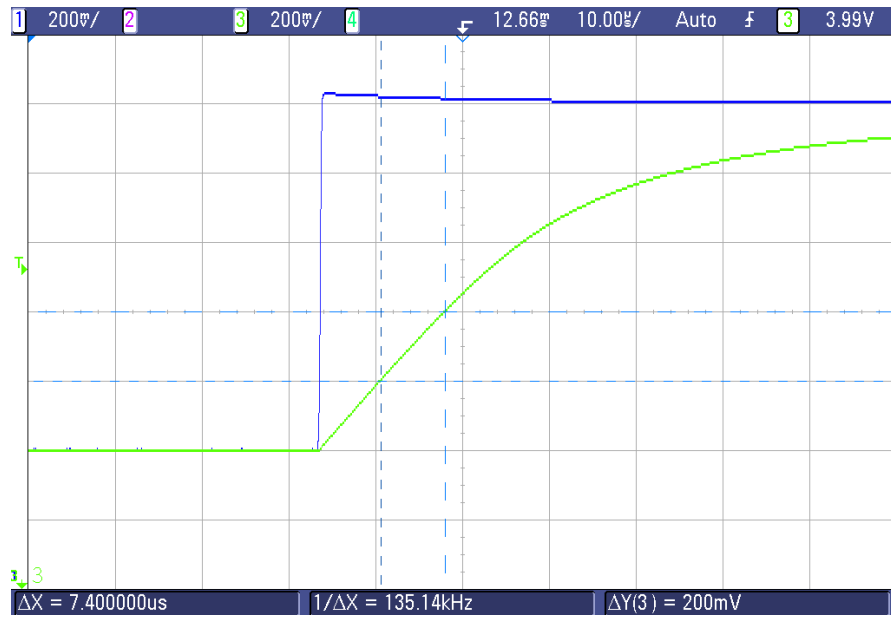


Figure A.7 The measured slew rate at 200°C.

VITA

Chiahung Su was born in Taichung, Taiwan in 1978. He received his B.S. degree in Electronics Engineering from National Taipei University of Technology in 2000, M.S. degree in Electrical Engineering from University of Texas at Arlington in 2004 and Ph.D. degree in Electrical Engineering from University of Tennessee at Knoxville in August, 2010. His research interest is analog IC design in CMOS, SOI and novel fabrication process. His dream job is either designing analog IC circuits with some experienced analog IC designers or doing research in analog IC design with a group of hardworking and smart students. In addition, he can speak Taiwanese, Chinese, English and a little bit of Japanese, and he always wants to keep learning Japanese as second foreign language.

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