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A/D Converters Architectures based on Cascaded Incremental and Cyclic Structures

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IMPRIMATUR POUR LA THESE

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Abstract

Characteristics of converters are extremely wide from Gigasamples to a few samples per second for bandwidth and resolution variation from a few bits to more than 20 bits. In the field of high resolution, converters architecture are mostly based on oversampling converters. Delta-sigma converter is a common implementation of this architecture. However, in certain applications, this converter is not very-well suited. In instrumentation and measurements, the continuously operation, the large offset and inaccurate gain of the $\Delta - \Sigma$ does not satisfy the specifications. The incremental converter, who is also based on $\Delta - \Sigma$ architecture, but work in a transient mode is more adapted. However this converter's drawback is the large time required to digitize a sample.

This thesis aims at studying a new ADC architecture based on an incremental converter, keeping the high precision characteristics and offering a faster conversion.

The cascading of an incremental converter with a cyclic converter is presented. The converter is used in incremental mode and produces a residual quantization error. This voltage is then passed to a faster cyclic converter. The conversion still benefit the high precision of incremental conversion while required conversion time is reduced. Another advantage of this new architecture is that both converters share the same hardware, which leads to a very compact converter. The introduced general architecture is flexible: the resolution solved by each conversion is not fixed, thus it is capable to optimize the tradeoff between conversion accuracy and conversion time. Another presented architecture for reducing the conversion time is to use a second-order incremental converter cascaded by a cyclic one.

A switched-capacitor implementation is proposed. The developed archi-

tecture is validated through the realization of two integrated circuits in a CMOS 0.18 μm technology. A circuit with first order only and another with first and second order. A 16-bit ADC with a sampling frequency of 500 Hz is realized. The maximum signal-to-noise ration is 84.8 dB, which is equivalent to 13.8 effective number of bits. The power consumption is 150 μW under 1.65 V and the active area is 0.1 mm^2. Compared to other solutions, the results are relatively efficient and competitive in the field of high resolution, with the benefit of a small circuit.

Keywords

Analog-digital conversion (ADC), incremental, cyclic, switched-capacitor circuit (SC), integrated circuit, CMOS.

Résumé

Les caractéristiques des convertisseurs analogique-numérique sont extrêmement vastes, du Giga-échantillons à quelques échantillons par seconde et une résolutions de quelques bits à plus de 20 bits. Dans le domaine des hautes résolutions, la plupart des architectures sont basées sur les convertisseur à suréchantillonnage. Les convertisseurs delta-sigma en sont la meilleure illustration. Le fait de suréchantillonner permet de réduire la sensibilité aux composant analogique et d'atteindre de grandes résolutions. Toutefois, dans certaines applications, ce convertisseur n'est pas approprié. Par exemple dans les système de mesure et instrumentation, le mode de conversion continu, un grand offset et un gain imprécis inhérant aux $\Delta - \Sigma$, ne satisfont pas aux spécifications. Le convertisseur incrémental, qui est aussi basé sur une architecture de type $\Delta - \Sigma$, mais fonctionnant en mode transitoire est mieux adapté. Cependant ce type de convertisseur nécessite un grand temps pour numériser un échantillon.

Ce travail de thèse a pour objectif l'étude d'une nouvelle architecture de conversion basée sur un convertisseur de type incrémental en gardant les caractérisiques de grande précision et présentant une plus grande rapidité.

La combinaison d'un convertisseur incrémental avec un convertisseur cyclique en cascade est presentée. Le convertisseur est utilisé en mode incrémental puis l'erreur residuelle à la sortie est échantillonée à nouveau par une conversion cyclique beaucoup plus rapide. Cette apporche permet de réduire le temps de conversion tout en conservant le bénéfice de la précision de l'incrémental. Un autre avantage de cette nouvelle architecture est que les deux convertisseurs utilisent le même *hardware*, menant ainsi à un convertisseur compact. L'architecture générale introduite est flexible, la résolution de chaque convertisseurs peut être ajustée

facilement permettant ainsi d'optimiser le compromis entre précision et temps requis pour une conversion. Une deuxième méthode pour réduire le temps de conversion et d'utiliser un convertisseur incrémental du second ordre combiné lui aussi avec un convertisseur cyclique.

Une implémentation à capacités commutées est proposée. L'architecture developée a été validée avec succès d'un point de vue théorique et au moyen de simulations. Sur la base de cette étude, deux circuits intégrés ont été implementés dans une technologie CMOS 0.18 μm. Un circuit avec structure du premier ordre uniquement et un autre avec premier et deuxième ordre. La réalisation pratique a permis de montrer le fonctionnement de cette nouvelle architecture. Un convertisseur 16-bit du premier ordre a été realisé avec une fréquence d'échantillonnage de 500 Hz. Un rapport signal sur bruit maximal a été mesure à 84.8 dB, équivalent à 13.8 bits avec une consommation de 150 μW pour une tension d'alimentation de 1.65V et une surface active de 0.1 mm^2. Les résultats montrent un grand potentiel pour ce type d'architecture pour des hautes resolution, tant au niveau basse consommation que surface réduite.

Mots-clés

Conversion analogique numérique (CAN), incrémental, cyclique, circuit à capacités commutées, CMOS.

Contents

Chapter 1

Introduction

The complexity of integrated electronic circuits being designed nowadays is continuously increasing as advances in process technology make it possible to create more and more complex system with higher processing ability, leading to the notion of SoC (System on Chip). Most parts of these SoC's are completely digital rather than analog blocks. Digital circuits are more economical, noise has much less influence on the quality of the signal, are flexible and easier to reconfigure. But since the real world is an analog place, SoC designs must include at least some analog interfacing functions. Analog-to-digital converter (ADC) are the link between these two worlds.

1.1 Analog to Digital Conversion

Figure 1.1 gives the performances that ADCs must achieve for typical recent applications [1]. In instrumentation, measurement and sensor applications, ADCs with very high resolution are required (16 to 20 bits). Typical applications include weight scales, smart humidity, pressure or temperature sensors, digital voltmeters or seismic sensors. These converters also require high absolute accuracy, high linearity and very low

[1] http://www.itrs.net

offset. For battery-powered sensors, power consumption must be minimized. On the other hand, the frequency bandwidth of the input signal is generally low.

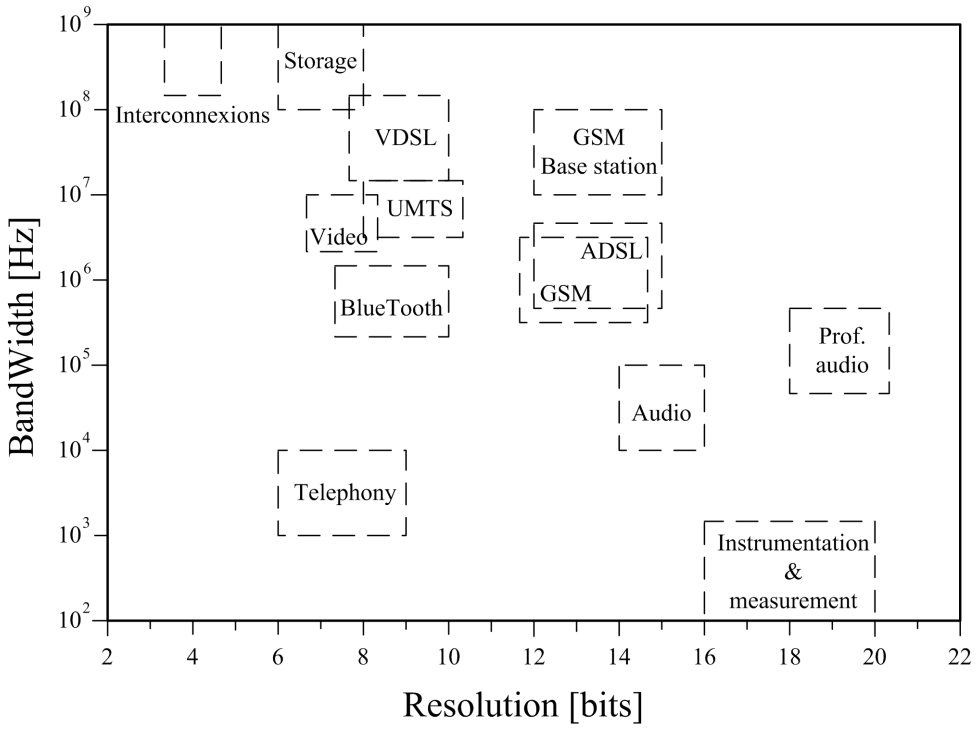

Figure 1.1 : Performances (resolution and bandwidth) needed for recently applications.

For high-resolution, Delta-Sigma is the most widely used converter, but nevertheless gain control and gain offset are not easy satisfied with this conversion principle. In telecommunication or audio applications, the signal waveform needs to be digitized continuously, and the spectral behavior of the signal is the most important parameter therefore Delta-Sigma are well suited for these applications.

In most sensor applications, however the goal is to digitize individual samples or the average value of a noisy DC signal. Incremental converter are well suited for these requirements. They are also based on the Delta-Sigma architecture, but there are significant differences

- the converter does not operate continuously.
- both analog and digital integrators are reset after each conversion
- the decimating filter following the modulator can be made much simpler

Nevertheless, the biggest drawback of the incremental converter is that it is very slow. A complete conversion needs to operate through 2^n cycles to achieve a n-bit resolution.

1.2 ADC parameters

Independently from the structure of the ADC, we can define a set of parameters that can specify the functional characteristics of a converter. These specifications are used to evaluate the performances of an ADC.

1.2.1 General parameters

The transfer function of an ADC represents the relationship between every input sample and the corresponding output code. The Full-Scale (FS) represents the difference between the minimum and maximum value of the input signal. For an ideal case, the transfer function is a uniform staircase function, as shown in Figure 1.2 for an ideal 3-bit linear converter.

The resolution n represents the number of bit of the digital output and the number of quantization levels of the ADC is directly related to this parameter (2^n levels). In the previous figure, the ADC has a 3-bit resolution, corresponding to 8 levels.

The width of each step is called the quantification step q, corresponding to the smallest difference of analog voltage between two suc-

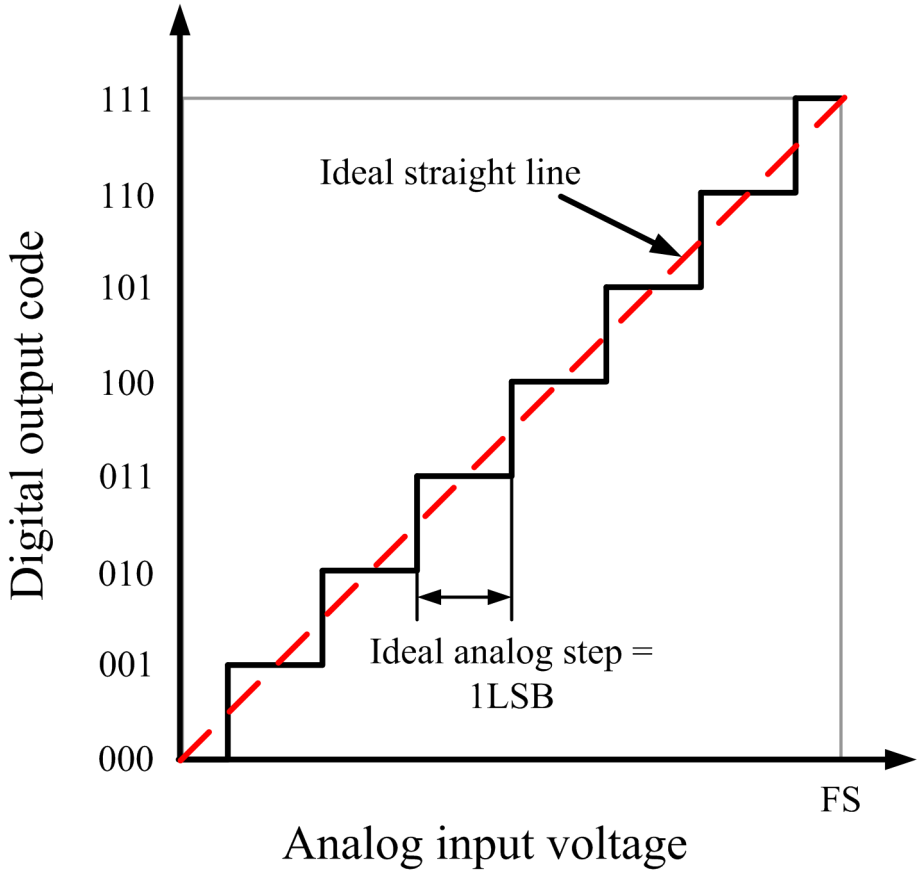

Figure 1.2 : Ideal transfer function of a 3-bit ADC.

cessive codes. It is generally expressed in LSB (Least Significant Bit). In an ideal case, the quantization step is constant for all codes:

$$q = FS/2^n = 1\,LSB \tag{1.1}$$

The ideal straight line of an ADC is crossing all the mid-code points of the ideal transfer function while the real straight line is performed by a linear regression on the mid-code points of the real transfer function.

Quantization error

The quantization error is the natural error that occurs when a signal is digitized. Figure 1.3 shows the evolution of this error, expressed in LSB, in function of the analog input applied to the converter.

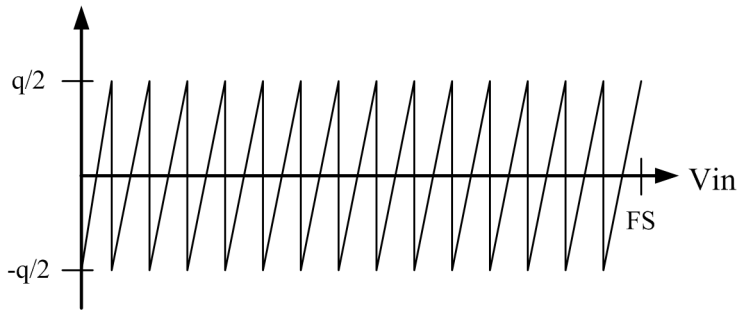

Figure 1.3 : Quantization noise.

A quantization noise can be associated with this error. The estimation of the true RMS value of this noise is made under the assumption that its error probability *p(q)* is uniform within a quantification interval of *(-q/2; q/2)*. In this interval: *p(x)=1/q*. Thus the power of the noise is:

$$P_q = \int_{-q/2}^{q/2} x^2 \cdot p(x)dx = \frac{q^2}{12} \tag{1.2}$$

and the equivalent RMS noise:

$$B_q = \sqrt{P_q} = \frac{q}{\sqrt{12}} = \frac{1LSB}{\sqrt{12}} \tag{1.3}$$

This error is directly related to the quantization step and thus to the resolution of the converter.

1.2.2 Static parameters

Static parameters are directly related to the comparison of the ideal conversion characteristics with the measured one. This comparison includes offset, full-scale, gain and linearity errors.

Offset and gain error

The offset error of an ADC is the horizontal distance separating the ideal and the real straight line for the same output digital code. It is

generally expressed in input-referred LSB.

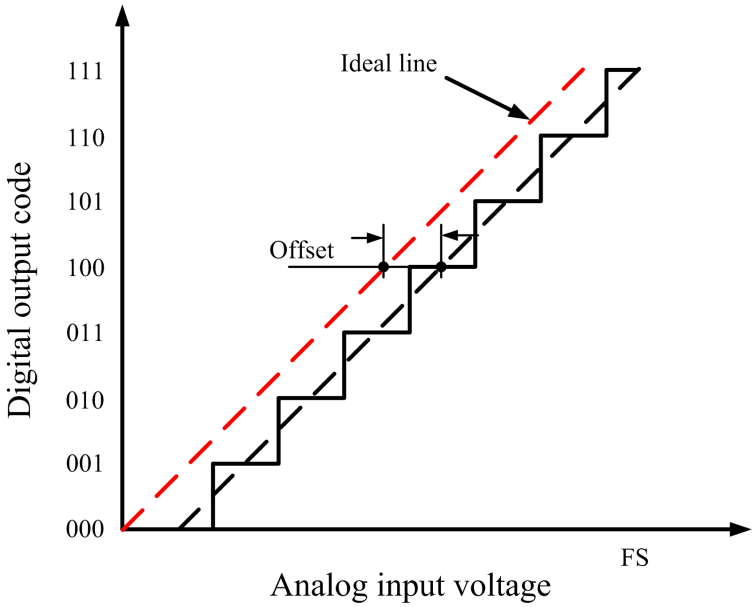

Figure 1.4 : Offset error.

The gain error of an ADC is the variation of the slope between the ideal and the real straight line. This error is dimensionless and is often expressed as a percentage.

Differential Non-linearity

The Differential Non-Linearity (DNL) can be defined as the difference between a real quantization step and the ideal quantization step. Each digital output code has its associated DNL value, expressed in LSB. If the absolute value of the DNL error is less than 1 LSB, the converter has no missing codes. The DNL can never be smaller than -1.

Integral Non-linearity

The Integral Non-Linearity (INL) error is the deviation of the mid-point codes from their ideal location on the real straight line. The INL can be obtained by the summation of the DNL errors.

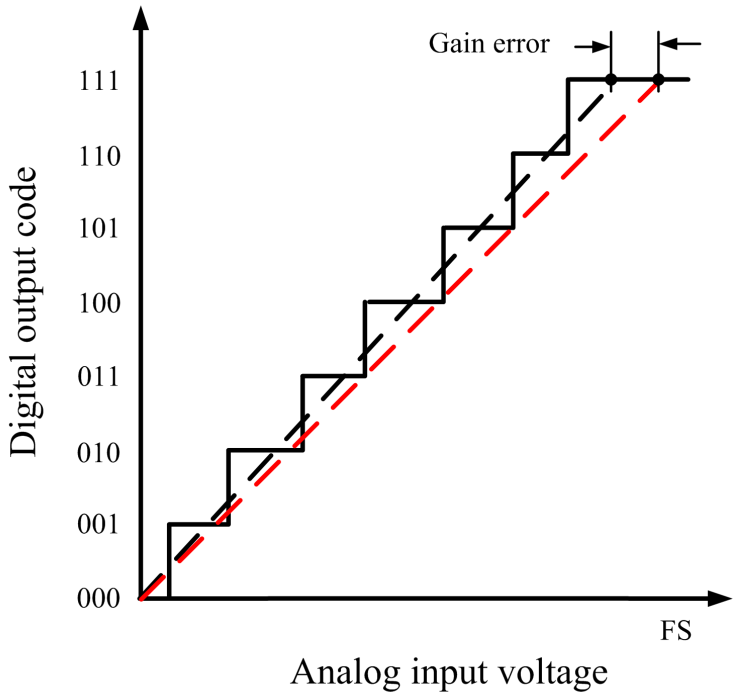

Figure 1.5 : Gain error.

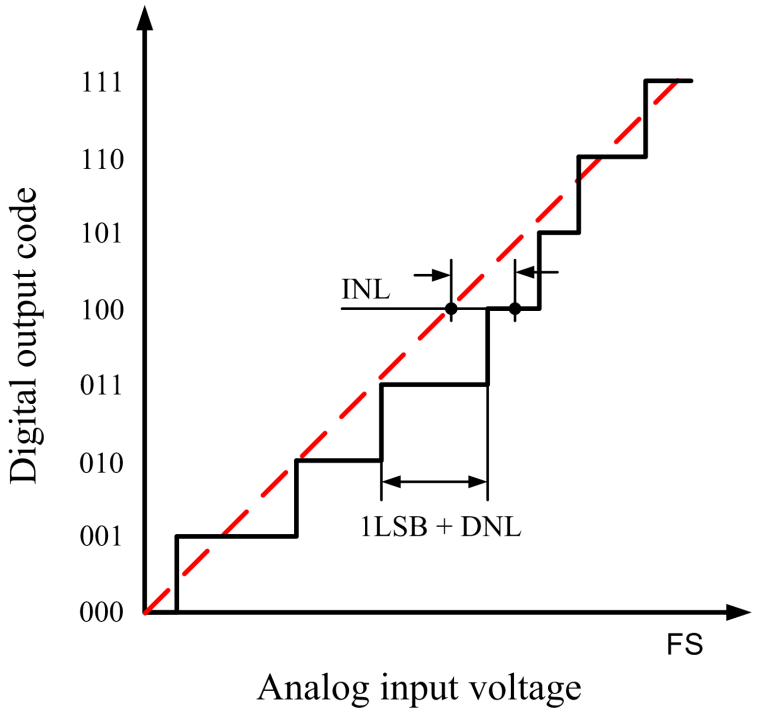

Figure 1.6 : INL and DNL errors.

1.2.3 Dynamic parameters

When an analog sine wave is applied to the ADC input, the converted digital signal can be analyzed using a Fast Fourier Transform (FFT). Dynamic parameters such as signal-to-noise ratio, harmonic distortion, can be determined using this method.

Signal-to-Noise Ratio

The Signal-to-Noise Ratio (SNR) represents the ratio between the power of the signal and the power of the noise. The noise includes both the quantization noise and circuit noise but it does not include any harmonics of the signal. Generally, this parameter is defined for a sinusoidal input with maximum amplitude with respect to the input range of the converter. The true RMS value of a full-scale sinus signal is given by:

$$A_{RMS} = \frac{FS}{2\sqrt{2}} = \frac{2^{n-1}q}{\sqrt{2}} \tag{1.4}$$

For a perfect ADC, the noise is only due to quantization noise. We can calculate the SNR expressed in dB as:

$$SNR_{dB} = 20\log\left(\frac{A_{RMS}}{B_q}\right) = 20\log\left(\sqrt{\frac{3}{2}}\cdot 2^n\right) \tag{1.5}$$

and theoretically the maximum achievable SNR for an n-bit resolution is given by:

$$SNR = 6.02\cdot n + 1.76\ (dB) \tag{1.6}$$

Signal-to-Noise plus Distortion Ratio

The Signal-to-Noise plus Distortion Ratio (SNDR) is defined as the ratio between the power of the signal and the power of the noise plus harmonic distortion. In a real converter, all the the variations of the functional parameter (non-linearity, jitter, ...) contributes to the noise.

Total Harmonic Distortion

For a sinusoidal input of frequency f_{in}, the non-linearity of the converter generates harmonic frequency. The Total Harmonic Distortion (THD) allows to evaluate the amount of these harmonics. It represents the ratio between the sum of the amplitude H_k of harmonics of order k and the amplitude of the input signal.

$$THD = 20\log\left(\frac{\sqrt{\sum_{k>1} H_k^2}}{A(f_{in})}\right) \ (dB) \tag{1.7}$$

Effective Number of Bits

The Effective Number of Bits (ENOB) is defined as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \ (bit) \tag{1.8}$$

It considers the total noise (quantization and distortion) of the ADC as a quantization noise and then calculates the effective number of bits that this converter has.

Dynamic Range

The dynamic range is the value of the input signal at which the SNR (or SNDR) is 0 *dB*. This parameter is useful for some type of data converters that do not obtain their maximum SNR (or SNDR) when input signal amplitude is Full-Scale.

Jitter

The sampling of the analog input does not happen at the exact desired time. This uncertainty Δt_j on the sampling time, commonly called jitter, generates a conversion error ΔV.

1.3 State of the art in AD conversion

1.3.1 Structures

ADCs can be implemented by using a large variety of architectures. Each of them has their benefits and disadvantages. In the next two figures we can plot two of the principal tradeoffs that appear in ADCs. The first one is the conversion time. Flash and pipeline structures have a minimal conversion time independent of the resolution. On the other side, conversion time doubles with every bit increase in resolution for first-order incremental converter.

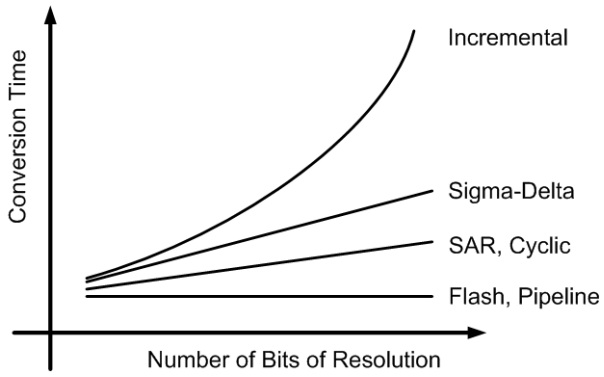

Figure 1.7 : Tradeoff between speed and resolution.

When we look at the circuit size in function of resolution, we get something totally different. Now for flash ADCs, the size of the chip increases exponentially with the resolution while for incremental the size will keep quite the same with the increase of the number of bit.

A selection of state-of-art ADC, based on publications of the Journal of Solid State Circuits (JSSC) in the years 1988-2008, is analyzed and their performances have been compared (cf. Annex A). The bandwidth of the converter is plotted in function of the effective number of bits (ENOB).

Families of ADCs are clearly observed. Each one of these architec-

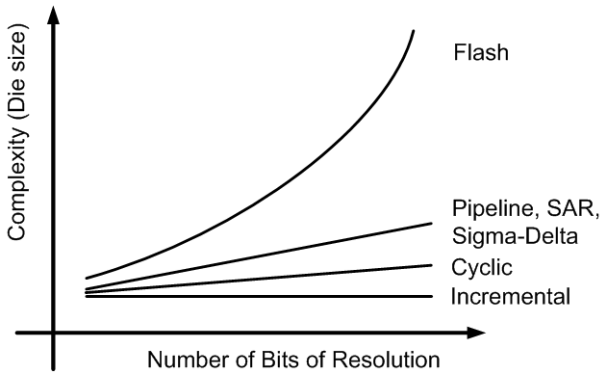

Figure 1.8 : Tradeoff between area and resolution.

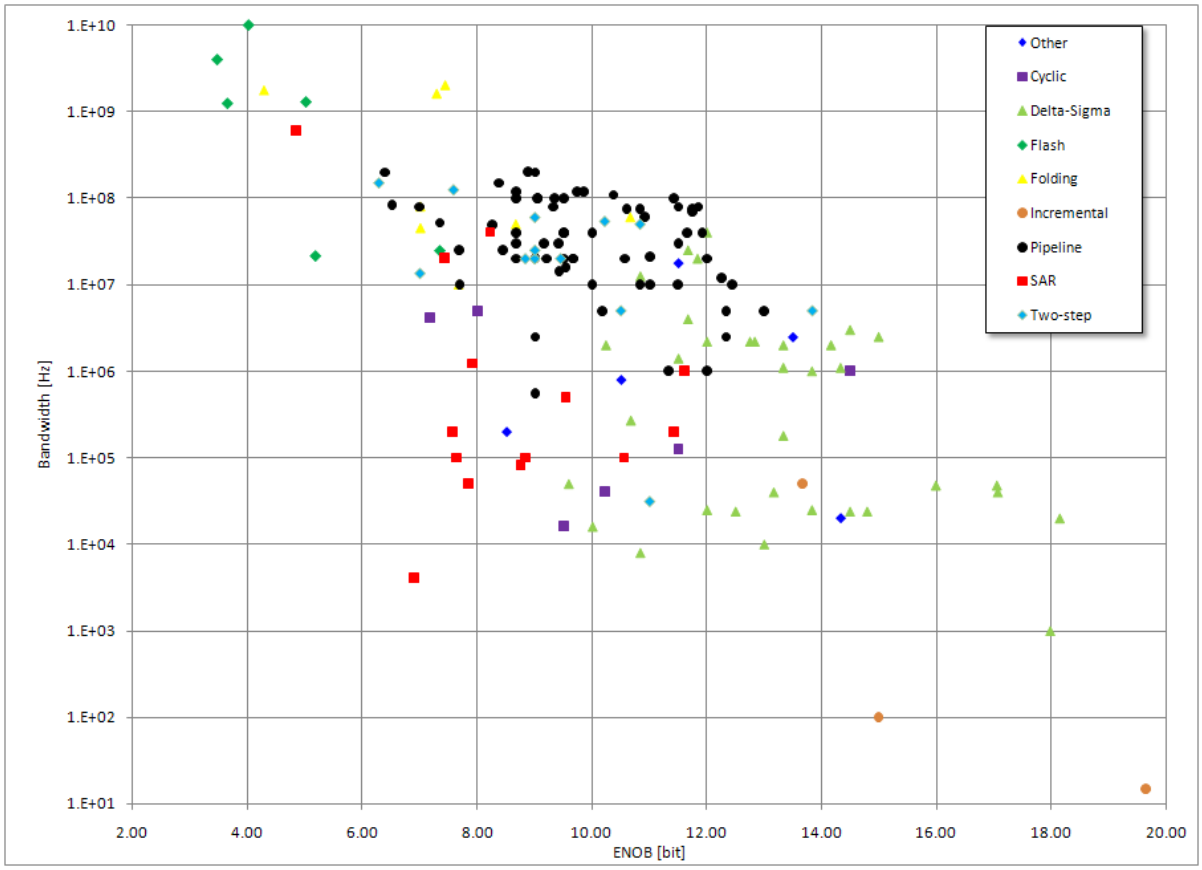

Figure 1.9 : Bandwidth versus ENOB.

tures uses a different method of operation which can be implemented efficiently for their optimum performance range.

Flash ADCs are the fastest ADC with speed up to 10 GS/s and resolution under 8 bits. They are just followed by folding structures that present quite the same characteristics. Pipeline ADC are present in a wide range of resolution (from 6 to 14 bits) and represent the fastest solution for these resolutions. Delta-Sigma covers the range of high resolution from 10 to 20 bits. Cyclic and SAR have a resolution between 6 and 12 bits but with a lower sampling rate than pipeline, however they demonstrate a great energy efficiency for this range of resolution. Incremental converters are present in very high resolution and due to their high conversion time, achieve only slow sampling rates.

1.3.2 ADC efficiency

In order to evaluate and compare the performance of different ADCs, a "Figure of Merit" (FOM) is introduced. The low-power efficiency is measured by the total power consumption (P) versus its overall performance, which is determined by the number of signal states effectively discriminated, namely 2^{ENOB} and the sampling rate Fs.

$$FOM = \frac{P}{2^{ENOB} \cdot Fs} \quad [J] \tag{1.9}$$

It represents the cost in terms of power dissipation to achieve a given performance. The lower the FOM, the better the efficiency of the ADC.

The FOM is used here to make a comparison of the efficiency of different ADCs. It is possible to calculate an estimation of the limit of the FOM, as shown in [1]. Let's assume an ADC based on a switched-capacitor system. A capacitor C is used to sample the input. A thermal

noise can be associated as:

$$\overline{v_{th}^2} = \frac{kT}{C} \tag{1.10}$$

where k is Boltzmann's constant, T is the temperature in Kelvin and C is the sampling capacitance.
The thermal noise power should be less than the quantization noise power. If we target a too small thermal noise, we must increase the capacitance and thus the power. A good compromise is to choose the quantization noise power four times the thermal noise power.

$$\overline{B_q^2} = 4 \times \overline{V_{th}^2} \tag{1.11}$$

where $\overline{B_q^2}$ is the quantization noise power, which is the quantization noise described in (1.3) and using (1.1) can be developed as:

$$\overline{B_q^2} = \frac{q^2}{12} = \frac{V_{PP}^2}{12 \cdot 2^{2N}} \tag{1.12}$$

where V_{PP} is the peak to peak (Full-Scale) input signal voltage.

If we take (1.11) and (1.12) and we solve for the sampling capacitance, we get:

$$C = \frac{48kT2^{2N}}{V_{PP}^2} \tag{1.13}$$

This equation gives the minimum capacitance value for a certain resolution.

Assuming we are using a switched-capacitor circuit to perform the conversion, an amplifier is associated with the capacitance to charge this latter. Two methods can be considered to reach the final charge:

- A constant ramp.
- A linear settling.

In a constant ramp the voltage across C is given by

$$V_0(t) = \frac{I}{C} \cdot t \tag{1.14}$$

where t is half a period set by the sampling frequency ($t = 1/2f_s$) and I is the current used to charge the capacitor.

In a linear settling, the voltage across C must reach a certain accuracy within half the sampling period. With a transconductance amplifier (with resistive load $Ro = 1/gm$) to drive the capacitance and a unit step function, the voltage across C is

$$V_0(t) = V_{PP}\left(1 - e^{-g_m t/C}\right) \tag{1.15}$$

A settling error $\left(V_{PP}e^{-g_m t/C}\right)$ of one LSB is set to simplify the calculation. The transconductance in (1.15) is written as $g_m = 2I_D/(nV_{DSsat})$ and V_{DD} represents the power supply. With these two equations, it is possible to determine the power needed to charge the capacitance and thus compute the ideal FOM. Detailed development can be found in [1]. For a constant ramp we have:

$$Lim_{FOM1} = \frac{96kTV_{DD}2^N}{V_{PP}} \tag{1.16}$$

And for a linear setting

$$Lim_{FOM2} = \frac{N\ln(2)n\frac{V_{DSsat}}{V_{DD}}}{\frac{V_{PP}^2}{V_{DD}^2}}48kT2^N \tag{1.17}$$

Parasitic capacitance can be added to obtain a more realistic model. We assume that the ADC has as many stages as bits N, containing a certain number of nodes M_N associated with a parasitic capacitance C_N. The total parasitic capacitance is:

$$C_P = C_N M_N N \tag{1.18}$$

and is added to the total load of the amplifier expressed in (1.13).

If we consider that thermal noise is the limiting parameter, capacitor increase by a factor of 4 when the resolution is increased by one

bit, according to (1.13). The power is directly proportional and is also increased by four. However, the FOM presented in (1.9) doubles the power for an increase of one bit of resolution. There's therefore a factor of 2 between the two comparison methods and therefore comparison of ADCs with different resolution must be performed carefully. The FOM is more representative of the efficiency to carry out a conversion for a given resolution.

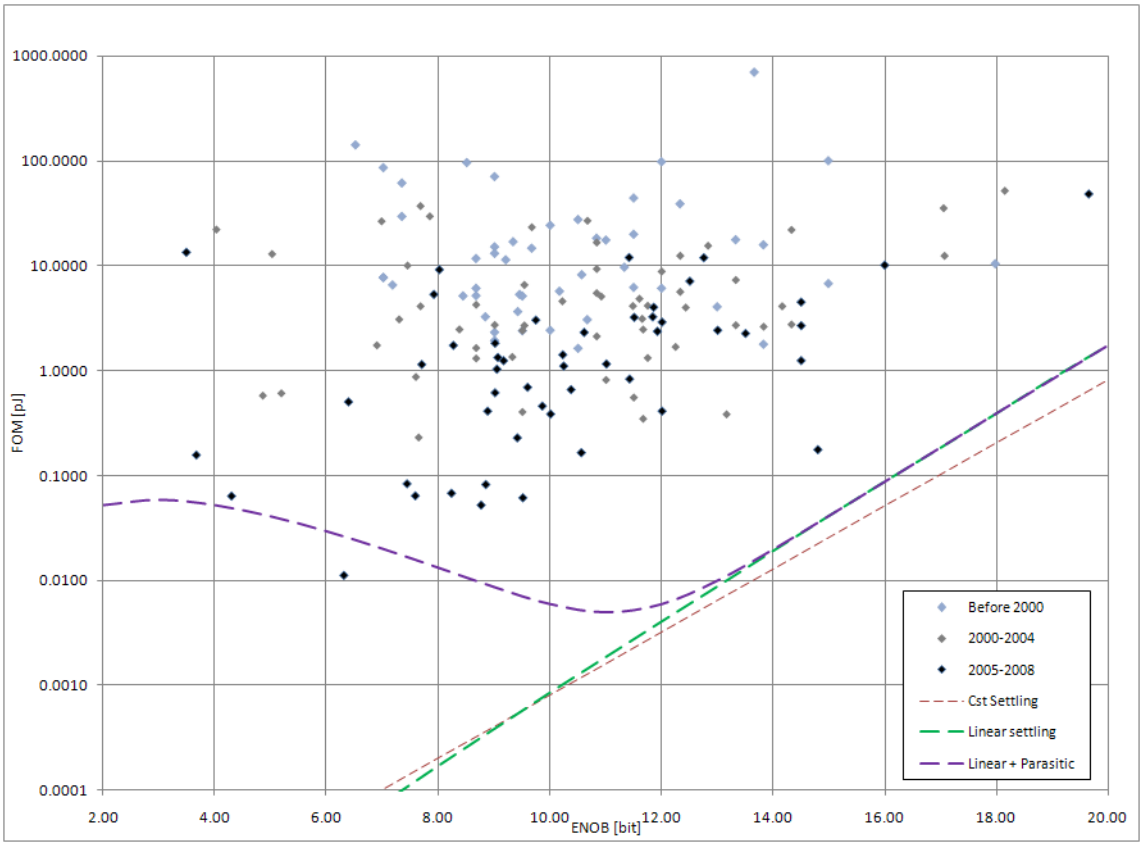

Figure 1.10 : FOM versus ENOB (with publication's year distinction)

Figure 1.10 and 1.11 represent the FOM for the same ADCs that were used in Figure 1.9. The limit Lim_{FOM1} and Lim_{FOM2} have been also plotted. We have used V_{DSsat}/V_{DD}=1/10, V_{PP}/V_{DD}=1/2 and T=300K. Lim_{FOM2} has been also plotted with a parasitic capacitance where we took M_N=50 and C_N=10fF.

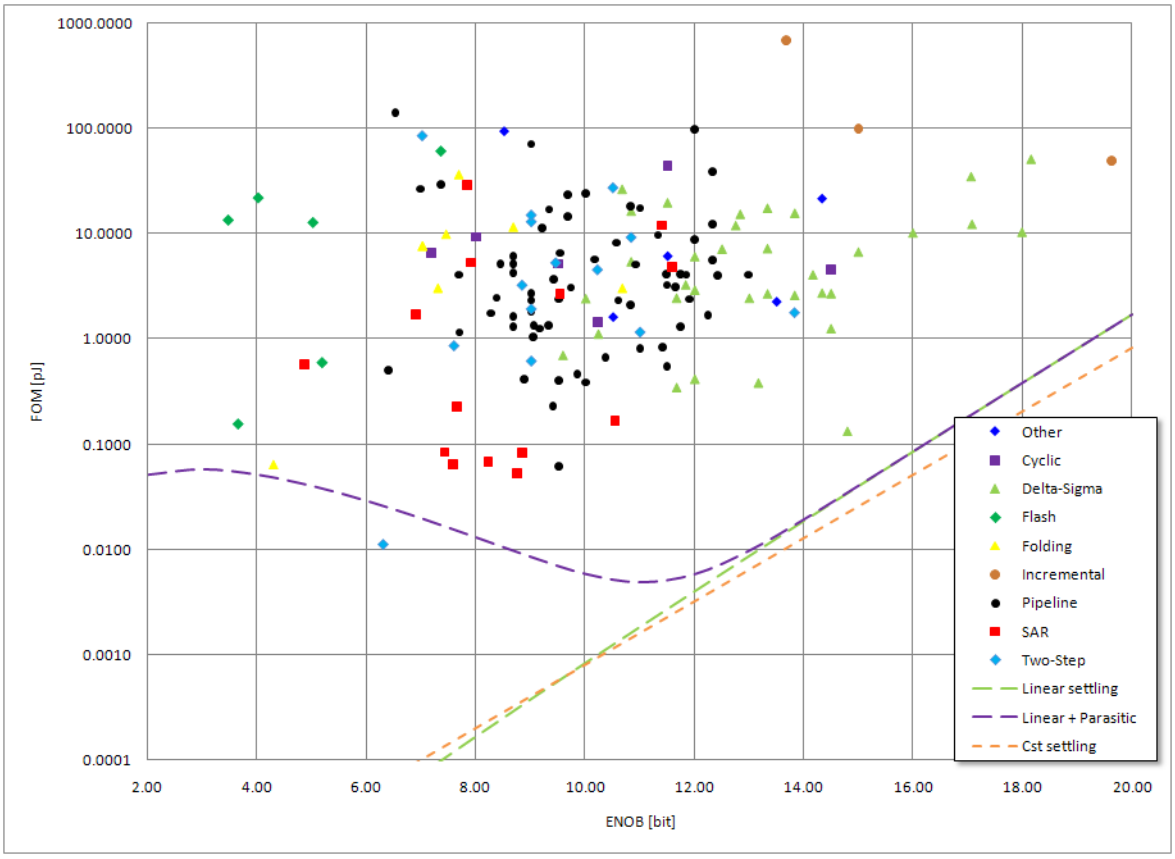

Figure 1.11 : FOM versus ENOB (with ADC families distinction)

All the ADCs are above the limits given by (1.16) and (1.17). The two limits increase by a factor of around two with the increase of one bit to the conversion. The introduction of the parasitic capacitance seems to match the observed limit with FOM. In fact at low resolution the required sampling capacitor tends to be in the same order of magnitude as the parasitic capacitance.

In recent years the power efficiency of ADCs has seen a great improvement. None of the ADCs published before year 2'000 goes under 1 pJ, while now ADCs with a FOM under 100 fJ are achieved. We can see an improvement of a factor-of-ten on the whole range of resolution within the last ten years.

For low resolution (under 7 bits), AD converters have traditionally

been implemented with flash-type. These converters are the fastest but not really power efficient, since they still use a large number of comparators. Recently a power efficiency of 65 fJ has been realized with a 5-bit folding technique [2] and even a 10 fJ has been demonstrated on a 7-bit ADC [3] with special techniques similar to SAR. These two converters are implemented in 90 nm technology.

In the field of medium resolution (8 to 12 bits), the SAR architecture is one of the most interesting regarding efficiency. A FOM of 85 fJ is obtained with 9 bits [4] and 10 bits [5]. In the last year, a Figure of Merit of 65 fJ is reached with 8 bits [6], 9 bit [7] and even 50 fJ in 10-bit [8]. Pipeline converters are also attractive candidates. Intrinsically, they offer a higher speed capability and with special technique a power efficiency of 65 fJ has been achieved [9]. 180 nm technology is used with [5] and [6] while [4] and [7] are realized in 90 nm technology and even more aggressive technology as 65 nm is used in [8] and [9].

For higher resolutions pipeline ADCs are also present with FOM approaching 1 pJ [10], [11] but effective resolution remain under 13 bits. Delta-Sigma can exhibit the same efficiency [12], [13] and recently 180 fJ is demonstrated with a 15-bit converter [14]. Reduced power consumption of the digital part is achieved with recent low-voltage technologies (90 nm and 65 nm) but also the reduction of the minimum size allow the designers to add more complex digital structures to increase the power efficiency.

1.4 Objectives

The main objective of this work is to develop and evaluate a new architecture of analog-to-digital converter for high-resolution.

- Developement of a new structure to reduce the number of cycles of the high resolution incremental converter, while keeping the same hardware. Using the fact that at the end of the conversion the quantization error is available in analog form and it is possible to further use this signal to refine the resolution, a cascading of an incremental stage with a cyclic converter will be considered.
- Use of a second-order incremental allowing another great improvement in speed. A cascading of the second-order incremental and a cyclic will be evaluated.

This increase of speed allows incremental ADCs to be used in application previously hold by Delta-Sigma. In another point of view, the power consumption can be drastically reduced for the same conversion speed, thus allowing this ADC to improve battery lifetime of portable systems.

1.5 Outline

Chapter 2 presents the different structures of interest for this thesis with detailed description.

In Chapter 3, the proposed converter based on incremental and cyclic converters is presented. A detailed operation description of the structure is provided. A theoretical analysis with non-idealities is performed to evaluate the performances. This chapter also contains a switched-capacitor implementation. Theoretical analysis is verified by simulation results.

Chapters 4 and 5 contain the two realizations that were integrated. Chapter 4 presents a first order incremental operation followed by the cyclic conversion, while Chapter 5 presents a modular prototype for first

or second order incremental implementation that was integrated. Practical aspect of the design are explained.

Chapter 6 contains the measurement results of the two prototypes integrated. A comparison of the different modes of operation is performed.

Finally, Chapter 7 gives a short overview of the work and discusses the results, as well as highlights some novel techniques which may be integrated.

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Chapter 2

High Resolution ADCs

This section discusses different existing high resolution conversion principles, some of them being used later for the new proposed structure.

2.1 Cyclic

Cyclic (or algorithmic) can be seen as a pipeline structure with only one stage where the output of the stage is fed back to the input. Compared to a pipeline, the time to process a sample is slower, while the area can be greatly reduced. Cyclic ADC can also achieve high resolution with the help of digital correction and/or calibration.

Cyclic ADC is well known for its ability to achieve medium resolution while requiring a small silicon area and featuring a reasonable conversion speed of one conversion cycle per bit of resolution. It has traditionally been used for general-purpose A/D conversion, such as microcontroller peripherals or voice applications [1]. Without any calibration or trimming, the resolution of cyclic ADCs is generally limited to 10 bits due to non-idealities such as device mismatch or finite OTA gain. Well-known techniques have been used to improve the resolution of the

cyclic ADC. Ratio-independent (for instance capacitor averaging) and gain-insensitive algorithms have been proposed [1], [2] and [3], allowing to reach 12-14 bit of resolution, at the expense of multiple conversion cycles per bit and/or additional active elements. Digital calibration is also being used, allowing up to 16 bit of resolution in cyclic [4] [5], but the important required digital circuit compromises the small silicon area and increase the power consumption.

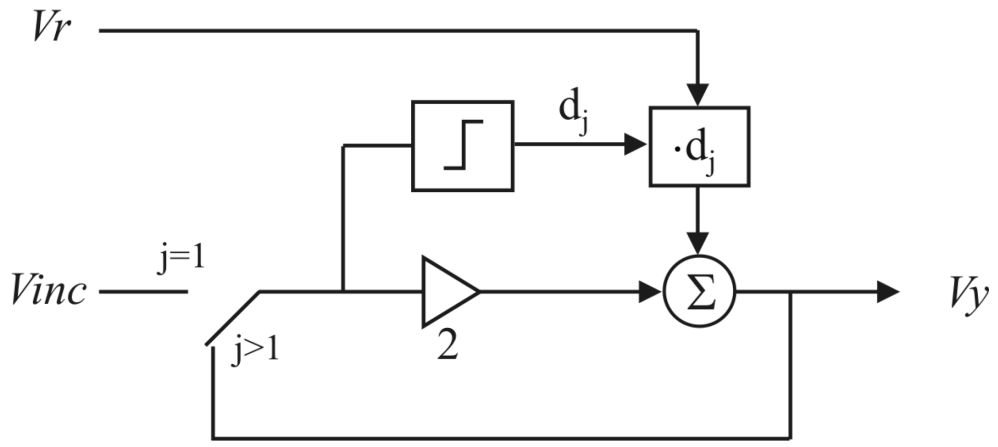

Figure 2.1 : Cyclic ADC.

The cyclic ADC conversion principle is usually implemented as in Fig. 2.1, where j conversion cycles are performed. During the first cycle ($j = 1$), the input voltage $Vinc$ is evaluated by a comparator to get bit d_1 of the result: $d_1 = 1$ if $Vinc > 0$, otherwise it is zero. $Vinc$ is multiplied by two, and an addition/subtraction of a reference voltage Vr takes place: if $d_1 = 1$, Vr is subtracted, otherwise it is added. The residue Vy is then looped back to the input for extracting the successive bits d_j of the result. The conversion is performed sequentially from the most significant bit to the least significant one. The number of cycles is proportional to the resolution. For an n-bit conversion, the number of cycle required is:

$$P_{cycl} = n - 1 \tag{2.1}$$

The cyclic conversion can use a redundant signed digit (RSD) algorithm [2]. In this scheme, two comparators with threshold voltages fixed at $+Vr/4$ and $-Vr/4$ are used, giving a ternary result d_j, which can take three values 1, 0 or -1, and leading to three possible reference voltage operations: if

- $d_j = 1$, Vr is subtracted;
- $d_j =$ -1, Vr is added;
- $d_j = 0$, no reference voltage operation is performed.

A block diagram of the RSD algorithm is shown in the next figure.

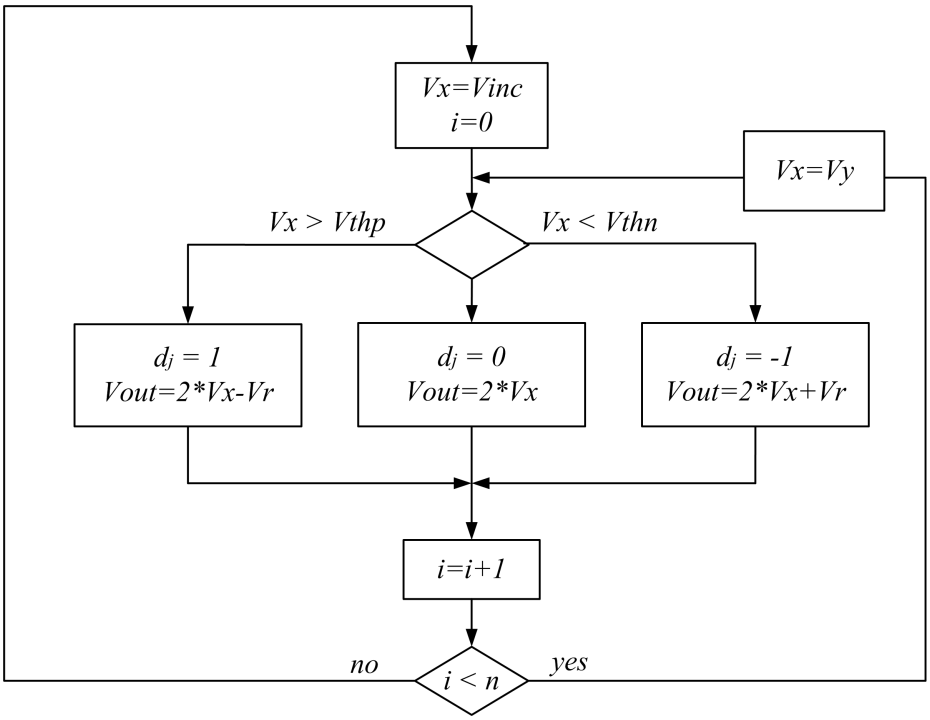

Figure 2.2 : RSD algorithm.

The use of the (RSD) cyclic algorithm offers the advantage to tolerate large comparator offset (up to $Vr/4$). Thanks to that the decision level overlaps between successive cycle conversions. The residu transfer function is shown graphically in Figure 2.3. Since a 1-bit ADC uses one

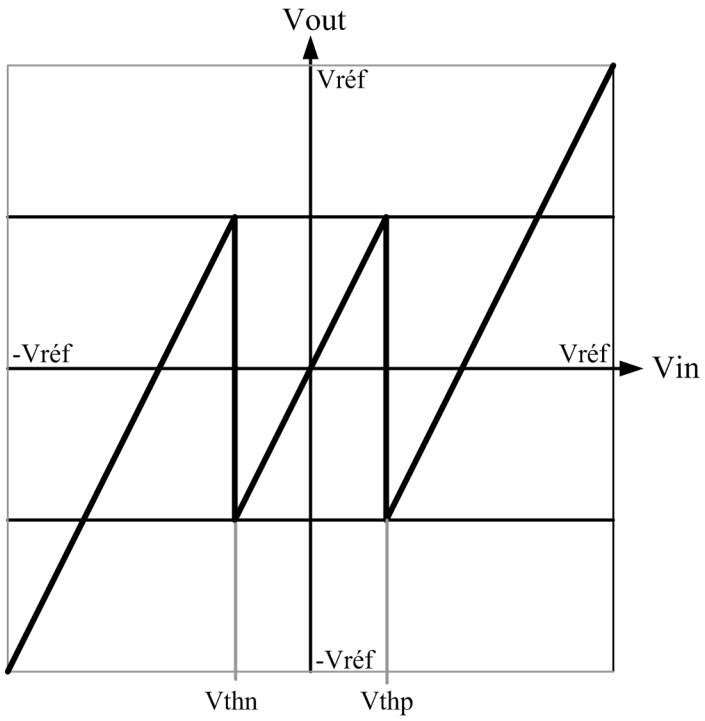

Figure 2.3 : RSD residu transfer function.

threshold, while a 2-bit ADC uses 3 levels, the use of two thresholds is referred to as 1.5 bit conversion. The redundant serial bitstream is then converted into a binary representation with additional logic.

2.2 Delta-Sigma

Quantization noise is one limiting factor for the dynamic range of an ADC and is given in equation (1.3). When the sampling frequency is increased by an oversampling ratio *OSR*, the noise floor is dropped. SNR is the same as before, but the noise has been spread over a wider range. The output is then filtered to the desired bandwidth, therefore reducing the total power of quantization noise. For an *OSR* of 2, the SNR is improved by 3 dB, or 0.5 bit/octave.

A more efficient way to use oversampling is to shape the spectral

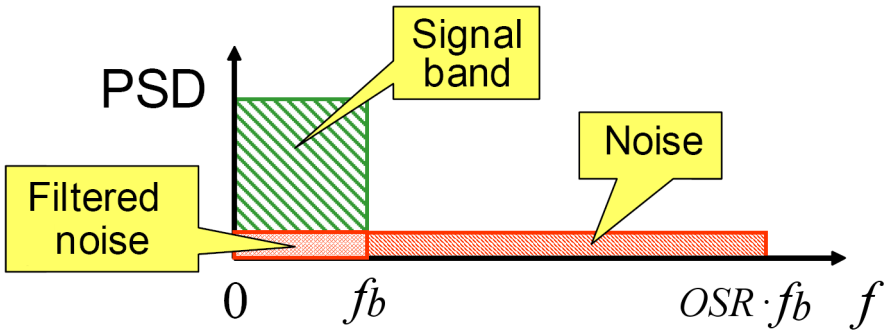

Figure 2.4 : Spectrum of an oversampled signal.

density such that most of the quantization noise power is outside of the desired signal band. A system that can do this is known as Delta-Sigma ($\Delta - \Sigma$) modulator. In a first-order modulator, the integrator acts as a high-pass filter for the quantization noise. Most of the quantization noise is pushed into higher frequencies, as shown in Figure 2.5. A digital filter applied to the noise-shaped modulator removes more noise. For a first-order modulator, the SNR improves with a rate of 9 dB/octave, or eequivalently 1.5 bit/octave.

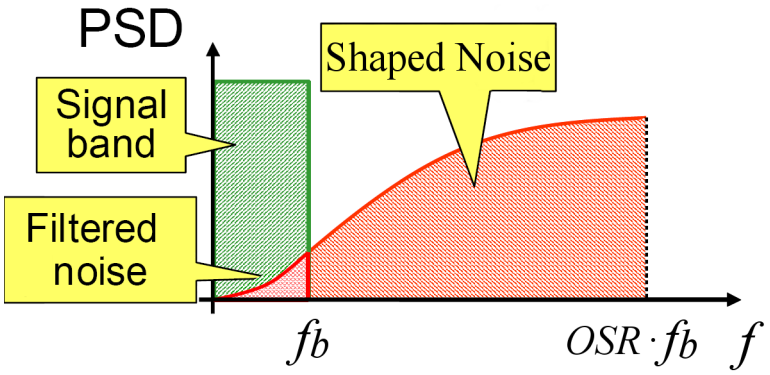

Figure 2.5 : Output spectrum of a first-order $\Delta - \Sigma$ modulator.

A complete $\Delta - \Sigma$ ADC consists of a modulator followed by a low-pass filter, as presented in Figure 2.6. It includes a difference amplifier

(Δ), an integrator (Σ) and a comparator (acting as a 1-bit ADC) with a feedback loop that contains a 1-bit DAC. The oversampled signal is converted back to Nyquist-rate by means of digital low-pass filtering and decimation. One of the benefits of using $\Delta - \Sigma$ modulation is that the ananlog circuit implementation is relatively simple.

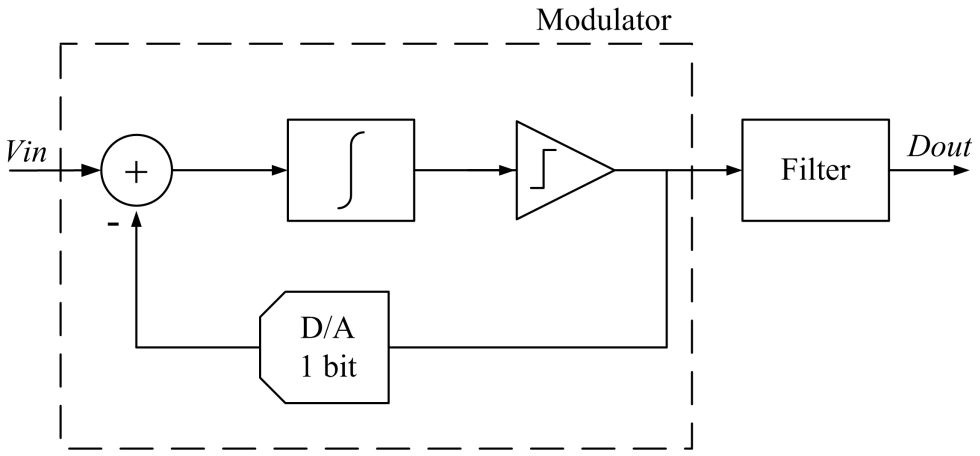

Figure 2.6 : $\Delta - \Sigma$ converter architecture.

A higher order of the modulator can achieve a better noise shaping, thus improving the SNR with the same oversampling ratio. The increase of the resolution of the quantizer and the oversampling ratio are the other method to improve the SNR. Nevertheless the order above can present problems of stability and multibit quantizer linearity is limited, affecting the accuracy.

Delta-Sigma can achieve very-high precision (more than 20 bits) but due to the oversampling (generally at least 16), the effective sampling frequency is limited to a few MS/s.

2.3 Incremental

Incremental ADC can be considered as a Delta-Sigma operated in a transient mode. Unlike the Delta-Sigma, converting a waveform in a continuous way, the incremental ADC converts individual samples with an integrator which is reset at the end of each sample's conversion. Compared to Delta-Sigma, they can achieve a higher linearity and lower offset.

For high resolutions, we have seen that oversampled ADC are the best candidates. Resolution above 20 bits can be reached with this structure [6], [7]. These converters operate with a sampling frequency much higher than the minimal required sampling frequency (f_s): $f_s \geq 2B$, where B is the input signal bandwidth. $\Delta - \Sigma$ converters are based on a modulator that samples and shapes the quantization error of the low-resolution quantizer (often one-bit) by means of analog filtering. The oversampled signal is converted back to input sample rate with digital low-pass filtering and resampling [8].

An alternative oversampling structure is the so-called incremental converter [9]. The analog and digital parts of this ADC present many similarities with the modulator, respectively the low-pass filter of a $\Delta-\Sigma$ converter. They can be considered to be delta-sigma operated in a transient mode. The converter does not operate continuously. One disadvantage of this incremental ADC is that it does not have the relaxed anti-aliasing filter requirement that conventional $\Delta-\Sigma$ ADC have. However, they provide very precise conversion, with high linearity and low offset. Digital filtering is also simpler.

2.3.1 First order incremental order

The incremental ADC introduced in [9] consists of a delta-sigma modulator which is reset before each conversion. A first-order incremental ADC is shown in Fig 2.7. The architecture is based on an integrator

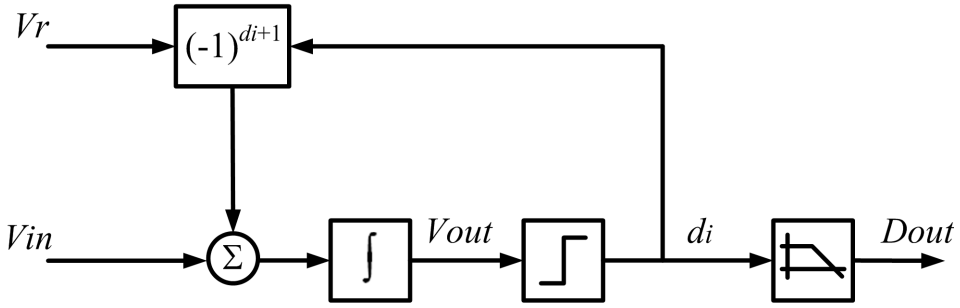

Figure 2.7 : First order incremental ADC.

and a comparator. Before each conversion, the integrator is reset. Then, for a k-bit resolution, 2^k integration steps are performed. For each step, the input voltage Vin is integrated, and depending on the sign of the digitized integrator output bit d_i, a reference voltage Vr is added or subtracted to the integrator. At the end of the 2^k steps, the output voltage $Vout$ of the integrator, called the residue voltage, is:

$$Vout_{[2^k]} = 2^k \cdot Vin - \sum_{i=1}^{2^k} d_i \cdot Vr \tag{2.2}$$

where d_i corresponds to $+1$ when the reference voltage is subtracted and -1 when it is added. The digital output $Dout$ corresponds to the number of subtraction minus the number of addition of the reference voltage Vr. The digital low-pass filter of output bitstream d_i is implemented by a simple up-down counter (first-order filter).

$$Dout = \sum_{i=1}^{2^k} d_i \tag{2.3}$$

Assuming that the input Vin is constant, it is worth noting that the amplitude of $Vout$ is always between the input range of the ADC, if

the input signal $|Vin| \leq Vr$.
Thus, with (2.2), we can write:

$$-\frac{Vr}{2^k} < Vin - \frac{1}{2^k}\sum_{i=1}^{2^k} d_i \cdot Vr < +\frac{Vr}{2^k} \tag{2.4}$$

An estimate of the input signal is:

$$\widehat{V}in = \frac{1}{2^k}\sum_{i=1}^{2^k} d_i \cdot Vr \tag{2.5}$$

In an ideal ADC the value of an LSB is defined as the full-scale input range divided by the number of quantization step:

$$V_{LSB} = \frac{2Vr}{2^k} \tag{2.6}$$

and the quantization error can be calculated as the difference between the estimated and the real input signal.

$$q = \frac{\widehat{V}in - Vin}{V_{LSB}} = \frac{\frac{1}{2^k}\sum_{i=1}^{2^k} d_i \cdot Vr - Vin}{\frac{2Vr}{2^k}} = \frac{1}{2}\sum_{i=1}^{2^k} d_i - \frac{2^k Vin}{2Vr} \tag{2.7}$$

Figure 2.8 shows the quantization error around zero input.

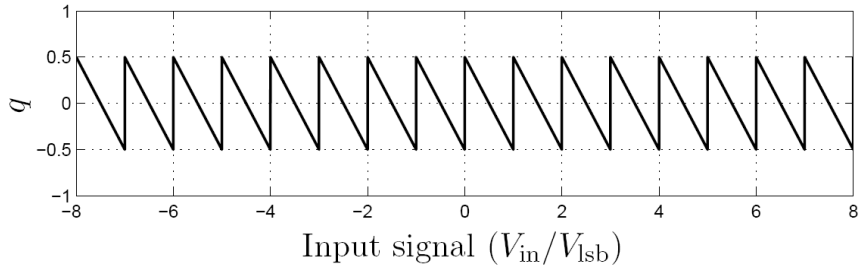

Figure 2.8 : Quantization error of the first order incremental converter.

As explained in [10], any systematic offset error at each integration step can be compensated using a double integration scheme of 2^{k-1} integration steps each (the second one using an inverted input voltage),

separated by the inversion of the residue voltage, giving the residue voltage:

$$Vout_{[2^k]} = -2^k \cdot Vin - \sum_{i=1}^{2^k} d_i \cdot Vr \tag{2.8}$$

The number of cycles P_{inc1} needed for k bits of resolution is:

$$P_{I1} = 2^k + 1 \tag{2.9}$$

2.3.2 Extension of the first-order

The first-order incremental converters biggest drawback is that it is very slow. The number of clock cycles grows exponentially with the resolution.

In $\Delta - \Sigma$ AD converter, decimation filters often consist of a higher-order filter. Analysis of high-order filters in [11] conclude that the best trade-off is to use a *m+1*-order filter for a *m*th-order modulator. As the architecture is the same of $\Delta - \Sigma$, it is interesting to apply this rule to the incremental filter. In [10], a second-order filter is used and it concludes that the resolution and the average accuracy may be increased, but the quantization error around zero remains the same. Figure 2.9 show the implementation of a first-order incremental with a second-order filter composed of two digital integrators.

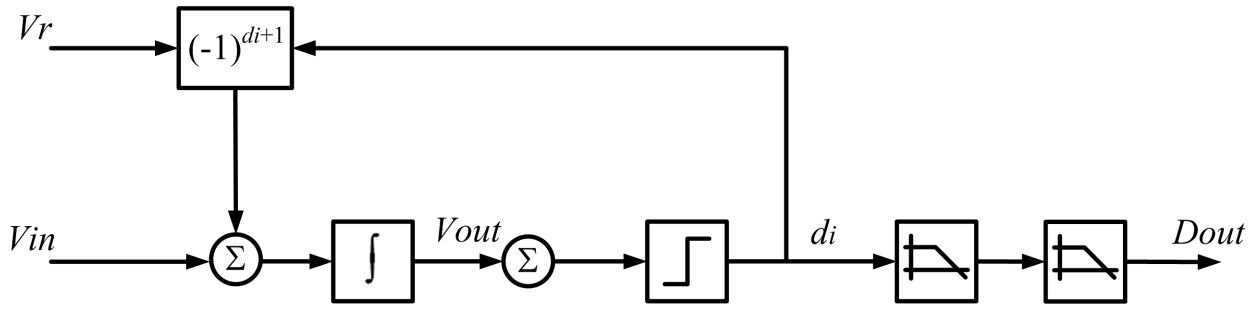

Figure 2.9 : First-order incremental with a cascade two first-order filter.

Figure 2.10 shows the quantization error of this structure around zero input. We can compare it to Figure 2.8. The average quantization noise is reduced but around zero there is a remaining peak.

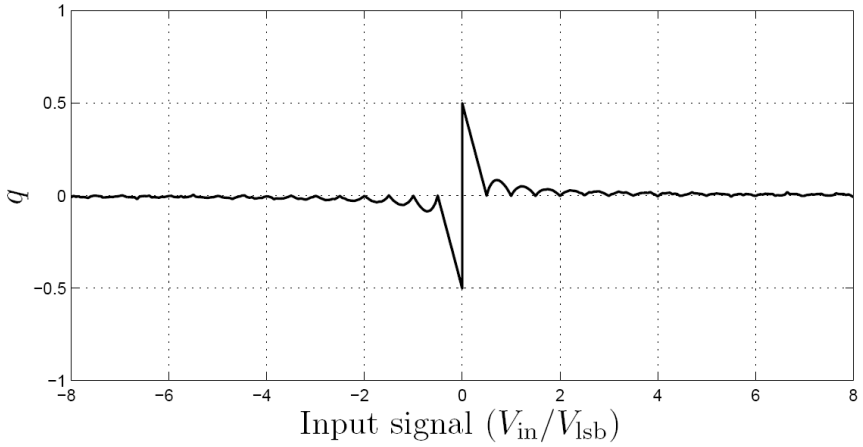

Figure 2.10 : Quantization error of the at the output of the second integrator.

For a small dc input signal, the linearized models of the quantizer and the modulator are no longer valid, i.e. the quantization noise is strongly correlated with the quantizer input. In fact, when a small signal is applied, it is clear that the signal will trigger the comparator to add Vr and the next cycle to subtract Vr, and the result would be exactly the same as if 0 input is applied. These zones, which are similar in $\Delta - \Sigma$ converter are called *dead-zones*.

This *dead-zone* problem can be canceled, and hence the higher order filter becomes effective, if the comparator is forced to make decisions and thus the whole loop is forced to operate even for extremely small input signals. This can be achieved by dithering [8]. Injecting a dither signal into the loop right before the quantizer can eliminate the error peaks around zero, as shown in Figure 2.10. For effective dithering, the amplitude needed for the injected dither signal should be fairly large (typically 0.3−0.6 LSB of the quantizer). Simulation of the quantization error is shown in Figure 2.12. The peak error around zero has completely

disappeared. With this technique, referring to [12] the number of cycles

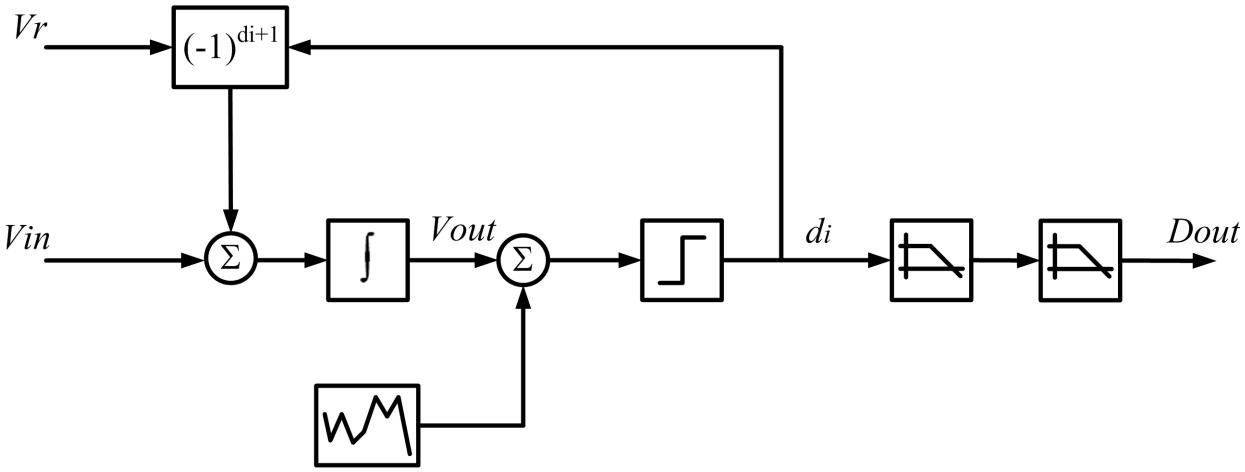

Figure 2.11 : First-order incremental with a cascade two first-order filter and dithering signal.

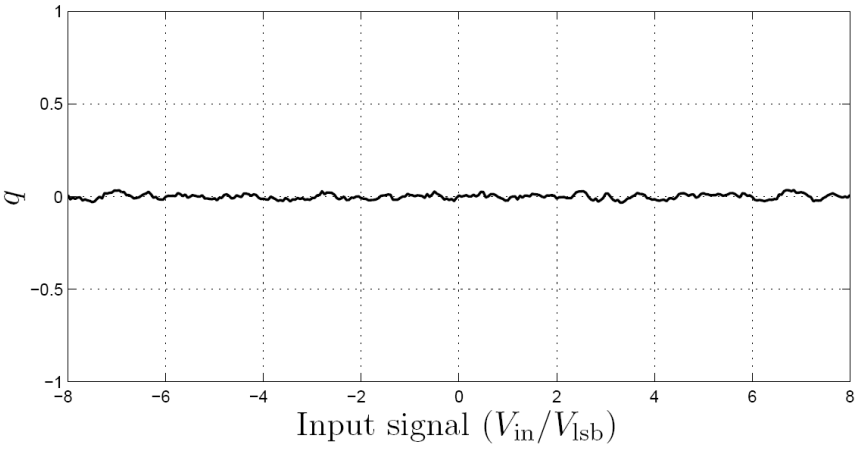

Figure 2.12 : Quantization error of the at the output of the second integrator, with dither signal injected into the loop.

$P_{I1,2}$ needed for k bits of resolution is decreased to:

$$P_{I1,2} = 3.9 \cdot 2^{\frac{2k}{3}} \tag{2.10}$$

For example, for a given resolution of 16 bits, the original converter should be operated through $P_{I1} = 65'537$ cycles, while the modified converter requires only $P_{I1,2} = 6'340$ cycles.

2.3.3 Second-order incremental

The first-order incremental ADC previously described can easily be cascaded with a similar stage [10], also called multistage delta-sigma modulator. The order of the used modulators specifies the type of the structure. Here we have a 1-1 multistage for the cascade of two first-order modulators. We will use the term second-order modulator for the 1-1 structure. Figure 2.13 shows the details of the structure. A

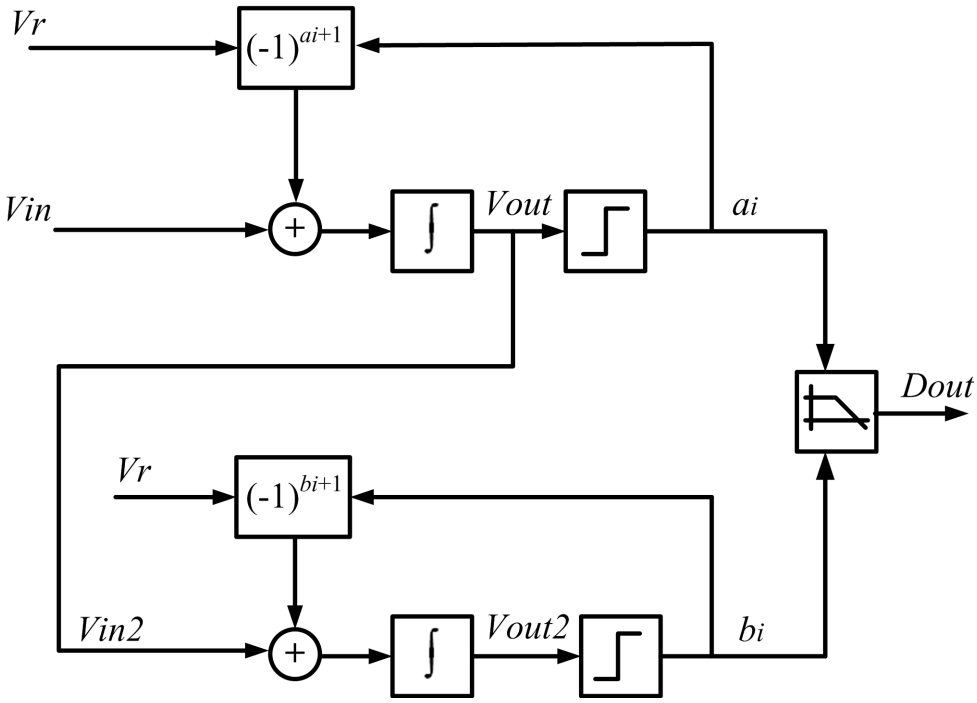

Figure 2.13 : Second order incremental ADC.

conversion begins with a reset operation of the two integrators, followed by an integration step of the first stage, giving residue voltage *Vout*. Then, p integration steps are performed, during which both first and second stages integrate their input signals, i.e. *Vin* for the first stage and *Vout* for the second stage. At the end of the p cycles, one more

integration step is needed for the second stage to complete p cycles.

$$Vout2_{[p+1]} = \frac{p \cdot (p+1)}{2} \cdot Vin - \sum_{i=1}^{p} a_i(p+1-i) \cdot Vr - \sum_{i=2}^{p+1} b_i \cdot Vr \quad (2.11)$$

Then, similarly to the first-order case, the output voltage of the first integrator is reset, while the residue *Vout2* of the second stage is inverted. Another *p+1* integration steps are performed with an inverted input voltage *Vin* and the finally we have:

$$\begin{aligned} Vout2_{[2p+2]} =& p \cdot (p+1) \cdot Vin - \sum_{i=1}^{p} a_i(p+1-i) \cdot Vr \\ & - \sum_{i=p+2}^{2p+1} a_i(2p+2-i) \cdot Vr - \sum_{i=2}^{p+1} b_i \cdot Vr - \sum_{i=p+3}^{2p+2} b_i \cdot Vr \end{aligned} \quad (2.12)$$

The dynamic range of $Vout2_{[2p+2]}$ is given by

$$-Vr \leq Vout2_{[2p+2]} \leq Vr \quad (2.13)$$

In an ideal converter the quantization error is given by:

$$-\frac{V_{LSB}}{2} \leq Vin - N_2 \cdot V_{LSB} \leq \frac{V_{LSB}}{2} \quad (2.14)$$

where N_2 is the digital representation of *Vin* and V_{LSB} is the analog voltage corresponding to the LSB (see equ. 2.6)

From (2.13) and (2.14), we have:

$$V_{LSB} = \frac{2 \cdot Vr}{p\,(p+1)} \quad (2.15)$$

and

$$\begin{aligned} N_2 =& \sum_{i=1}^{p} a_i(p+1-i) + \sum_{i=p+2}^{2p+1} a_i(2p+2-i) \\ & + \sum_{i=2}^{p+1} b_i + \sum_{i=p+3}^{2p+2} b_i \end{aligned} \quad (2.16)$$

Resolution k is given by the number of LSB step over the full range

$$k = \log_2 (2Vr/V_{LSB}) = 2 \cdot \log_2 (p) \tag{2.17}$$

The total number of cycles P_{I1-1} required for k bits of resolution is:

$$P_{I1-1} = 2p + 2 = 2^{k/2} + 2 \tag{2.18}$$

If we take a 16-bit ADC, the first-order converter should be operated through $P_{I1} = 65'537$ cycles, while the second-order requires only $P_{I1-1} = 258$ cycles.

The digital processing as shown by (2.16) is composed of two first order digital filters with triangular and rectangular-shaped impulse response.

2.3.4 Higher order incremental

Another way to reduce the number of cycles through the converter is to use higher-order modulator structures. Similarly to the $\Delta - \Sigma$ converters, this leads to less cycles for a given resolution due to the higher loop-gain and the more aggressive noise shaping. Multiple archi-

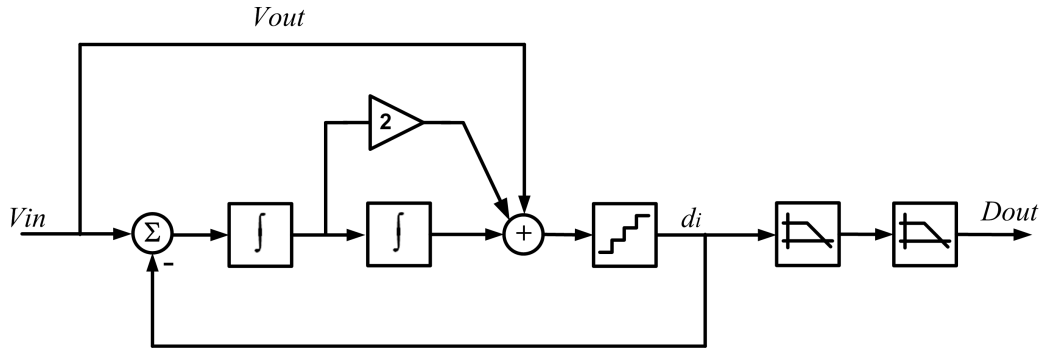

Figure 2.14 : Second-order incremental with the input signal fed forward to the input of the quantizer (CIFF structure)

tectures are present with high-order modulators. In Figure 2.14 a possible second-order realization is shown. Quantizers are often increased

to insure stability for order above 3. For a second-order converter with 1-bit quantizer the required number of cycles for k bit is:

$$P_{I2} = 2^{k/2} + 1 \tag{2.19}$$

In [12] a third-order incremental converter with a 4^{th} order filter is presented and the number of cycles for k bit of resolution is:

$$P_{I3} = 4.52 \cdot 2^{k/3.5} \tag{2.20}$$

Higher order modulators present potential disadvantages: The first one has to do with the ability to use multibit quantizers. The linearity of the corresponding multibit feedback DAC is limited, and it directly affects the overall accuracy of the ADC. The second nonideal effect has to do with stability: higher-order loops (over 2) have the potential to become unstable. Digital filtering becomes also more complex as well as area and power consuming.

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Chapter 3

Proposed ADC

This chapter focuses on the new proposed structure. It introduces the cyclic and incremental converters and discusses its operation in details. The different extensions of the introduced architecture are also analyzed. Then the hybrid structure is proposed and a theoretical analysis is provided. Simulations based on the theoretical equations are provided and finally a possible implementation is presented.

3.1 Cascading ADCs

In order to fully exploit the distinctive advantages of different conversion principles, cascaded converters have been introduced. Oversampled conversion has been used in the front-end for the high resolution conversion, and the residue has been fed to a pipeline [1], [2]. In [3] a $\Delta - \Sigma$ modulator is cascaded with a 4-bit flash converter, with smaller accuracy but much faster conversion speed.

At the end of the conversion of the incremental converter, the quantization error multiplied by 2^n is available as an analog signal. As this is a large signal, it can be easily used for further refining the conversions resolution. In [4] the quantization error is digitized at the end of

each conversion with a Nyquist-rate multibit converter. In [5], successive approximation is used at the end of the conversion.

This work present the design of a new cascaded (or hybrid) converter topology made of an incremental converter and a cyclic converter. The oversampled stage extracts the most significant bits (MSB) of the result, and produces an analog residual voltage (the residual quantization noise). This voltage is then passed to a cyclic converter, which extracts the least significant bits (LSB) of the result. Cyclic and incremental have in common that they can be implemented in a simple way: a switched-capacitor circuit. Thus, it is possible to use both converters in a cascaded mode with the benefit of each converter. The biggest advantage of this new topology is that both converters can share the same hardware, thus leading to a very compact converter.

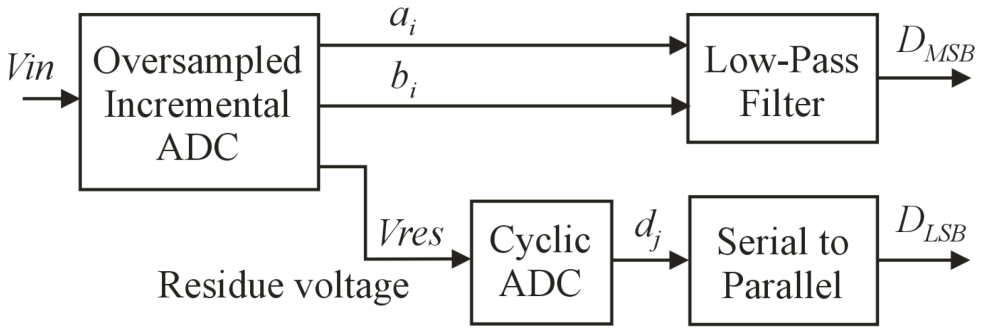

Figure 3.1 : Proposed conversion scheme.

The proposed conversion principle, represented in Fig. 3.1, consists of a two-step conversion scheme. An oversampled, incremental ADC is used in the first step, producing one or several digital bitstreams, one for each modulator (the figure shows a two stage modulator with bitstreams a_i and b_i), which are filtered through a low-pass filter to obtain D_{MSB}, the most significant part of the conversion result. The residue voltage *Vres* of the incremental ADC is fed into a cyclic ADC, producing a serial bitstream d_j, which is transformed into parallel format to obtain D_{LSB},

the least significant part of the result.

The re-use of the quantization error is only suitable with incremental converter where the quantization error is available in analog form at the output of the integrator. This is not the case with the first-order incremental with higher order filter.

Like in any sub-ranging ADC, any difference between the output range Ao of the first stage residue and the input range Ai of the second stage causes differential non-linearity errors.

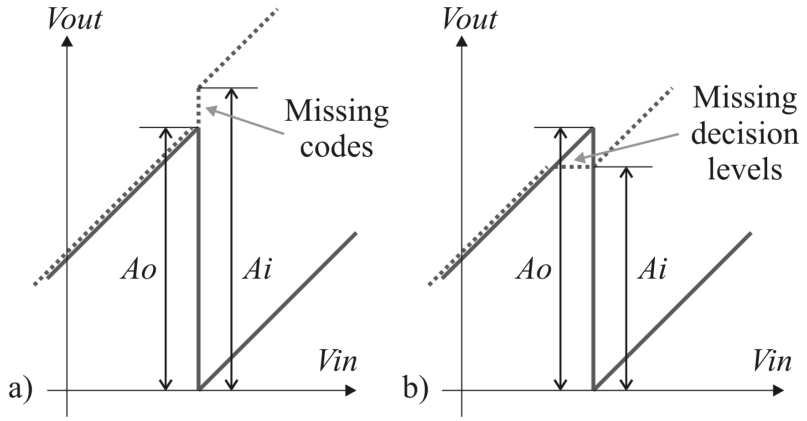

Figure 3.2 : First stage output residue Vout in function of its input Vin (solid line) and corresponding second stage result (dashed line) in case of inter-stage amplitude mismatch: a) Ao < Ai causes missing output codes, while b) Ao > Ai causes missing decision levels.

A residue voltage that exceed the [-Vr:+Vr] interval ($Ao > Ai$) is out of the cyclic range and establishes an LSB code of all ones which remains unchanged until the input re-enters the boundaries. On the other hand if the residue does not reach the -Vr or +Vr limit ($Ao < Ai$) then the LSB cyclic does not switch from zero to Full-Scale or vice-versa leading to missing codes.

In a practical implementation, a perfect output to input amplitude matching between the two cascaded converters must be guaranteed to

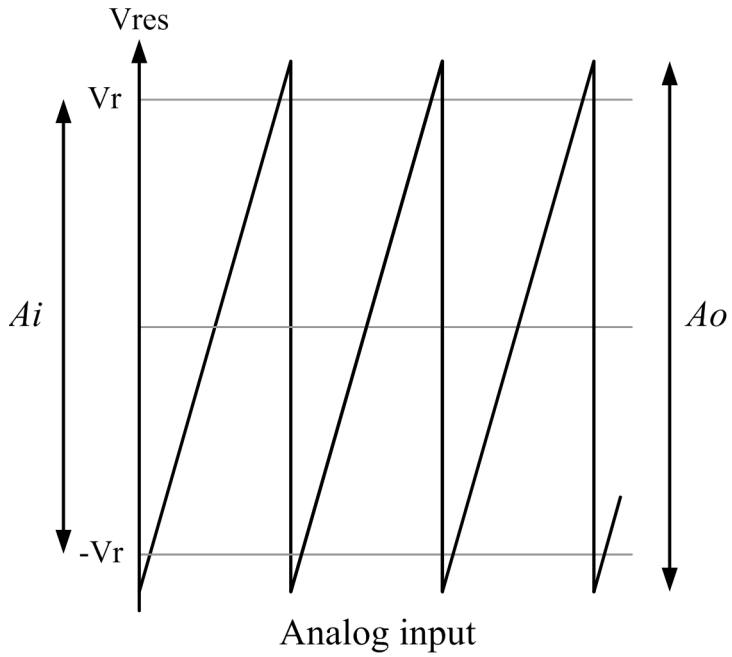

Figure 3.3 : Residu of the incremental converter with a residue voltage higher than the input range of the cyclic.

avoid non-linearity effects. Since the amplitude of the residue voltage of the incremental ADC may go above $+Vr$ or below $-Vr$ (due to comparator offset), an over range input capability for the cyclic ADC must be provided. This feature can be implemented by inserting a supplementary cycle at the beginning of the cyclic conversion, during which a reference addition/subtraction is performed on a non-doubled input voltage (see Figure 3.4)

3.1.1 Resolution Comparison

In the proposed conversion scheme, the n-bit cyclic ADC is used to convert the residue voltage *Vout* (for the first-order) or *Vout2* (for the second-order) of the k-bit incremental ADC, giving an overall resolution $m = k + n$. The total number of cycles per conversion as function of the

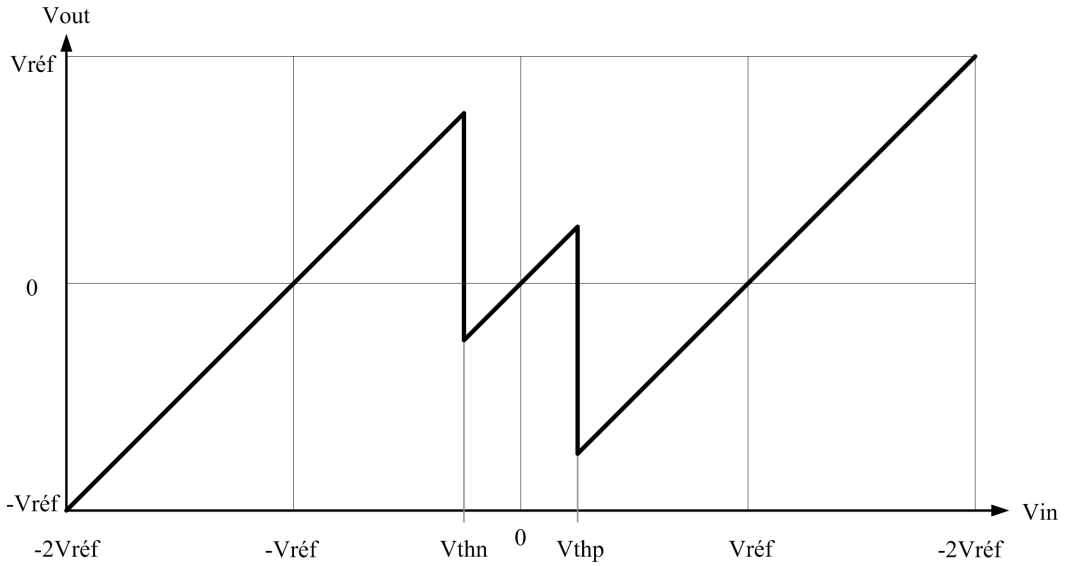

Figure 3.4 : Transfer function of the extra-cycle.

resolutions k and n is given by:

$$P_{H1} = 2^k + n + 1 \tag{3.1}$$

$$P_{H2} = 2^{k/2} + n + 2 \tag{3.2}$$

Assuming ideal ADCs (no mismatch, no thermal noise) and excluding extra-cycle and using a single integration scheme, the number of cycles per conversion in function of the theoretical resolution is plotted in Figure 3.5 for four different configurations of the proposed hybrid converter (first- and second-order with 6 or 8 bit of cyclic resolution n) and for the pure incremental 1^{st} and 2^{nd} order approach. The first order incremental with second order digital filtering is also added (Eq. 2.10). For comparison, the curves of incremental of third-order and Delta-Sigma of first to third order are also plotted. For $\Delta-\Sigma$, relations from [6] are used for the number of cycles per conversion in function of the resolution.

In this figure, we see that the proposed first-order structure performs faster, for all resolutions, than the first-order incremental even with second-order filter. It is also faster than second-order incremen-

tal up to 12 or 16 bits depending on the number of bits solved by the cyclic. The proposed second-order structure is faster than a 3^{rd} order incremental structure.

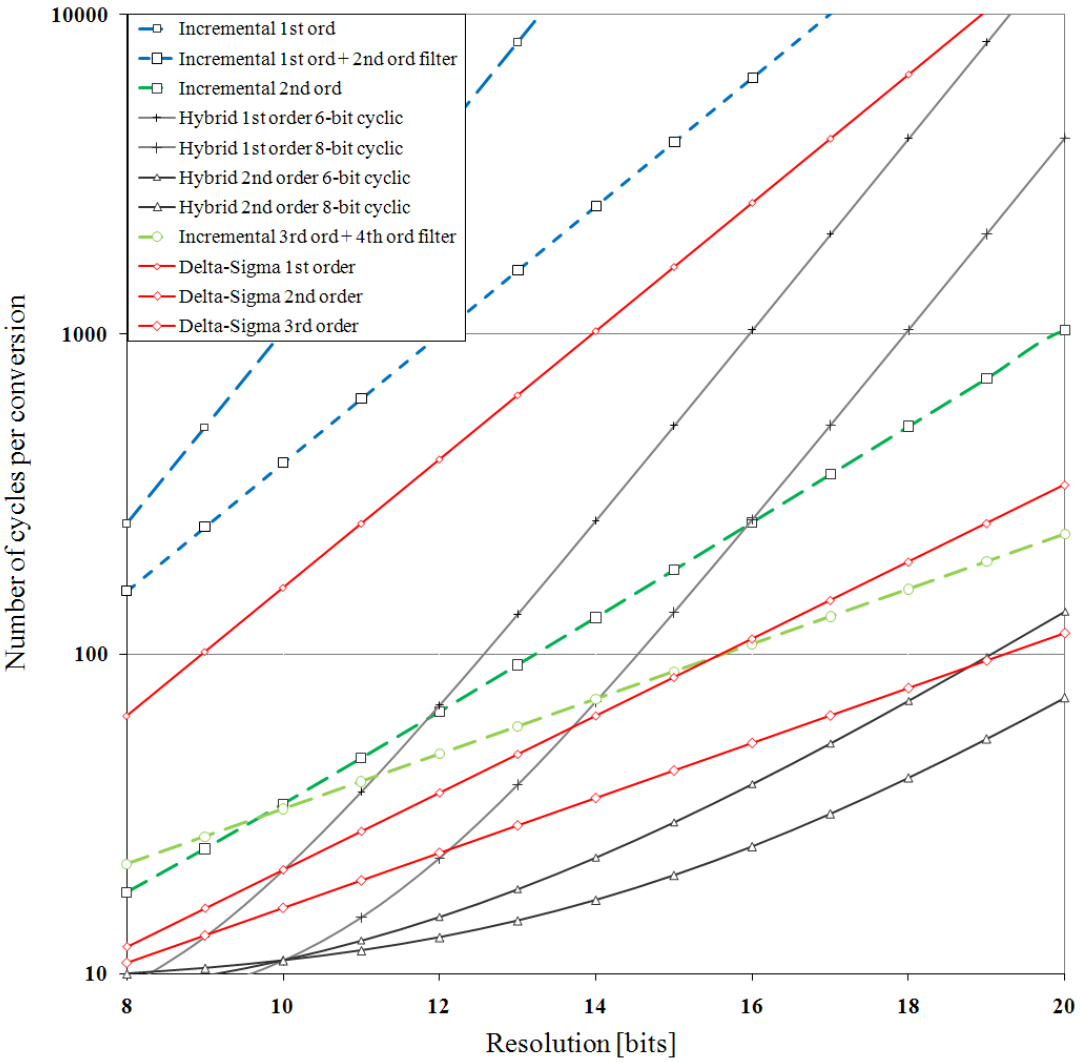

Figure 3.5 : Theoretical number of cycles per conversion in function of resolution, for a 1^{st} and 2^{nd} order incremental ADC, a 1^{st} incremental with second-order digital filtering, a 1^{st} order incremental ADC followed by a 6-bit and 8-bit cyclic ADC, a 2^{nd} order incremental ADC followed by a 6-bit and 8-bit cyclic ADC a 3^{rd} order incremental and a Delta-Sigma from 1^{st} to 3^{rd} order.

3.2 Theoretical analysis

The different structures introduced before have non-idealities that affect their results.

Cyclic

In the cyclic converter a gain error γ and δ can be assigned to the feedback voltage, respectively the reference voltage. Figure 3.6 shows the two introduced errors.

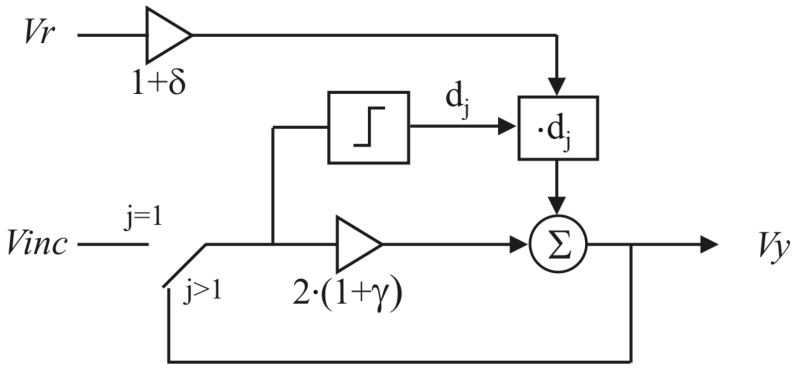

Figure 3.6 : Cyclic ADC with error γ and δ.

At each cycle the residue voltage Vy is affected by errors γ and δ as follow: after the first cycle, we have:

$$Vy_{[1]} = 2 \cdot (1+\gamma) \cdot Vinc - d_1(1+\delta) \cdot Vr \tag{3.3}$$

Thus, at the end of the conversion, requiring *n-1* cycles, we have:

$$\begin{aligned} Vy_{[n-1]} = &(2 \cdot (1+\gamma))^{n-1} \cdot Vinc \\ &- (1+\delta) \cdot \sum_{j=1}^{n-1} d_j \cdot (2 \cdot (1+\gamma))^{n-1-j} \cdot Vr \end{aligned} \tag{3.4}$$

Incremental first-order

In the first-order incremental converter, gain errors α and β on the input voltage *Vin*, respectively the reference voltage *Vr*, are added. The

residue voltage after a conversion is:

$$Vout_{[2^k]} = -(1+\alpha)\cdot 2^k \cdot Vin - (1+\beta)\sum_{i=1}^{2^k} d_i \cdot Vr \tag{3.5}$$

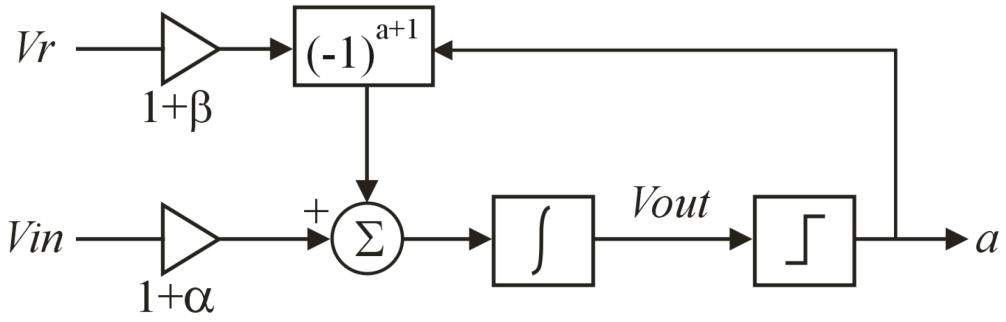

Figure 3.7 : First-order incremental with error α and β.

Incremental second-order

With the second-order scheme we can add gain errors of α_2 and β_2 on the input voltage, respectively the reference voltage of the second stage. The residue voltage *Vout2* of the integrator, after *2p+2* steps, is:

$$\begin{aligned} Vout2_{[2p+2]} =& p\cdot(p+1)(1+\alpha_1)\cdot(1+\alpha_2)\cdot Vin \\ &- (1+\beta_1)\cdot(1+\alpha_2)\cdot\sum_{i=1}^{p} a_i(p+1-i)\cdot Vr \\ &- (1+\beta_1)\cdot(1+\alpha_2)\cdot\sum_{i=p+2}^{2p+1} a_i(2p+2-i)\cdot Vr \\ &- (1+\beta_2)\cdot\sum_{i=2}^{p+1} b_i\cdot Vr - (1+\beta_2)\cdot\sum_{i=p+3}^{2p+2} b_i\cdot Vr \end{aligned} \tag{3.6}$$

Now that we have introduced the error parameters, we can analyze the effect of parameters α, β, α_2, β_2, γ and δ (gain and reference errors) on the overall resolution of the proposed converters.

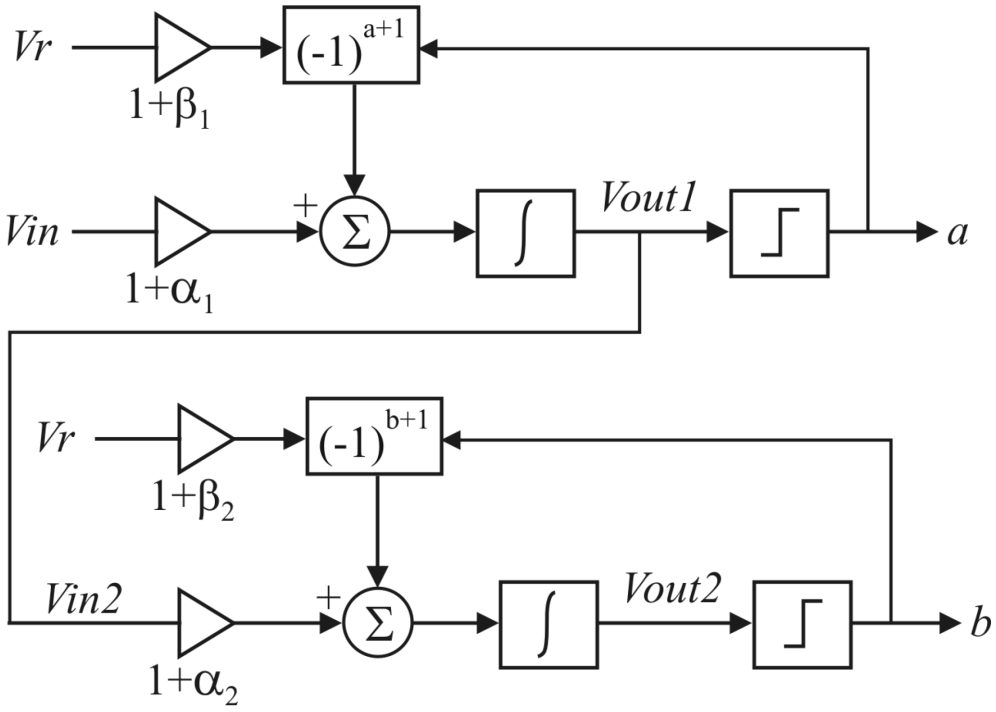

Figure 3.8 : Second-order incremental with gain errors.

3.2.1 Extra cycle errors

The amplitude matching between the first (incremental) and second (cyclic) stages of the proposed structure requires an over range capability for the RSD converter. This can be performed simply by an extra cyclic conversion without doubling operation, with the following equation:

$$Vy_{[j]} = (1+\gamma) \cdot Vinc - d_j \cdot Vr + Vy_{[j-1]} \tag{3.7}$$

The location in time of this extra cycle influences the dynamic of the input range, and the obtained gain error. In the normal case, the converter input range is $[-Vr, +Vr]$. If the extra cycle occurs before the first cycle, the dynamic of the converter will be increased by Vr on both sides of its range, leading to an input range of $[-2Vr; +2Vr]$. If it is done before the second cycle, the maximum input signal dynamic will be $+3/2\,Vr$, etc. The input range of the converter can thus be described with the following equation, where j represents the location of the extra-cycle in

the cyclic conversion:

$$\left[\left(-1-\frac{1}{2^{j-1}}\right)\cdot Vr;\left(1+\frac{1}{2^{j-1}}\right)\cdot Vr\right] \tag{3.8}$$

The position of the extra-cycle has an influence on the dynamic input range but also on the propagation of the errors. Let us see the error introduced by γ in the cyclic conversion. Parameter γ introduces an overall gain error which affects the amplitude matching between the first and second stages, and hence introduce DNL errors at the first stage residue voltage transitions: if $\gamma > 0$ (amplification), missing decision levels appear; if $\gamma < 0$ (attenuation), missing codes appear. To analyze this error, we take the maximum input signal value, corresponding to an input of $+Vr$. The binary output code is [1, 1, ... , 1], and the obtained voltage is:

$$Vy_{[n]} = 2^{n-1}\cdot(1+\gamma)^n\cdot Vr - \sum_{j=1}^{n} d_j\cdot(1+\gamma)\cdot(2(1+\gamma))^{n-j}\cdot Vr \tag{3.9}$$

After n cycles, the residue voltage is equal to 0 when $\gamma = 0$. If the extra cycle occurs before the first cycle ($j = 1$), the overall DNL error is:

$$\Delta_{\gamma E(j1)} = \gamma\cdot 2^n \tag{3.10}$$

However, if this operation is done before the second cycle ($j = 2$), the overall error will be bigger because a doubling operation is done before. We obtain:

$$\Delta_{\gamma E(j2)} = \gamma\cdot 3\cdot 2^{n-1} = 1.5\cdot\Delta_{\gamma E(j1)} \tag{3.11}$$

It is possible to characterize the amount of error introduced by γ and by the position T of the extra-cycle:

$$\Delta_{\gamma E(jT)} = \gamma\cdot(2^{T-1})\cdot 2^{n-T+1} \tag{3.12}$$

With this expression we can determine that minimal error is obtained when the extra cycle is performed before the first conversion cycle.

3.2.2 Cyclic conversion

In a first step, we consider the cyclic RSD conversion inaccuracies with the influence of parameter γ. We have seen before the influence of this parameter at the first stage transition. But errors also appear within the cyclic conversion, located at the MSB transitions of the cyclic conversion, corresponding to the comparator thresholds (usually $+Vr/4$ and $-Vr/4$), where the same input voltage can give two different ternary codes having the same binary result. The corresponding codes are [0, 0, 1, 0, ..., 0] and [1, -1,-1, 0, ..., 0] (from the MSB to the LSB). With an ideal converter, these codes would give two identical residue voltages *Vy'* and *Vy"*. From (3.3), and after n cycles, we have:

$$Vy' = (1+\gamma)\cdot(2(1+\gamma))^{n-1}\cdot Vinc - \left((2(1+\gamma))^{n-3}\right)\cdot Vr \tag{3.13}$$

$$\begin{aligned} Vy'' = {} & (1+\gamma)\cdot(2(1+\gamma))^{n-1}\cdot Vinc \\ & - \left((2(1+\gamma))^{n-1} - (2(1+\gamma))^{n-2} - (2(1+\gamma))^{n-3}\right)\cdot Vr \end{aligned} \tag{3.14}$$

The difference between these two values is:

$$\begin{aligned} Vy'' - Vy' &= Vr\cdot\left(2\,(2(1+\gamma))^{n-3} + (2(1+\gamma))^{n-2} - (2(1+\gamma))^{n-1}\right) \\ &\cong Vr\cdot\gamma\left(2^{n-2}\cdot(2n-5) - 2^{n-1}\,(n-1)\right) \end{aligned} \tag{3.15}$$

If we divide this difference by Vr, we obtain the maximal intrinsic non-linearity error of the cyclic RSD ADC, occurring at the MSB

transitions of the cyclic conversion:

$$\Delta_{\gamma C(j1)} \cong 3 \cdot 2^{n-2} \cdot \gamma \tag{3.16}$$

This error is smaller than the error introduced at the first stage residue voltage transitions (see Eq. (3.10)). If the extra cycle is done before the second cycle, the major error appears at voltages $\pm Vth/2$ (i.e. $\pm Vr/8$). The critical codes are [0, 0, 0, 1, 0, ..., 0] and [0, 1,-1, -1, 0, ..., 0], and the error is:

$$\Delta_{\gamma C(j2)} = 3 \cdot 2^{n-3} \cdot \gamma \tag{3.17}$$

The error is even smaller if the extra cycle is done in the second cycle, but in all cases this error in the cyclic conversion is still smaller than the one at the transition points.

The second error parameter δ of the cyclic converter modifies the reference voltage of the cyclic conversion, and therefore degrades also the inter-stage voltage matching, producing DNL errors at the first stage residue voltage transitions. To analyze this error, we take the maximum input signal value, corresponding to an input of $+Vr$. The corresponding voltage residue is:

$$Vy_{[n]} = 2^{n-1} \cdot Vr - (1+\delta) \sum_{j=1}^{n} d_j \cdot 2^{n-j} \cdot Vr \tag{3.18}$$

Since it is doubled at each cycle, the error value is:

$$\Delta_{\delta(C)} = -\delta \cdot 2^n \tag{3.19}$$

3.2.3 First-order implementation

As expressed in (2.7), the residue voltage of a first-order incremental ADC has the appearance of a periodic falling ramp. Parameter α affects

Vin only, modifying the dynamic range of the conversion, but not its linearity. Parameter β increases the amplitude of the residue, thus contributing to the inter-stage amplitude mismatch with a positive DNL located at the transition points of the residue voltage *Vout*, multiplied by the cyclic gain 2^n of the second stage:

$$\Delta_\beta = \beta \cdot 2^n \tag{3.20}$$

3.2.4 Second-order implementation

Since the same second stage (cyclic RSD ADC) is used, it introduces the same DNL errors than for the first-order implementation. Let us now consider the influence of parameters α_1, α_2, β_1 and β_2.

Parameter α_1 influences only *Vin* and does not contribute to non-linearity. Due to the presence of the second integration loop, any DNL of the first integration loop will be multiplied by the integration factor $2^{k/2}$ of the second loop (cumulative effect). As for the first-order implementation, a positive DNL due to β_1 occurs at the transition points of the first residue voltage *Vout1*. This error is multiplied by $(1+\alpha_2)\cdot 2^{k/2}$ and by the gain 2^n of the second stage:

$$\Delta_{\beta 1} = \beta_1 \cdot (1+\alpha_2) \cdot 2^{k/2} \cdot 2^n \cong \beta_1 \cdot 2^{n+(k/2)} \tag{3.21}$$

Following the same inter-stage amplitude mismatch analysis, parameter α_2 of the second integrator stage, because of its amplification effect, produces also a positive DNL which is multiplied by the subsequent stage gains:

$$\Delta_{\alpha 2} = \alpha_2 \cdot 2^{n+(k/2)} \tag{3.22}$$

Finally, parameter β_2 introduces a negative DNL, which is also amplified by the integrator:

$$\Delta_{\beta 2} = -\beta_2 \cdot 2^{n+(k/2)} \tag{3.23}$$

These three errors (3.21-3.23) do not appear systematically on all transition points of the first integrator residue voltage. The biggest appears at the middle of the dynamic input range, which corresponds to the threshold of the comparator, while the others appear at all the other residue voltage locations with unequal values due to compensation phenomena between α_2, β_1 and β_2.

3.2.5 Summary of the errors and comments

The theoretical linearity errors of the proposed hybrid ADC are summarized in Table 3.1. For the first-order implementation, error parameters β, γ and δ contribute each to the same error at the first stage residue voltage transitions. Interestingly, β, γ and δ can cancel each other. They can therefore be grouped into the same parenthesis. Parameter γ gives raise to slightly smaller error at the 2^{nd} stage MSB transition points.

Position	Linearity errors (LSB) 1st order incr. conversion	2nd order incr. conversion
In the cyclic conversion	$\gamma \cdot 3 \cdot 2^{n-2}$	$\gamma \cdot 3 \cdot 2^{n-2}$
At each residue transition of the 1st stage	$(\beta + \gamma - \delta) \cdot 2^n$	$(\gamma - \delta) \cdot 2^n$
Middle of input range	-	$(\alpha_2 + \beta_1 - \beta_2) \cdot 2^{n+(k/2)}$
Other residue transition positions	-	$(\alpha_2 + \beta_1) \cdot 2^{n+(k/2)-1}$ $(-\beta_2) \cdot 2^{n+(k/2)-1}$

Table 3.1 : Linearity errors introduced by the different non-idealities in LSB.

For the second-order implementation, errors α_2, β_1 and β_2 are dominant because they are multiplied each by $2^{k/2}$. They constitute the fundamental resolution limitation of the proposed structure. Again, due to their position in the conversion flow, α_2, β_1 and β_2 error at the mid-

dle point input range can be canceled with appropriate values. Errors related to β_2 appearing in other positions of the dynamic range are different in term of position and amplitude compared to errors due to α_2 and β_1. So they are not grouped in the summary table.

3.3 Simulations

A model of the proposed hybrid ADC, incorporating the non-ideality parameters used in the above theoretical analysis, was used to validate the proposed linearity errors. In a first step, theoretical non-linearites $(\alpha, \beta, \ldots)$ were introduced in the model. A linear ramp on the whole input range with at least 13 points per LSB is applied on the input. The corresponding output is compared to an ideal ramp to compute INL and DNL.

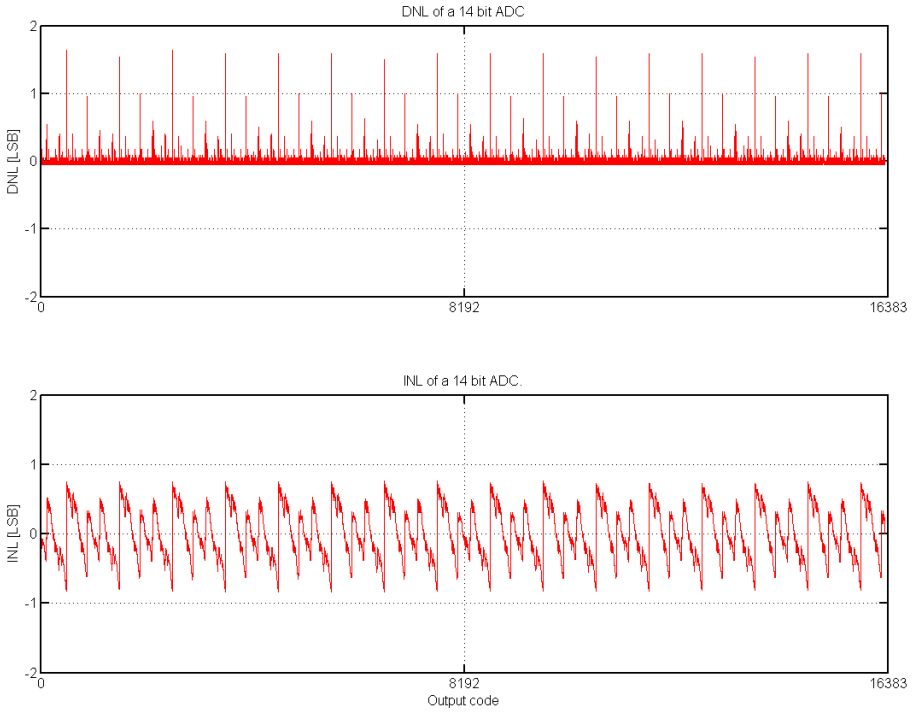

Figure 3.9 : DNL and INL for the first order 14b (4-10) with γ=0.0015.

Figure 3.9 shows a 14 bits converter with the first 4 bits solved by the incremental converter and the last ten by a cyclic one. The error introduced is $\gamma = 0.0015$. The corresponding error predicted by the theory (cf.(3.10)) is 1.54 LSB, which is very close to the one we can observe here (around 1.63 LSB).
On Figures 3.10 and 3.11, the second order incremental is used for the simulation.

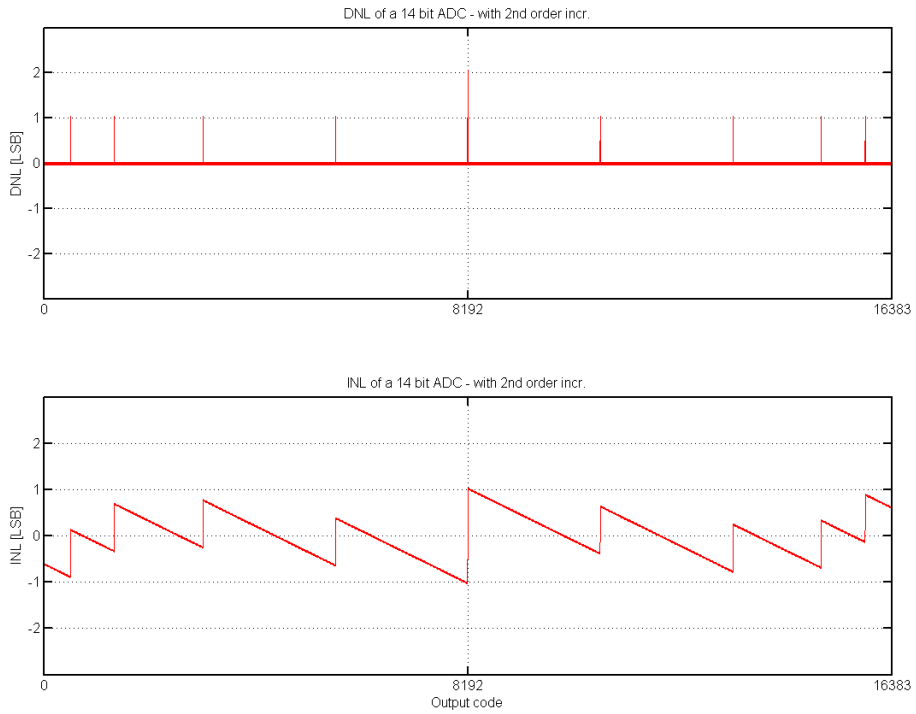

Figure 3.10 : DNL and INL for the second order 14b (4-10) with $\alpha 2$=0.0005.

In a first order, errors appear in a regular way at each transition point, while with the second order incremental converter, the biggest error are always located in the middle of the conversion and minor errors appears at fractional parts of the whole range.

In a second part, the maximal achievable resolution of the first and second order conversion principle was computed. A static switched-

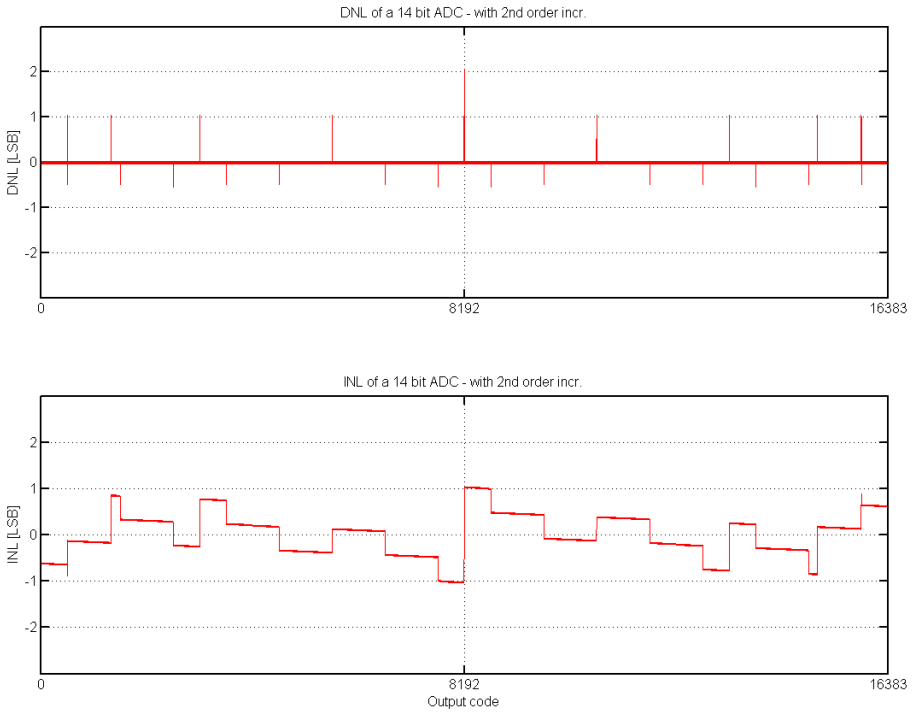

Figure 3.11 : DNL and INL for the second order 14b (4-10) with $\beta 2$=-0.0005.

capacitor model was considered. The different non-idealities were introduced in a MATLAB static-model of the ADC.

- Random offset associated to the OTA amounting to 1% of the full scale of standard-deviation
- Random noise generated in the comparators amounting to 2% of the full scale of white noise
- Parasitic capacitor *Cp* of 20% of the value of the sampling capacitors.
- Limited gain of the OTA to 90 dB

The introduction of the parasitic capacitance and the limited gain of the OTA introduce a gain error in the residue transfer function. If the actual opamp has a finite gain of a and an offset of *Voff* and a

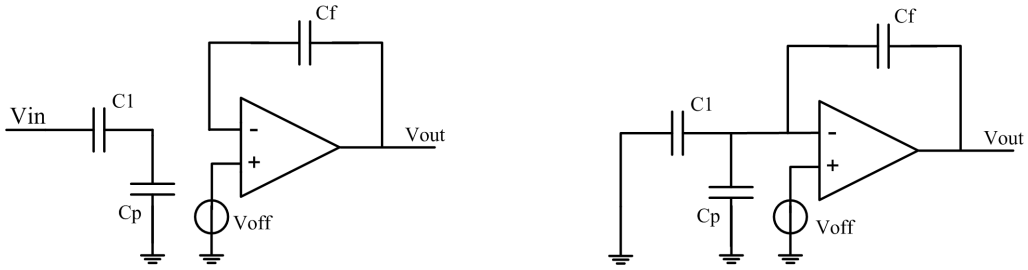

Figure 3.12 : Two phases of a simple integrator scheme. Single-ended is shown for simplicity.

parasitic capacitance *Cp* is added on the common node, then for the simple switched-capacitor of Figure 3.12 the residue transfer function becomes:

$$V_{out} = \left(\frac{a}{a+1+Cp/Cf}\right) \cdot \left[Vin \cdot \left(\frac{C1}{Cf}\right)\right] + Voff \tag{3.24}$$

This error has been taken in account and introduced in the equation that described the conversion. For the capacitance value, three different error Gaussian distributions with standard deviation of 0.1%, 0.3% and 1% were introduced. Charge injection of the switches was not simulated here.

The equations were implemented and simulated with Matlab. An input sine wave was applied to the converter and the result was analyzed with a 4'096-point FFT. The effective number of bits of the converter was deduced from the SNDR computed from the FFT. Fifty runs, each of them with different randomly distributed errors, were performed for each configuration of resolution and each of the three standard deviation levels.

In a first simulation, capacitor mismatch was set to 0.3% and the ENOB was computed in function of the gain of the amplifier. For high gain, the accuracy is limited by the capacitor mismatch and for lower gain, accuracy is limited by the gain itself. A minimal gain of 80 dB

seems to be necessary to avoid limitation by the amplifier.

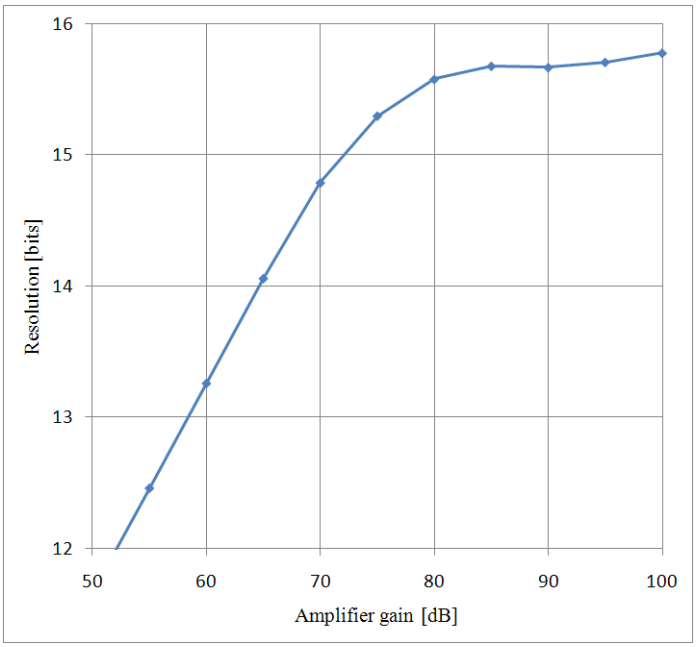

Figure 3.13 : ENOB of converter in function of the gain of the amplifier.

The simulation results are shown in Figure 3.14, where is given the number of conversion cycles in function of the resolution. From all the resolution combinations between first and second stage resolutions (k and n), the plotted structure is the one requiring the minimum number of cycles with a resolution reduced by only half an LSB. As the mismatch level decreases, the conversion is faster because more bits can be resolved by the cyclic stage, much faster than the incremental stage. Conversely, higher mismatch levels require more bits to be resolved by the first stage, thus leading to longer conversions.

For the first-order implementation, Table 3.2 gives the optimal ADC structure (parameter pair $k{-}n$) and the corresponding number of conversion cycles given in 3.1 in function of the desired resolution for the three different error levels and for resolutions ranging from 10 to 18 bit. While 9 bit of resolution can be performed by the cyclic converter with 0.1% mismatch, it decreases to 8-7 bits for 0.3% mismatch and drop

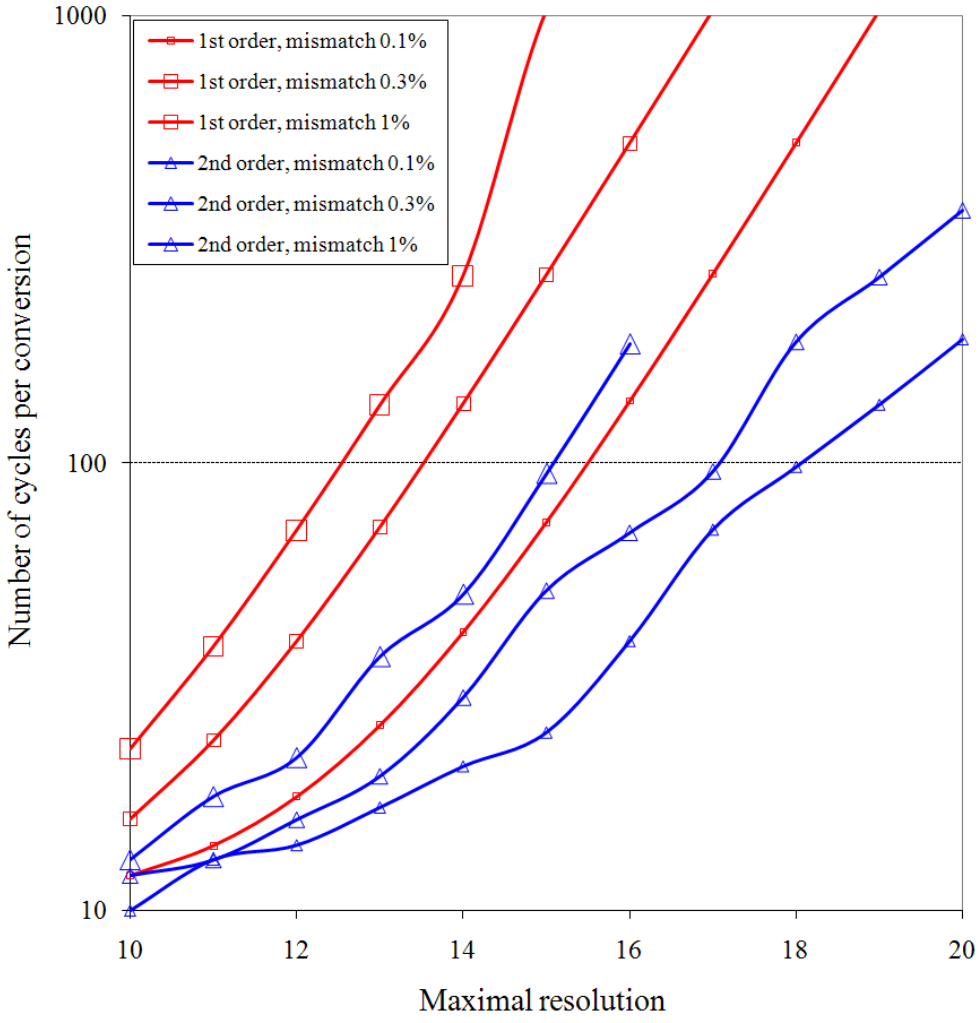

Figure 3.14 : Maximal achievable resolution and corresponding number of cycles per conversion for the proposed principle (1st and 2nd order) when three different error variances of 0.1%, 0.3% and 1%.

to 5-6 bits for 1% mismatch. This affects greatly the number of cycles which is 10 times higher. With a 0.3% mismatch and a 16-bit conversion, the number of cycle is reduced by a factor of 100, while having the same hardware.

	Error 0.1%		Error 0.3%		Error 1%	
	Structure	Cycles	Structure	Cycles	Structure	Cycles
10			2-8	13	4-6	23
12	3-9	18	4-8	25	6-6	71
14	5-9	42	6-8	73	9-5	518
16	7-9	138	9-7	520	11-5	2'054
18	9-9	522	11-7	2'056	14-4	16'390

Table 3.2 : Optimal ADC structure in function of required resolution and error level (1st order implementation)

For the second-order implementation, Table 3.3 gives the optimal ADC structure (parameter pair k-n) exactly like the previous table for resolutions ranging from 12 to 20 bit. While a 16-bit conversion needs only 138 cycles with a 0.1% mismatch level, it needs 2'054 cycles with a 1% level. For this mismatch level, the conversion accuracy cannot be better than 16 bit due to the intrinsic first stage errors. For a typical 0.3% mismatch level, the benefit in terms of conversion time is around 3 compared to a pure second-order incremental converter.

	Error 0.1%		Error 0.3%		Error 1%	
	Structure	Cycles	Structure	Cycles	Structure	Cycles
12	4-8	14	6-6	16	10-2	36
14	8-6	24	10-4	38	12-2	68
16	10-6	40	12-4	70	15-1	185
18	14-4	134	16-2	260	-	-
20	16-4	262	18-2	368	-	-

Table 3.3 : Optimal ADC structure in function of required resolution and error level (2nd order implementation)

If we compare first and second order solutions, we can observe that the second-order always needs a smaller number of cycles to obtain the

same accuracy. Even if the mismatch has a greater influence for the second-order, leading to an increasing use of the precise incremental converter, the benefit given by the second-order shorter conversion cycles is still important. Under 16 bit of resolution the gain in speed is around 2, while complexity is doubled. For a 16-bit conversion, the improvement in speed is around 7 (for a 0.3% mismatch solution).

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Chapter 4

First realization

The first realization is an ADC with a targeted nominal resolution of 16 bit and a conversion frequency of 500 Hz. The design was realized with a UMC 0.18 μm Flash (2 poly, 4 metal) CMOS technology. The supply voltage is $Vcc = 1.65V$ for analog and digital. The input is differential and has a range of $Vcc/4$.

4.1 Proposed implementation

The proposed implementation of the conversion principle is shown in the schematic diagram of Figure 4.1, and is based on switched capacitor circuits. The key idea of this implementation is to use the same hardware for both stages (incremental and cyclic), and operate them in a two-step conversion mode. The circuit has been realized with a first-order incremental converter. It is very compact and requires only one active element, the amplifier.

The ADC has a fully differential structure, and consists of a fully differential OTA, three comparators, eight capacitors (four on each side) and switches. The differential input ($vinp - vinn$) can be inverted with the switch *s40* and the same can be operated for the reference voltage

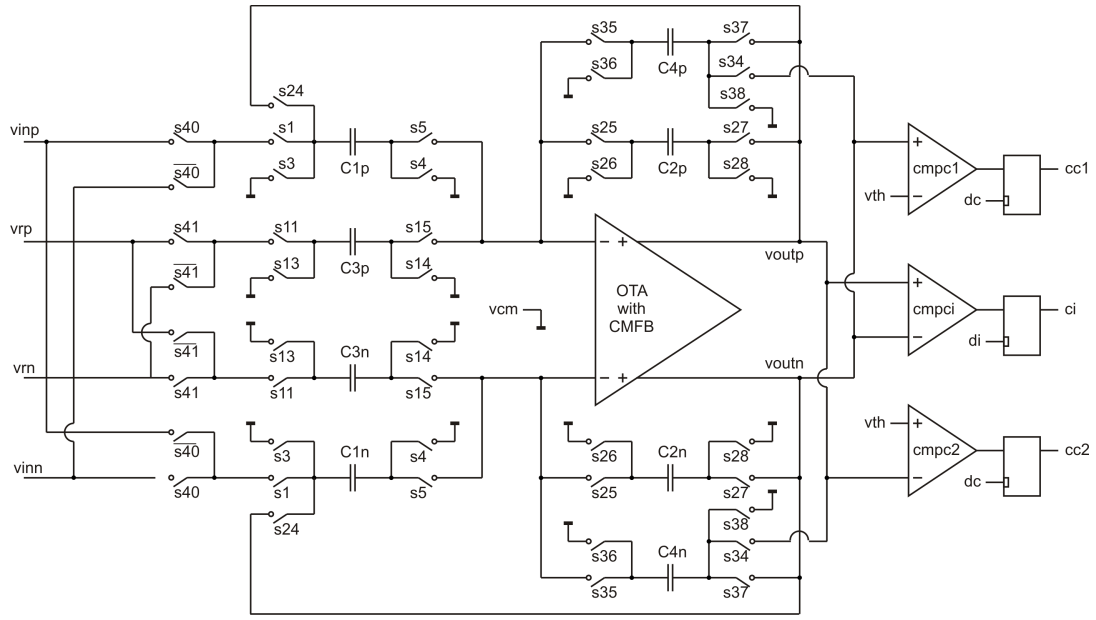

Figure 4.1 : Detailed schematic of the first-order implementation.

(*vrp* - *vrn*) with switch *s41*.

Capacitor *C1* is used to sample the input voltage while capacitor *C3* is used to sample the reference voltage. Capacitor *C2* is the normal feedback capacitor while *C4* is another feedback capacitor used for special operations.

Comparator *cmpci* is used to compare if $voutp > voutn$, in other words if the output voltage is positive or negative. It is used during the incremental mode. Comparators *cmpc1* and *cmpc2* are used to check if the output voltage is bigger, respectively smaller than voltage ($vth - vcm$), respectively voltage ($vcm - vth$). They are used during the cyclic mode. *vcm* represents the common mode voltage.

Incremental mode

The ADC is first used in incremental mode. The next figures shows the schematic with the corresponding timing diagram. All the components which do not appear in the figure are not used.

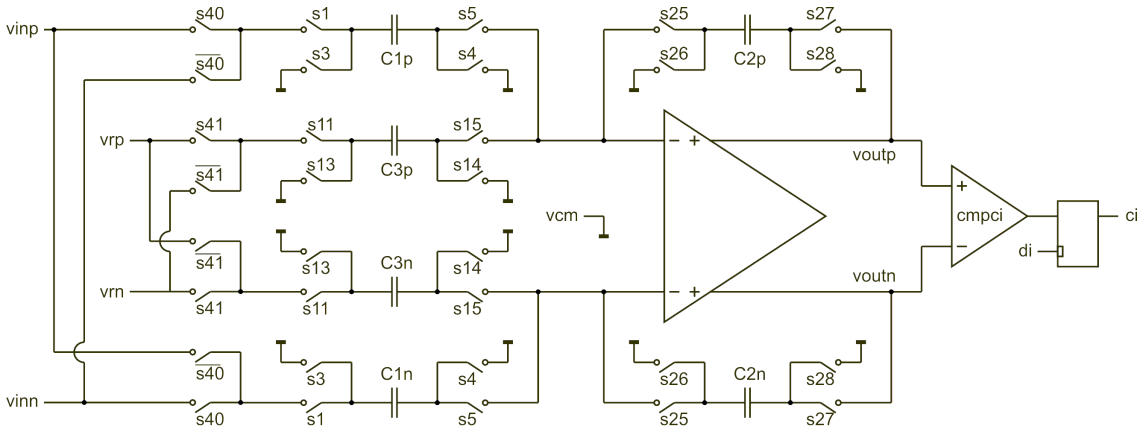

Figure 4.2 : Schematic used in the incremental mode.

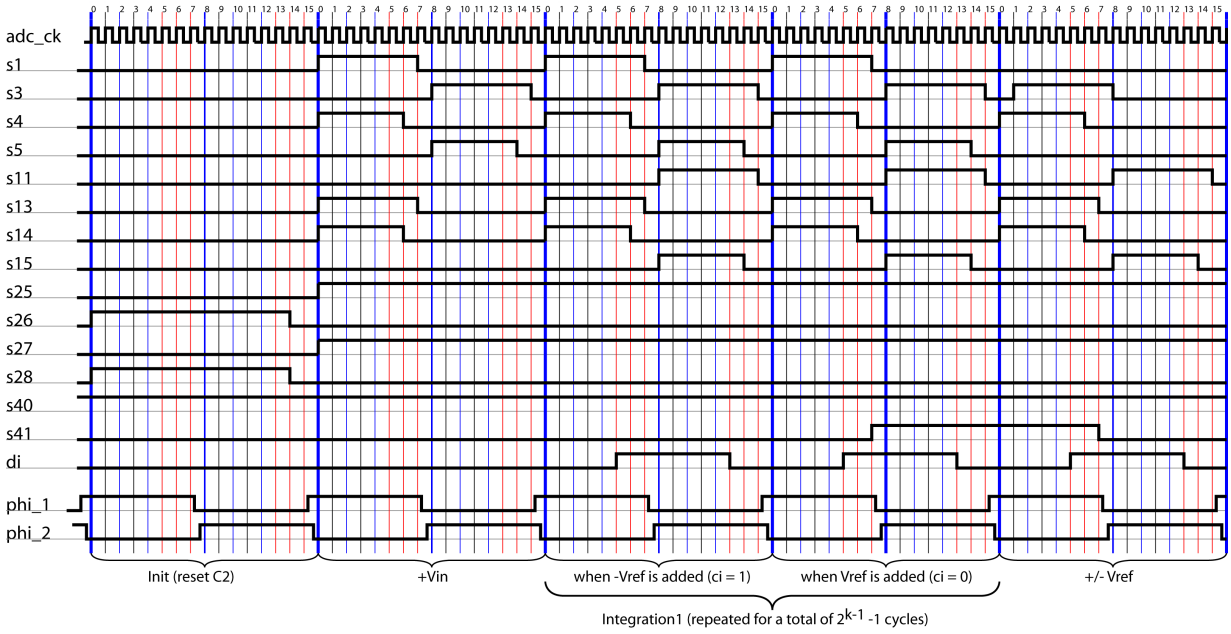

Figure 4.3 : Timing of the integration cycle.

The complete conversion occurs in 6 phases, described below.

Phase A: initialization

During this phase, *C2* is reset through *s26* and *s28*.

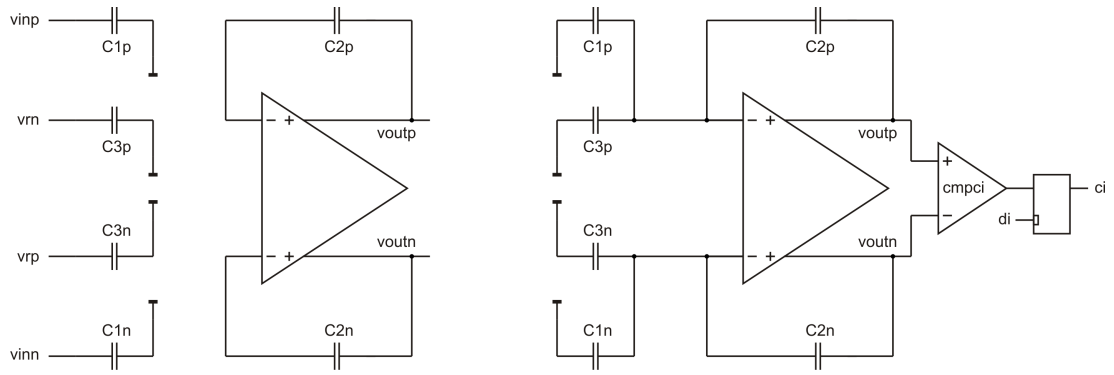

Figure 4.4 : Detailed schematic of the two half period of an integration cycle.

Phase B: positive integration

The incremental conversion begins with 2^{k-1} integration cycles with a positive input voltage ($s40 = 1$), as explained earlier. Each cycle has two steps, shown in the next Figure. In a first step, capacitor *C1* (formed by *C1p* and *C1n*) is charged with input voltage ($vinp - vinn$), and capacitor *C3* (formed by *C3p* and *C3n*) is charged with the positive reference voltage ($vrp - vrn$) if $s41 = 1$, or the negative reference voltage ($vrn - vrp$) if $s41 = 0$. In a second step, the charge of *C1* and *C3* is transferred into the feedback capacitor *C2*. The value of *s41* depends on the comparison result *di* of the previous cycle: if $di = 1$, the output voltage was positive and in this case a subtraction operation of the reference voltage is required, which is done when $s41 = 0$.

The first integration cycle is special, because no reference voltage operation must be performed, which is done by activating *s13* instead of *s11* during the half first period. After 2^{k-1} integration cycles, a final cycle is required to allow the delayed reference voltage operation to take place. For this, no input voltage must be sampled, which is done by

activating *s3* instead of *s1* during the first half period.

The total number of cycles is therefore $2^{k-1}+1$. The comparisons are done at the end of every cycle, except the last one. The number of comparisons N_{pos} is counted with an up-down counter, initialized to zero, and counting as +1 for a positive comparison ($ci = 1$) and −1 for a negative comparison ($ci = 0$). At this point the output voltage $Vout_{I1}$ is equal to:

$$Vout_{I1} = 2^{k-1} \cdot \left(\frac{1}{2} \left(\frac{C1n}{C2n} + \frac{C1p}{C2p} \right) \right) \cdot Vin + N_{pos} \cdot \left(\frac{1}{2} \left(\frac{C3n}{C2n} + \frac{C3p}{C2p} \right) \right) \cdot Vr \tag{4.1}$$

Phase C: inversion of the residue voltage

For analog offset correction, the residue voltage must be inverted between the positive and negative integrations. The residue voltage inversion requires the following operations:

1. Copy of the residue voltage into *C1*, then transfer into *C4*. Reset of *C2*. See Figure 4.5.

2. Copy of the output voltage (*C4*) into *C2*, reset of *C1*, then transfer into *C1*. Reset of *C4*. See Figure 4.6.

3. Copy of the output voltage (*C1*) into *C4*, but with inverted output for voltage inversion, then transfer into *C2*. Reset of *C1*. See Figure 4.7.

Now the inverted input is equal to:

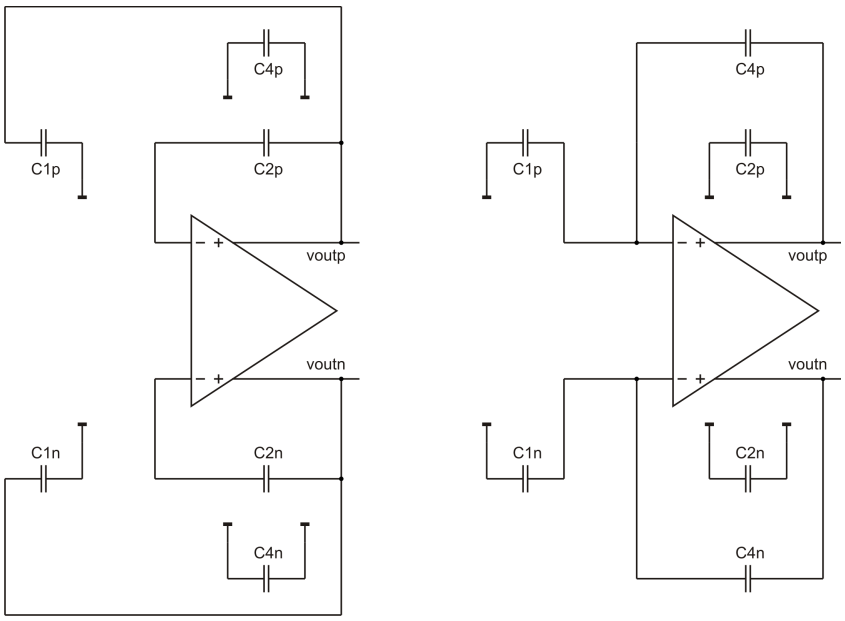

Figure 4.5 : Schematic used during the first cycle of the inversion phase.

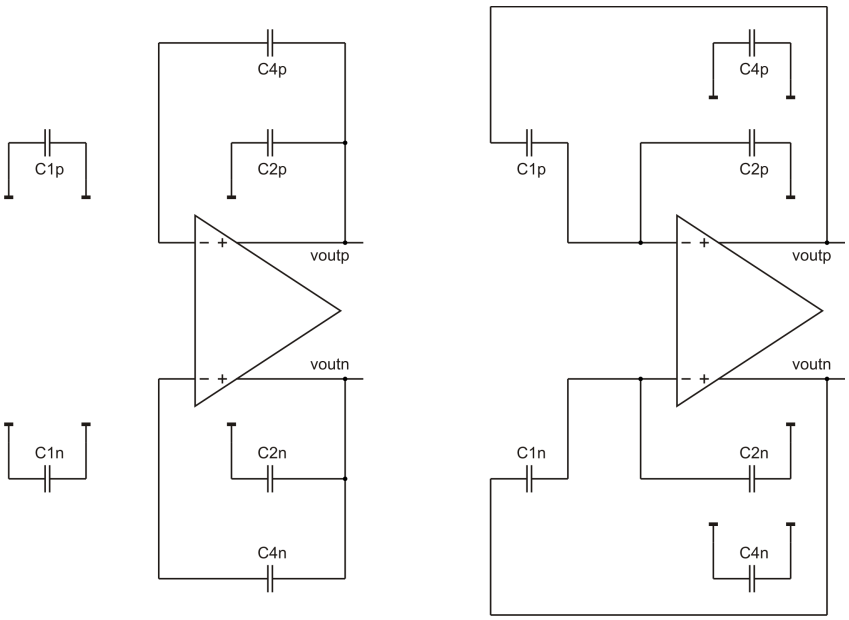

Figure 4.6 : Schematic used during the second cycle of the inversion phase.

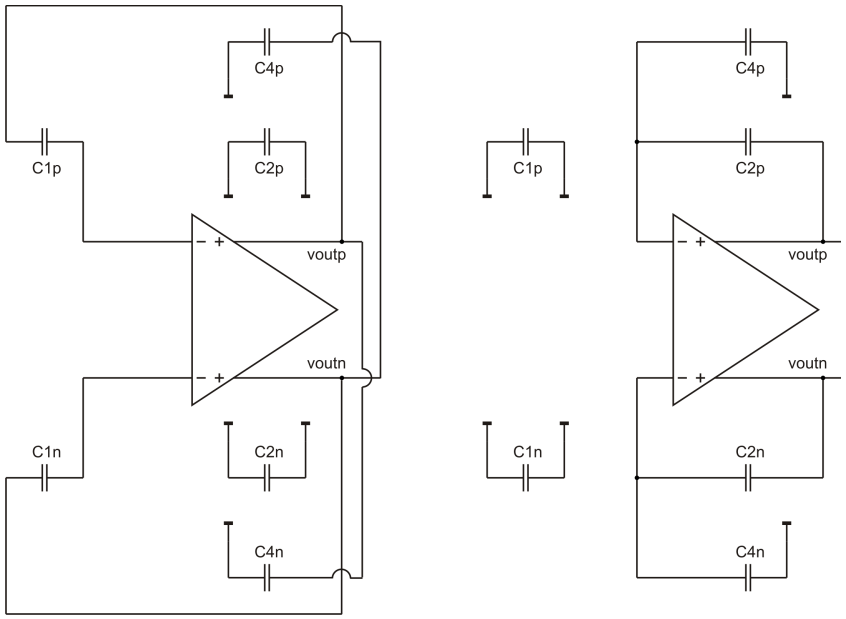

Figure 4.7 : Schematic used during the third cycle of the inversion phase.

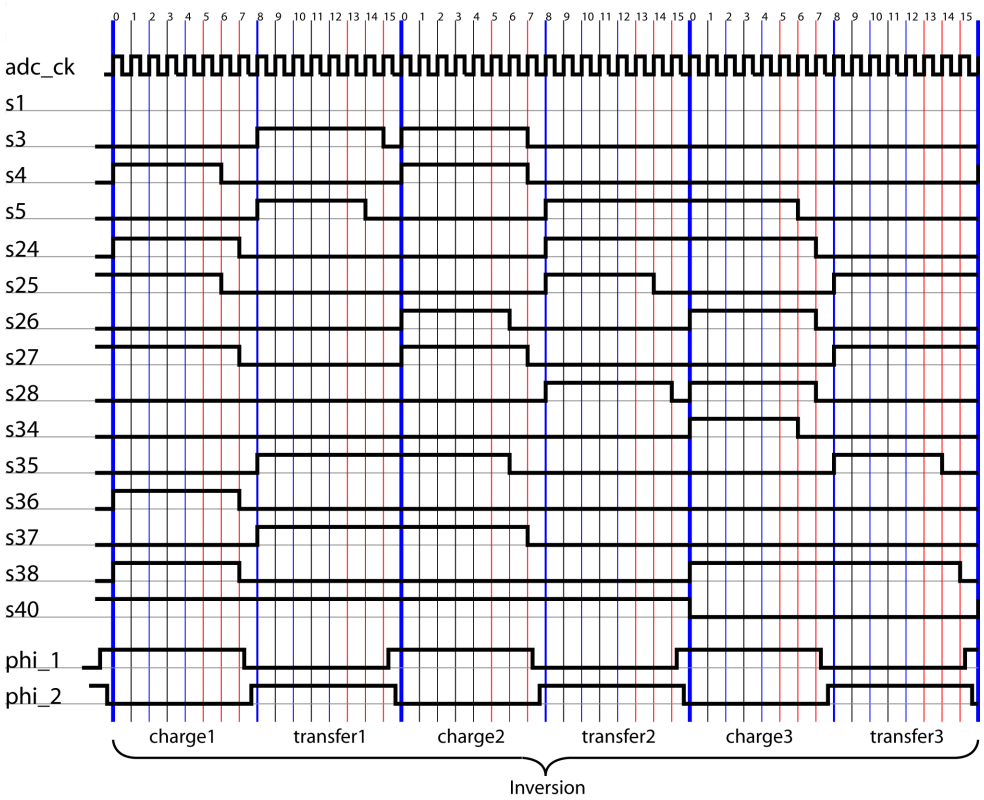

Figure 4.8 : Timing of the inversion cycle.

$$Vout_{INV} = -Vout_{I1} \cdot \frac{1}{8} \cdot \left(\frac{C1n \cdot C4p + C1p \cdot C4n}{C4p \cdot C4n} \right) \cdot \left(\frac{C2n \cdot C1p + C2p \cdot C1n}{C1p \cdot C1n} \right) \cdot \left(\frac{C4n \cdot C2p + C4p \cdot C2n}{C2p \cdot C2n} \right) \tag{4.2}$$

It is theoretically possible to perform this inversion in one cycle rather than three by simply swaping between upper and lower integrating capacitors but in this way the mismatch of the capacitors cannot be compensated.

Considering the first parenthesis of eq. 4.2, we can write the different capacitors as:

$$\begin{aligned} C1n &= (C1 - \Delta C1) \\ C1p &= (C1 + \Delta C1) \\ C4n &= (C4 - \Delta C4) \\ C4p &= (C4 + \Delta C4) \end{aligned} \tag{4.3}$$

and,

$$\begin{aligned} &\left(\frac{C1n \cdot C4p + C1p \cdot C4n}{C4p \cdot C4n} \right) \\ &= \left(\frac{(C1 - \Delta C1) \cdot (C4 + \Delta C4) + (C1 + \Delta C1) \cdot (C4 - \Delta C4)}{(C4 + \Delta C4) \cdot (C4 - \Delta C4)} \right) \\ &= \frac{2C1C4 - 2\Delta C1\Delta C4}{C4^2 - \Delta^2 C4} \\ &\cong \frac{2C1}{C4} \end{aligned} \tag{4.4}$$

First order mismatch cancel each other and only second order mismatch are present. If we make the same consideration for second and

third parenthesis we have an inverted output voltage without first order mismatch.

$$Vout_{INV} = -Vout_{I1} \cdot \frac{1}{8} \cdot \left(\frac{2C1}{C4}\right) \cdot \left(\frac{2C2}{C1}\right) \cdot \left(\frac{2C4}{C2}\right) = -Vout_{I1} \quad (4.5)$$

Phase D: negative integration

The same sequence than for the positive integration occurs, except that the input voltage is inverted thanks to signal *s40*, which is set to 0. The number of comparisons is summed to the count N_{pos} obtained during the positive integration, but this time a positive comparison (*ci* = 1) is counted as -1 and a negative one as $+1$. The total number of cycles is also $2^{k-1} + 1$.

Phase E: extra-cycle

Then, the same hardware is switched to a cyclic RSD converter to perform the second part of the conversion. The corresponding circuit is shown in the Figure 4.9.

The cyclic conversion begins with an extra cycle in which the output voltage is not doubled, but a ternary reference operation is done based on the ternary result of a previous comparison (comparators *cmpc1* and *cmpc2*). The extra cycle sequence is shown in the next Figure, where in the left the OTA output voltage (residue of the incremental conversion) is first copied into *C1*, while *C4* is reset, and *C3* is charged with (+*vr*, 0, -*vr*) depending on the ternary result of the previous comparison. On the right, the charges of capacitors *C1* and *C3* are transferred into *C4*, which becomes the feedback capacitor. *C2* is left unused until the end of the conversion.

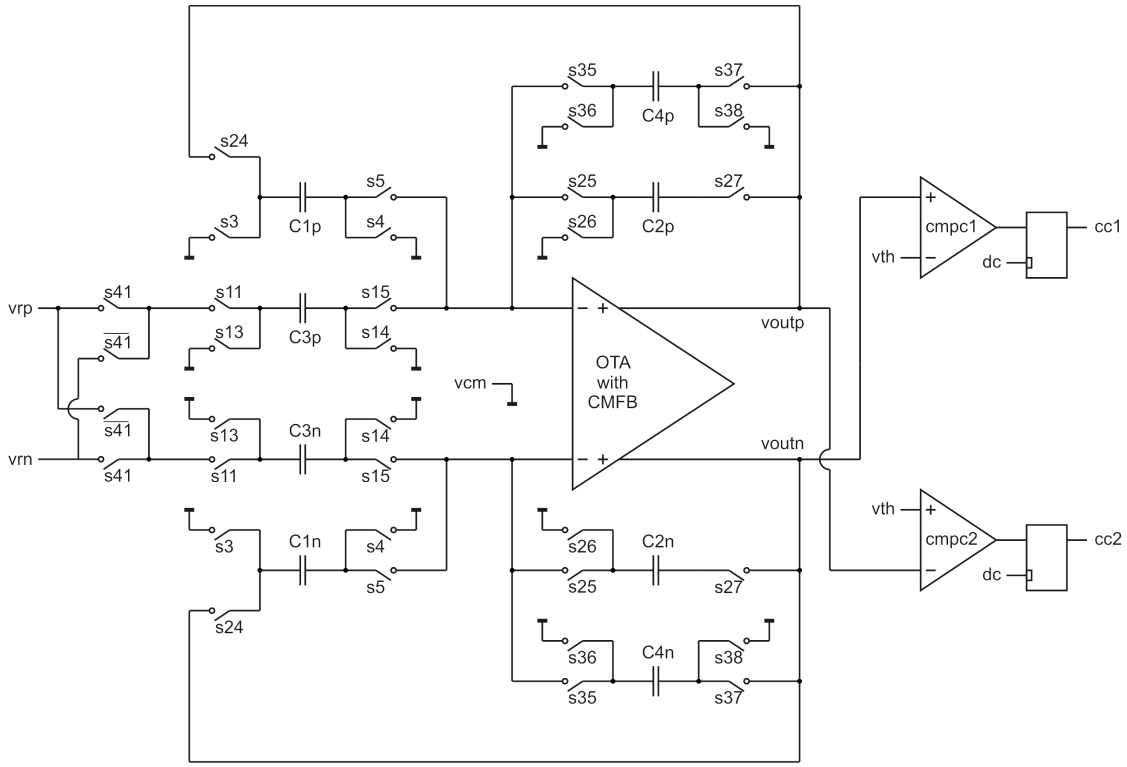

Figure 4.9 : Schematic used during the cyclic phase.

After this first cycle the output voltage is equal to:

$$Vout_{C1} = \left(\frac{1}{2}\left(\frac{C1n}{C4n} + \frac{C1p}{C4p}\right)\right) \cdot Vout_{I2} + d_1 \cdot \left(\frac{1}{2}\left(\frac{C3n}{C4n} + \frac{C3p}{C4p}\right)\right) \cdot Vr \tag{4.6}$$

Phase F: cyclic conversion

The conversion takes then an RSD operation mode, in which *C1* and *C4* are used for doubling, and *C3* for reference operation. *C2* is left unused.

A total number *n-1* cycles are executed after this extra cycle and

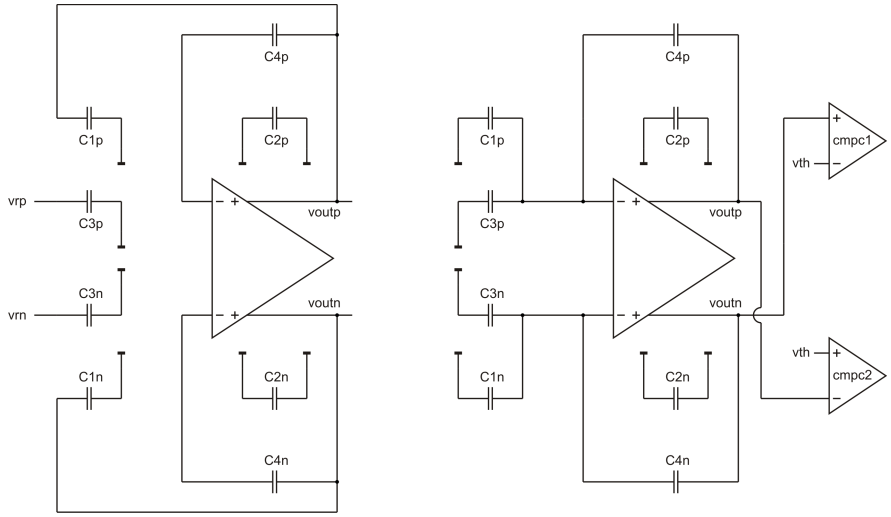

Figure 4.10 : Detailed schematic used during the RSD cyclic phase.

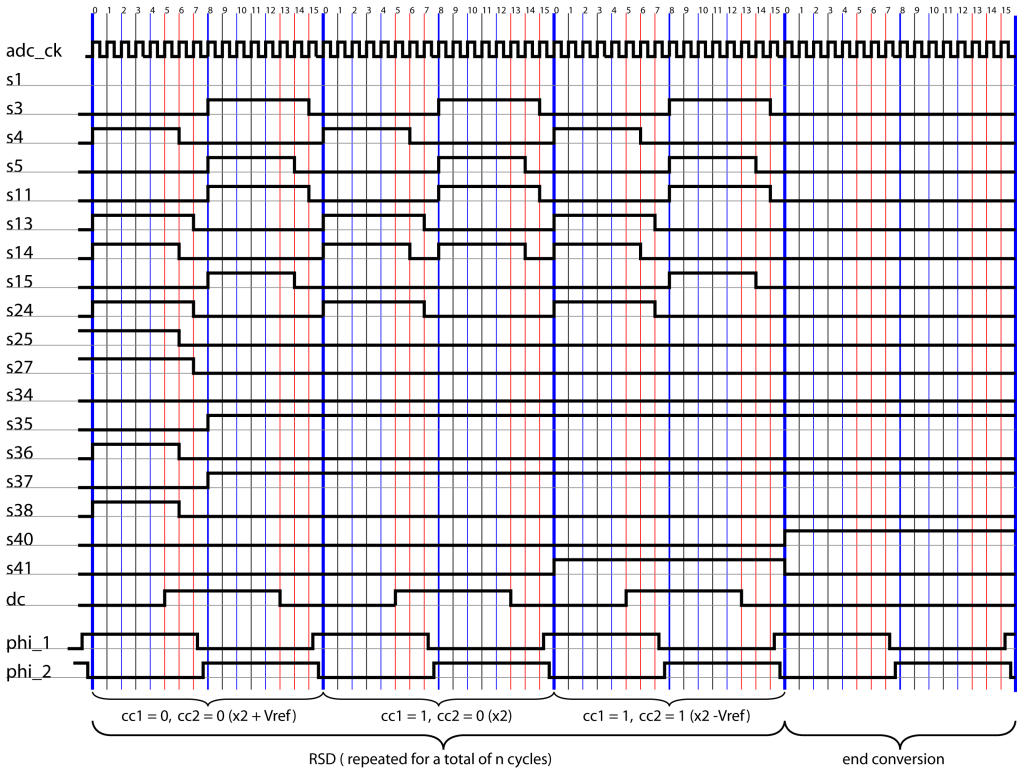

Figure 4.11 : Timing of the cyclic cycle.

the final output is:

$$Vout_{Cn} = \left(1 + \frac{1}{2}\left(\frac{C1n}{C4n} + \frac{C1p}{C4p}\right)\right)^{n-1} \cdot Vout_{C1} + \left(\frac{1}{2}\left(\frac{C3n}{C4n} + \frac{C3p}{C4p}\right)\right) \cdot \sum_{j=1}^{n-1} d_j \cdot \left(1 + \frac{1}{2}\left(\frac{C1n}{C4n} + \frac{C1p}{C4p}\right)\right)^{n-1-j} \cdot Vr \tag{4.7}$$

4.2 Flexible configuration

The ADC features a configurable resolution which can be changed using the following truth table, in which the columns indicate the possible resolutions of the first stage (incremental) conversion, and the rows indicate the possible resolutions of the second stage (cyclic) conversion. On every cell appears on the first line the obtained resolution (in bit), and on the second line the number of ADC cycles for the incremental conversion (on the left) and the number of supplementary ADC cycles for performing the rest of the conversion, i.e. the inversion phase, RSD and extra-cycle phases explained below (on the right). In order to have the total number of cycles for a conversion, the two numbers of the second line must be added.

From all the possible resolution configurations (49 altogether), we distinguish:

- The sub-optimal resolutions (white) for which a simpler ADC principle is advised.
- The over-optimal resolutions (violet) requiring a too good matching.
- The resolutions possible with very good (orange) and good (yellow) mismatch levels.
- The resolutions possible with common mismatch levels (green).

	3 bit	4 bit	5 bit	6 bit	7 bit	8 bit	9 bit	10 bit
4 bit	7 8 11	8 16 11	9 32 11	10 64 11	11 128 11	12 256 11	13 512 11	14 1024 11
5 bit	8 8 12	9 16 12	10 32 12	11 64 12	12 128 12	13 256 12	14 512 12	15 1024 12
6 bit	9 8 13	10 16 13	11 32 13	12 64 13	13 128 13	14 256 13	15 512 13	16 1024 13
7 bit	10 8 14	11 16 14	12 32 14	13 64 14	14 128 14	15 256 14	16 512 14	17 1024 14
8 bit	11 8 15	12 16 15	13 32 15	14 64 15	15 128 15	16 256 15	17 512 15	18 1024 15
9 bit	12 8 16	13 16 16	14 32 16	15 64 16	16 128 16	17 256 16	18 512 16	
10 bit	13 8 17	14 16 17	15 32 17	16 64 17	17 128 17	18 256 17		

Table 4.1 : Resolution modes in function of the desired configuration.

The green zone corresponds to a mismatch level of 0.3%, which is commonly achieved with standard layout techniques. For instance, for achieving a resolution of 16-bit with standard mismatch level of 0.3%, there are many possibilities:

- A conservative configuration with an oversampling ratio of 1024, requiring 1037 conversion cycles followed by 6 bit solved in cyclic.

- A more aggressive configuration with an oversampling ratio of 512, requiring 526 conversion cycles and 7 bit solved by the cyclic.

The orange and yellow zones correspond to mismatch levels of 0.1%, which is achievable only by means of special layout techniques with absolute mismatch minimization. Using such a mismatch level, resolutions of up to 18 bit with oversampling ratios of only 512 is theoretically achievable.
The identification of the possible resolution zones has been done by simulations.

Input range and capacitor ratios

The input range of *vin* has been fixed to be 415 mV around *vcm*. The capacitor ratio between *C1* and *C3* is linked to the reference voltages and input range by the following relation:

$$\frac{C1}{C3} = \frac{vrp - vrn}{vin_{[range]}} \cong 3 \tag{4.8}$$

4.3 Detailed Design

4.3.1 Capacitors

Noise and mismatch requirement determines the capacitor size. The design of the capacitor size involve a trade-off between resolution of the ADC, power consumption and area occupied by the capacitors. If we set a thermal noise much lower than the quantization noise, capacitors sizes are over-dimensioned and power and area is being wasted, on the other side too small capacitors will introduce noise and mismatch and resolution will decrease. Several noise sources affect the resolution and we will consider the following two:

- Thermal noise of capacitor switch (kT/C)
- Thermal noise of the amplifier

Noise of on-resistance of CMOS switches has not been taken into account.

In incremental mode: the ADC is integrating the noise, whose RMS value is therefore divided by the square root of the number of integration cycles.
For the cyclic conversion, the noise is mainly caused by the first cycles, whose signal is amplified by 2 at every following cycle.

The output referred mean square noise of one elementary conversion $v_{no,el}$ is the sum of thermal noise of amplifier and kT/C noise. Referring to [1] we have:

$$v_{no,el}^2 = v_{n,kTC}^2 + v_{n,ota}^2 = \xi \cdot \left(\frac{kT}{C} + v_{n,ota}^2 \right) \cdot G^2 \tag{4.9}$$

where G represents the closed-loop gain of the residue amplification and C the total input capacitance. The constant ξ can assume the value of either 1 or 2 depending on, respectively, whether the circuit is implemented in single-ended or differential configuration.

For the incremental converter, the corresponding input referred noise after the conversion is divided by the square-root of the number of integration cycle, which is 2^k for a k bit resolution.

$$v_{ni,inc} = v_{no,el}/\sqrt{2^k} \tag{4.10}$$

In the cyclic conversion, the total noise referred to the input is the contribution of the different cycles, where the close loop gain G is equal to 2.

$$v_{ni,cyc} = \sqrt{\frac{v_{no,el}^2}{G^2} + \frac{v_{no,el}^2}{G^2 \cdot G^2} + \cdots + \frac{v_{no,el}^2}{G^{2n}}} \cong \frac{1}{\sqrt{3}} \cdot v_{no,el} \tag{4.11}$$

The total input referred noise of the converter is the sum of incremental noise and the cyclic noise referred to the input of the converter (so divided by the gain G_{inc} of the incremental).

$$v_{ni,tot} = \sqrt{v_{ni,inc}^2 + \frac{v_{ni,cyc}^2}{G_{inc}^2}} = \frac{1}{\sqrt{2^k}} \cdot \sqrt{v_{no,el}^2 + \frac{v_{no,el}^2}{3 \cdot 2^k}} \tag{4.12}$$

We can see from (4.10) and (4.11) that the noise is mainly given by the incremental conversion.

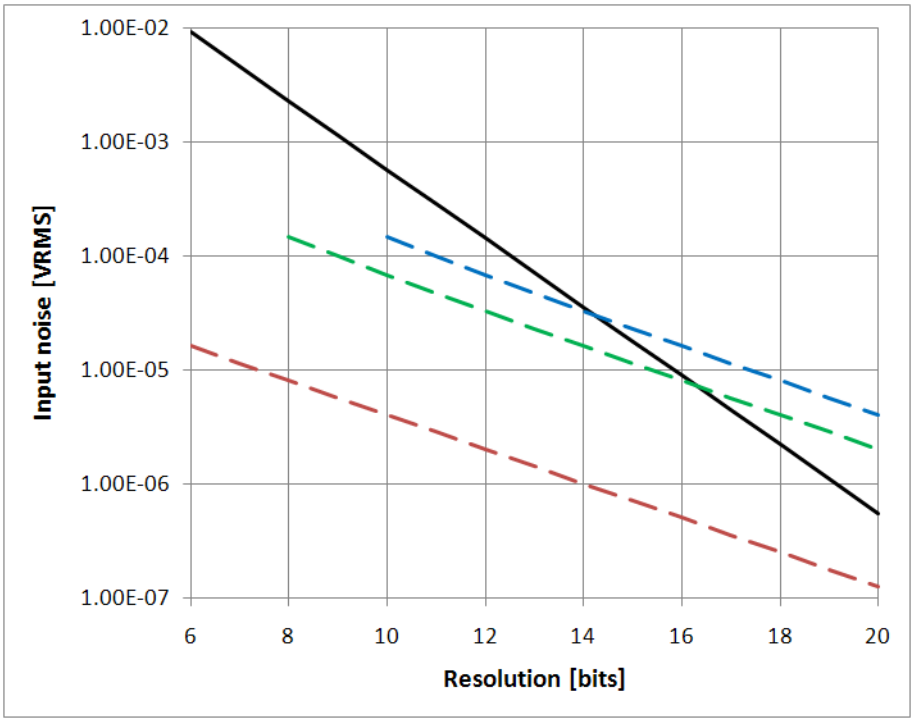

Figure 4.12 : Input noise requirement. In black the maximum allowed input noise. In dashed red the input noise for a pure incremental ADC. In dashed green and blue, the input noise for respectively 8-8 mode and 6-10 mode incremental-cyclic ADC. All configurations with $1pF$ capacitors.

This total thermal noise should be less than the quantization noise. A good compromise is chosen with the quantization noise power four times the total noise power.

$$B_q^2 = 4 \times V_{n,tot}^2 \tag{4.13}$$

In Figure 4.12, configuration with $1pF$ are plotted. With 8 bits solved by the cyclic, it is possible to reach 16 bits of resolution while only 14 bits are obtained with 10 bits solved by the cyclic.

For a configuration of 8 bit solved by the incremental and 8 bit solved by the cyclic, the total thermal noise is 280 μV. We can distribute this overall noise between the different noise contribution and fix to 50% to the capacitor noise and 50% to amplifier noise. This implies a

capacitor of at least $1pF$. In configuration 7-9 and 6-10 the capacitor size is respectively $0.4pF$ and $1.6pF$. A good comproise has been taken with a value of 1.2 pF.

4.3.2 Switches

Two key parameters for the dimensioning of CMOS switches are their conductance and charge injection. Transmission gates have been used to equalize the conductance on the whole input range. Linearity is not optimum with this circuit but this is not an issue. With charge injection, carriers released from the channel are injected on both part of the switch. For switches connected to the high impedance node (input of the amplifier), their charge injection has to be minimized to avoid the charge going on the capacitors. This is realized using almost minimal and equally sized N and P transistors.

The following widths have been chosen for the switches of the circuit (Table 4.2). In order to reduce sub-threshold leakage, all transistors are drawn with a minimal length of 0.24 μm.

	N	P
High impedance node switches	0.5	0.5
Other switches	1.0	2.4

Table 4.2 : Width of the gate of the transistors in μm.

4.4 Amplifier

The proposed structure is a folded-cascode operational transconductance amplifier (OTA). This architecture can easily achieve a large gain (thanks to the cascoding) and has a quite large bandwidth, however

the output swing is reduced. A complementary differential input pair is implemented to provide a rail-to-rail input range. The amplifier is fully differential.

4.4.1 Slewing and settling time

Slewing and settling times are important parameters, which are linked together because they must share together the available time for the OTA to correctly stabilize. This time is given by half a clock period, multiplied by 5/8 because not all the half clock cycle is available (see timing diagram of Figure 4.3) giving us a available time of 1.16 μs.

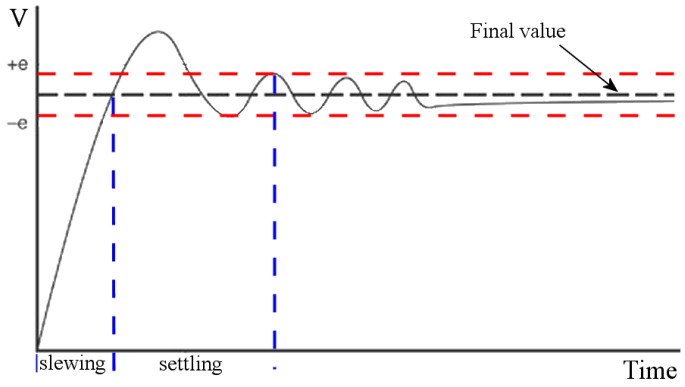

Figure 4.13 : Slewing and settling time.

The transition time is the total of the slewing and settling time.

$$t_{transfer} = t_{slew} + t_{set} \tag{4.14}$$

In our case, we can specify that about 25% (250ns) will be dedicated for slewing and 900ns will be dedicated for settling.

Slewing

The slewing-rate is given by the following formula

$$SR = \frac{\Delta Vout}{t_{slew}} = \frac{I_{Out}}{C_L} \tag{4.15}$$

In our design, the OTA must be able to drive 2.4 pF from $-0.4\,V$ to $+0.4\,V$ within 250 ns, giving a slew rate of 3 MV/s.
In standard output stages, GainBandWidth (GBW) is defined by:

$$GBW = \frac{g_m}{2\pi \cdot C_L} \tag{4.16}$$

where g_m is the transconductance of the input transistor and is equal to

$$g_m = \frac{2 \cdot I_D}{n \cdot U_t \cdot \left(1 + \sqrt{1 + 4 \cdot IC}\right)} \tag{4.17}$$

where IC is the inversion coefficient of the OTA input transistor.
With these relations GainBandWidth and Slew-Rate can be linked by the following equation.

$$GBW = \frac{SR}{\pi \cdot n \cdot U_t \left(1 + \sqrt{1 + 4 \cdot IC}\right)} \tag{4.18}$$

IC is set to 1 and we assume that current Ip is equal to output current $Iout$. We obtain a minimal GainBandwidth of around 8 MHz.

Settling

The relation linking the settling time and the bandwidth of a system is given by:

$$GBW = \frac{\ln\left(1/\epsilon\right) \cdot \beta}{2\pi \cdot t_{set}} \tag{4.19}$$

where the feed-back factor is the closed-loop gain:

$$\beta = \frac{C_{in} + C_{OTA}}{C_f} \tag{4.20}$$

and the term ϵ is the relative settling error. For a 0.25 LSB at 16-bit level precision, we have:

$$\epsilon = \frac{1}{4 \cdot 2^{16}} \tag{4.21}$$

If we set the settling time to 900 ns, we get a GBW of around 4.5 MHz.

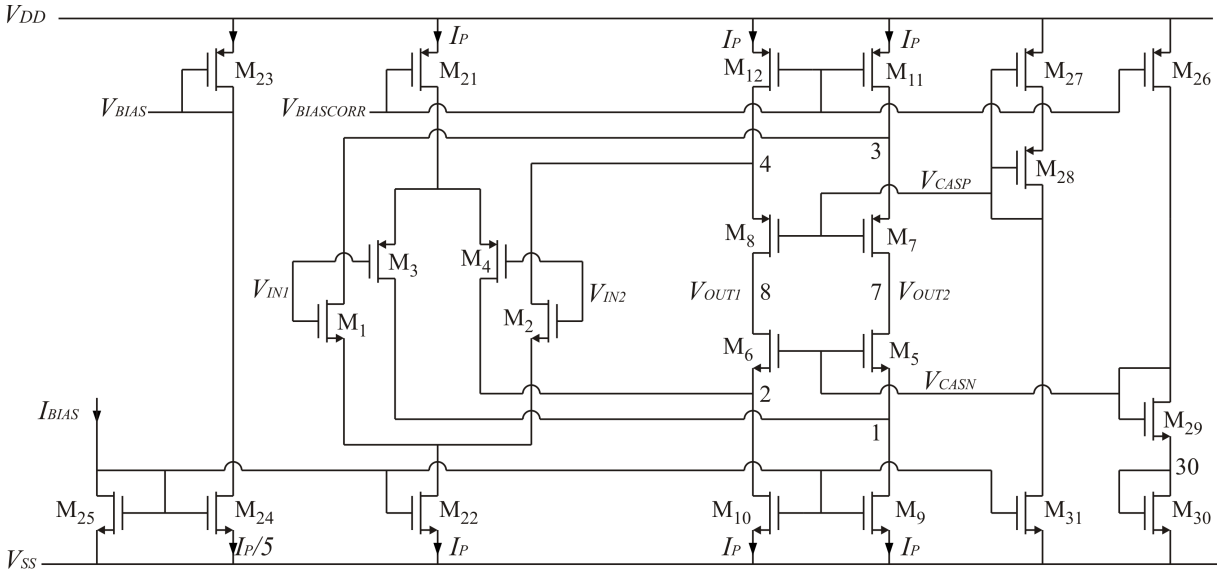

Figure 4.14 : Folded-Cascode amplifier.

4.4.2 Design

M1-M2 and *M3-M4* are the input driver transistors. The cascode transistors are realized with transistors *M5* to *M12*. The bias currents are defined by NMOS *M22* and PMOS *M21*. The common-mode feedback (CMFB) is achieved by controlling the bias voltages of *M21*, *M11* and *M12*.

With the previous specification about GainBandWidth and Slew-rate and the initial specification for the gain, we can determine the value of the various transistors sizes. The ratio of the current were set so that $I(M21) = I(M12)$. The slew-rate requirement gives the minimum value for the current *Ip*.

$$Ip = SR \cdot C_L \tag{4.22}$$

We have chosen a value superior to the specification. *Ip* is set to 25 μA. The minimum length of all mirror transistors is set to 1 μm for matching considerations. The biasing current provided is fixed to 0.5 μA. The transistor *M25* cannot be set in strong inversion because the width would be to small. This one has been reduced to 0.4 μm which implies

an inversion coefficient (IC) of 2.5. The current is multiplied in a first way by ten with *M24*. Thus implies a width for *M24* of 4 μm. In a quite same way the transistor *M23* is set to W/L ratio of 5.

The minimum length for the input transistors is still set to 1 μm also for matching consideration but also to reduce flicker noise influence. The width of the input transistor will determine the GainBandWith of the amplifier with the following equation:

$$GBW = \frac{g_{m1} + g_{m2}}{2\pi \cdot C_L} \tag{4.23}$$

The width of the N input $M1-M2$ is set to 40, while the P input $M3-M4$ is set to 100. Both are working in medium inversion ($IC \cong 1$).

The design of the cascode n and p pair is more tricky. The sizes of the transistor will determine the gain of the amplifier, which is dependent of the resistance seen through transistor *M5* plus *M7*. The use of equations is not so beneficial due to an uncertainty of the determination of the output transconductance g_{ds}. Several simulations are necessary to finely tune the amplifier. The transistor *M9-M10* and *M11-M12* are sized to fix the current *Ip*. Simulations have seen that reducing (W/L) ratio for *M9-M10* increase the performances.

For the biasing structure, the transistor *M31* and *M26* are sized to fix a current of respectively $5\mu A$ and $2.5\mu A$. The transistor *M28* is sized equal as *M8* and *M29* equal as *M6*, and then the remaining transistors (*M12* and *M17*) are designed such as to have a biasing voltage that maximizes the performance of the amplifier. Several simulations are also necessary here to finely tune the structure.

The transistors sizes are summarized in Table 4.3.

Transistor	width [μm]	length [μm]	Id
M1	40	1	25 Ib
M2	40	1	25 Ib
M3	100	1	25 Ib
M4	100	1	25 Ib
M5	10	2	25 Ib
M6	10	2	25 Ib
M7	15	1	25 Ib
M8	15	1	25 Ib
M9	20	1	50 Ib
M10	20	1	50 Ib
M11	14	1	50 Ib
M12	14	1	50 Ib
M21	25	1	50 Ib
M22	20	1	50 Ib
M23	5	1	10 Ib
M24	4	1	10 Ib
M25	0.4	1	Ib
M26	2.5	1	5 Ib
M27	2	3.3	10 Ib
M28	15	1	10 Ib
M29	10	2	5 Ib
M30	3	6.7	5 Ib
M31	4	1	10 Ib

Table 4.3 : Amplifier transistors dimensions.

4.4.3 Noise

Thermal noise

The main contributor of the noise in such a structure are the two differential input stages. As seen on Chapter 2 the thermal noise density in a transistor is equivalent to:

$$i_{nth}^2 = (8/3) \cdot g_m \cdot k \cdot T \tag{4.24}$$

where g_m is the small-signal transconductance. We can get the equivalent

input-mean-square voltage-noise with:

$$v_{nth}^2 = \frac{i_{nth}^2}{g_m^2} \tag{4.25}$$

and we obtain $2.95 \cdot 10^{-17} V^2/Hz$ for the NMOS and $7.45 \cdot 10^{-17} V^2/Hz$ for the PMOS. The two noise densities must be multiplied by 2 and added to get the total noise density of $2.08 \cdot 10^{-16} V^2/Hz$,
which correspond to $14.4 nV/\sqrt{Hz}$.

We must integrate the noise density over the bandwidth of the amplifier and then take the square root to get the total RMS thermal input noise:

$$V_{nthRMS} = \sqrt{2 \cdot \int_0^{GBW} v_{nth}^2 \cdot df} = 105 \mu V_{RMS} \tag{4.26}$$

Flicker noise

The flicker noise (or *1/f* noise) density can be calculated using the following formula:

$$i_{n1f}^2 = \frac{KF \cdot I_D}{C_{OX} \cdot L^2 \cdot f} \tag{4.27}$$

where KF is a flicker noise coefficient given by the technology, C_{OX} the gate oyxde capacitance, L the length of the transistor and f the frequency.
The flicker noise has been calculated for the four input transistors. In a same way as for the thermal noise, the equivalent input-mean-square current-noise can be reflected to the gate by dividing by g_m^2:

$$v_{n1f}^2 = \frac{i_{n1f}^2}{g_m^2} \tag{4.28}$$

For the NMOS we obtain $8.5 \cdot 10^{-13} V^2/(f \cdot Hz)$ and $2.17 \cdot 10^{-11} V^2/(f \cdot Hz)$ for the PMOS, which give a total flicker noise of $4.5 \cdot 10^{-11} V^2/(f \cdot Hz)$.

The noise corner, where the thermal noise is equal to *1/f* noise can

be found by:

$$f_c = \frac{v_{n1f}^2}{v_{nth}^2} = 216kHz \tag{4.29}$$

To estimate the RMS flicker noise, we must integrate from f_{op}=500 Hz (frequency of the conversion, which has an offset correction compensating the flicker noise below that frequency) up to the noise corner.

$$V_{RMS}^2 = \int_{f_{op}}^{f_c} \frac{v_{n1f}^2}{f} df = v_{n1f}^2 \cdot \ln\left(\frac{f_c}{f_{op}}\right) = 2.7 \cdot 10^{-10} (V_{RMS})^2 \tag{4.30}$$

which corresponds to 16.5 μV_{RMS}. This noise remain indicative, as (4.27) is based on empirical models, and accuracy is sometimes questionable. We have taken into account only the input transistors. If we sum the thermal and flicker noise, we obtain around 106 μV_{RMS}.

4.4.4 Simulation

AC Simulations

The following AC simulations were performed, using in all cases a load of 1.6 pF (maximal capacitor load taking into account process variations) on each output node, and a voltage supply of 1.65 Volt. Since the OTA is a 1-stage system, there is no concern about stability. The current can vary because of process variations only, by a maximum of $\pm 30\%$.

Case A: typical conditions
Case B: fast-fast corner in fast conditions, low temperature
Case C: fast-fast corner in fast conditions, high temperature
Case D: slow-slow corners in slow conditions, low temperature
Case E: slow-slow corners in slow conditions, high temperature
Case F: fast-n-slow-p corners in slow conditions, low temperature
Case G: fast-n-slow-p corners in fast conditions, high temperature

Case	Model	Temp $[°C]$	Bias Current $[\mu A]$	DC gain $[dB]$	GBW $[MHz]$	Phase Margin $[deg]$
A	tt	+27	1.0 (nominal)	85.3	24.6	82
B	ff	−20	1.0	85.4	26.5	82
C	ff	+85	1.3	85.1	27.9	81
D	ss	−20	0.7	84.7	19.5	83
E	ss	+85	1.0	86.1	22.3	81
F	fnsp	−20	0.7	85.2	19.1	83
G	fnsp	+85	1.3	84.2	27.4	81
H	snfp	−20	0.7	85.2	19.8	83
I	snfp	+85	1.3	84.1	28.5	81

Table 4.4 : Amplifier corner simulations.

Case H: fast-p-slow-n corners in slow conditions, low temperature
Case I: fast-p-slow-n corners in fast conditions, high temperature
The typical scenario (A) is plotted in Figure 4.15.

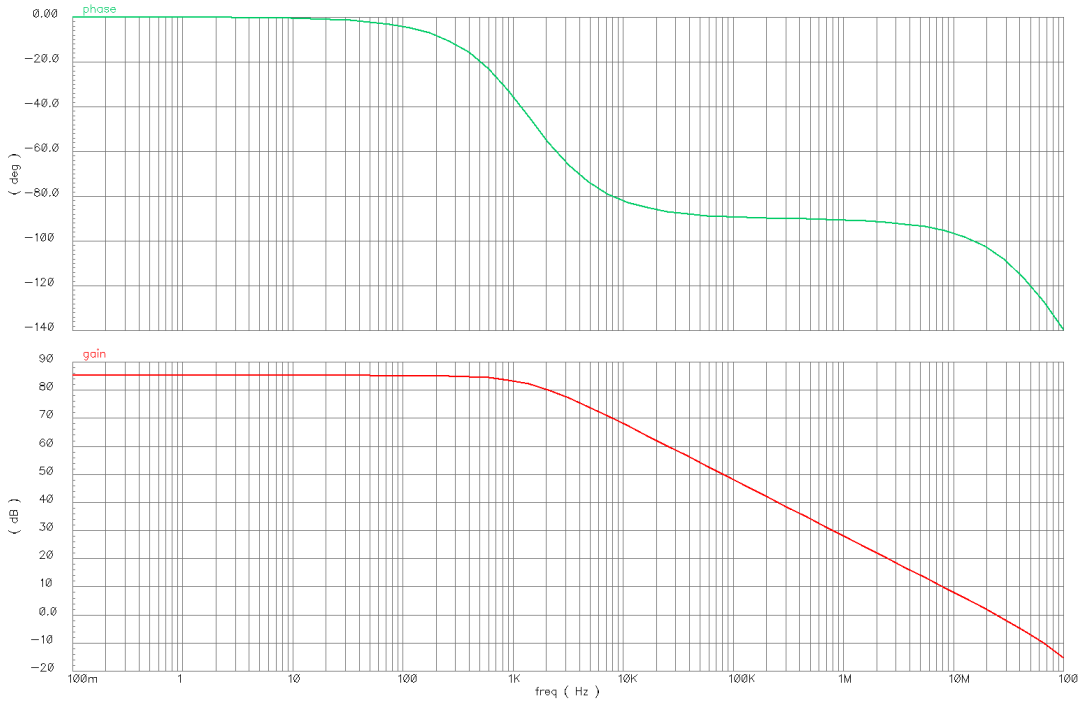

Figure 4.15 : Amplifier performances.

Noise simulations

The thermal input referred noise density of the OTA has been simulated with Spectre in function of the frequency and is shown in Figure 4.16. We see that the density of about $9.7nV/\sqrt{Hz}$ is in the same order of magnitude than what has been calculated: $14.4nV/\sqrt{Hz}$. The thermal noise contribution is thus equivalent to $72\mu V_{RMS}$.

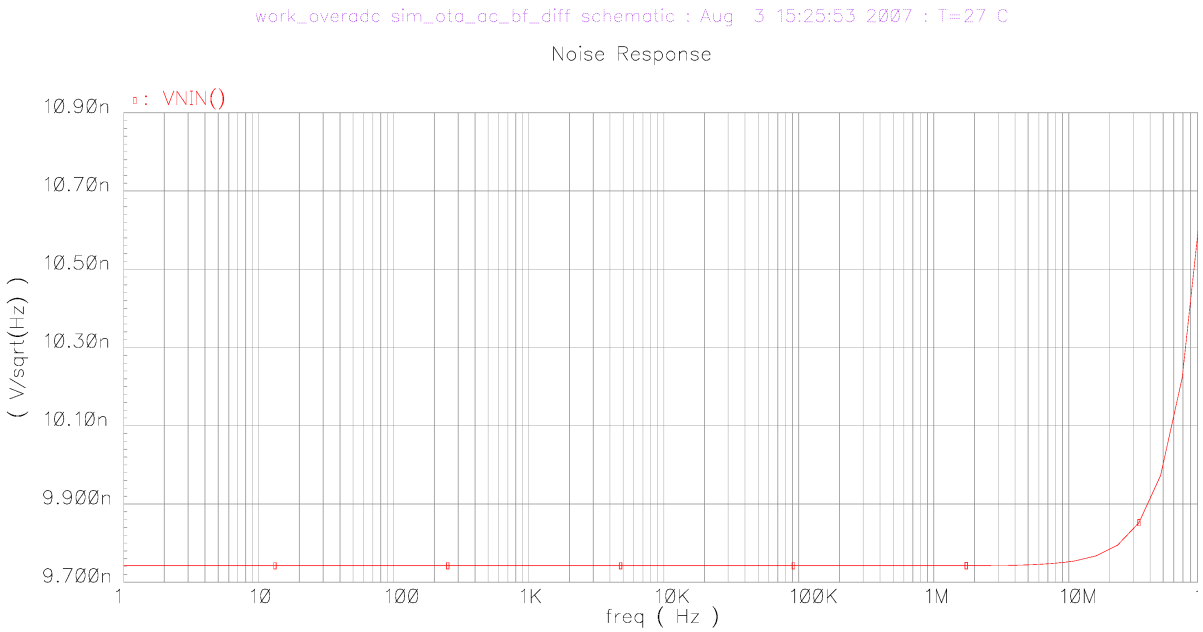

Figure 4.16 : Amplifier input referred thermal noise density.

Figure 4.17 shows the same simulation including the flicker noise. We see that the corner frequency is around $200kHz$. The integration of this noise density from $500Hz$ to $200kHz$, give a value of 5 μV_{RMS}, which is 3 times smaller than the one we calculated. The major part of the noise is thermal noise and flicker noise is negligible. On the next table a resume of calculated and simulated noise is presented.

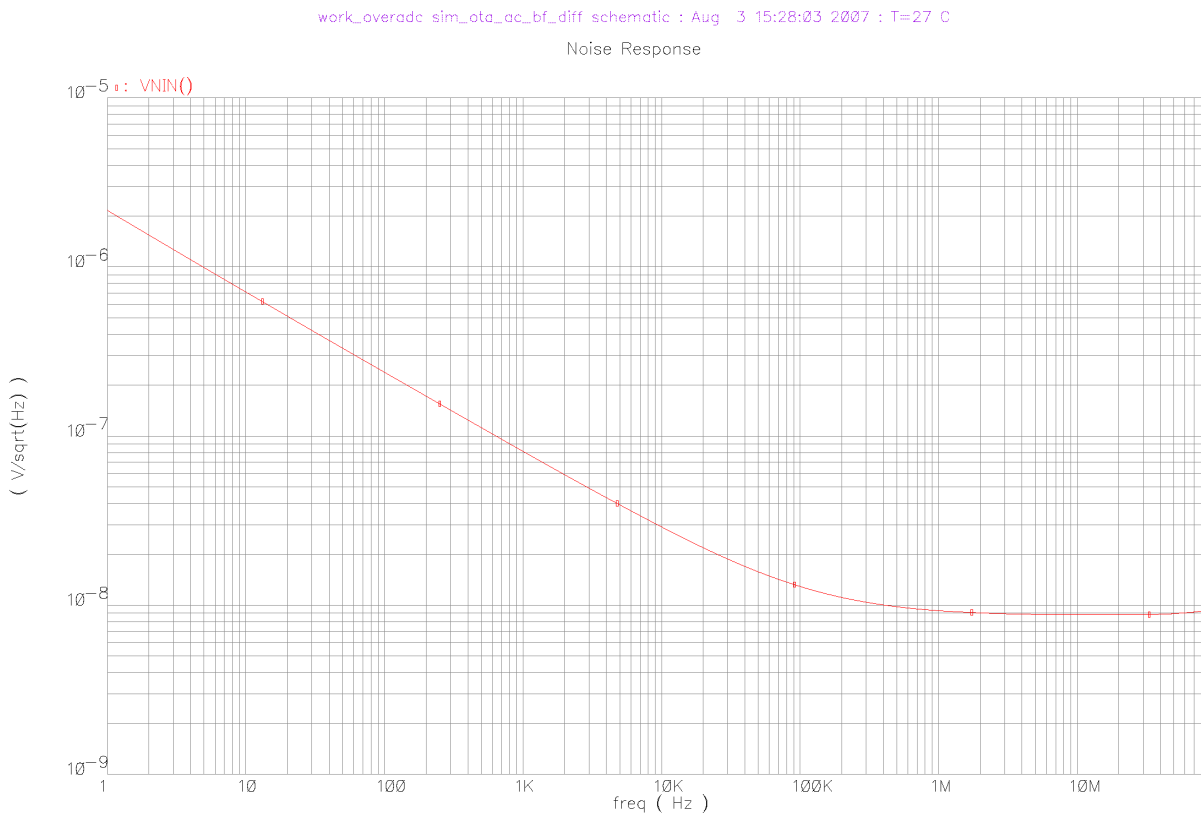

Figure 4.17 : Amplifier input referred noise including flicker noise.

	Calculated	**Simulated**
Thermal	105	72
Flicker	16.5	5
Total	106	72

Table 4.5 : Amplifier Noise.

4.5 CMFB

In a fully-differential amplifier, a common-mode feed-back (CMFB) is needed to define the DC voltage at the output nodes. A dynamic switched-capacitor CMFB is selected for low-power consumption and no restriction on the maximum differential output signals values. A fully mathematical description can be found in [2].

Figure 4.18 shows the CMFB implementation. The matched capacitors *C2* form a capacitor divider used to average the differential output. During $\phi 1$, capacitor *C1* are precharged to the bias voltage *vbias*. During $\phi 2$, *C2* is switched in parallel with *C1*, so to add a correctional DC offset voltage on *vbiascorr*. As *vbiascorr* changes, the gatesource voltage of transistors changes, which in turn, changes the current sunk by these transistors, canceling the variation of the output common-mode. All the capacitors are 0.5 pF and the switches are made with transmission gate. $\phi 1$ and $\phi 2$ are non-overlapping clock signals.

An on-chip non-overlapping clock generator generate the clock phases from an external clock.

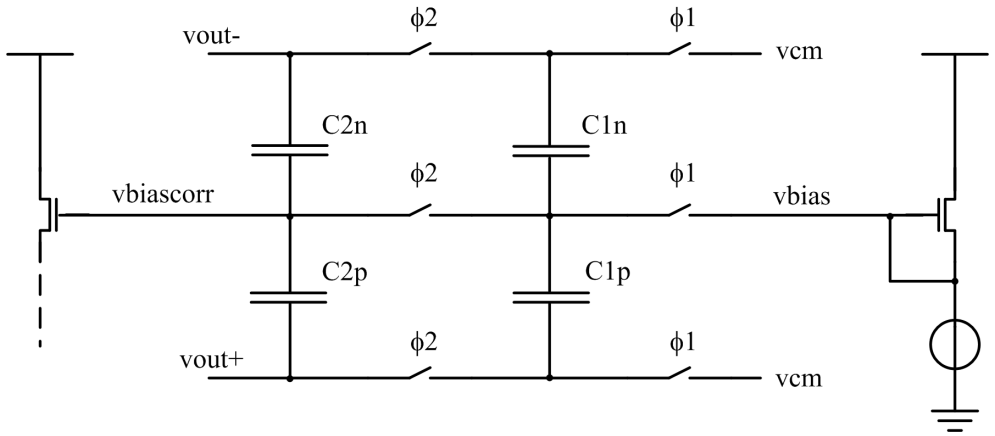

Figure 4.18 : CMFB implementation.

4.6 Comparators Design

The comparators do not need to be very accurate for the following reasons:

- In incremental mode, any comparison error leads to an analog difference which can be fully sensed by the subsequent cyclic conversion thanks to the extra-cycle over-range capability.

- In cyclic mode, any comparison error can be corrected without loss of linearity thanks to the properties of the RSD conversion.

4.6.1 Schematic

The comparators are therefore simple dynamic comparators (latched). Figure 4.19 show the schematic of the comparator. The latch operation is composed of 2 phases:

- Reset phase: logic control signal latch is '1', both outputs are reset to '1' through MP3 and MP4. The inputs are separated from the outputs by MN3 and MN4.
- Set phase: control signal latch is '0'. MN1 - MN2 and MP1 - MP2 consists a dynamic range, the outputs is defined by inputs.

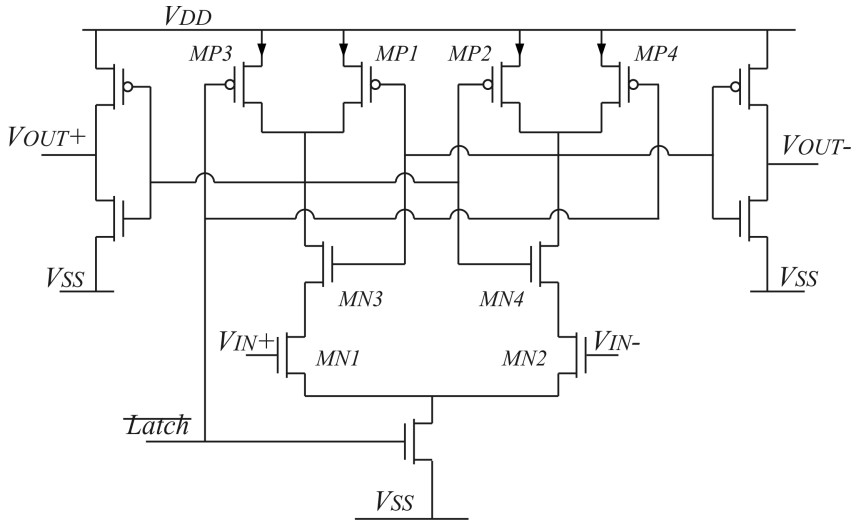

Figure 4.19 : Schematics of dynamic latch.

4.6.2 Connecting

Normally, the comparison voltages must be located at *vcm* for the incremental conversion (comparator *ci*), and at *vcm* + *vth* (comparator

cc1) and *vcm - vth* (comparator *cc2*) for the cyclic conversion, *vth* being about *vref/4*. Therefore, three threshold voltages would be normally required. However, the differential structure allows to get rid of one threshold for the cyclic conversion, applying the connecting schematics of the next Figure. With this, only one threshold voltage (*vth*) must be generated, the other one (*vthp*) being virtually generated by using the complementary OTA output for performing the comparison (*voutn* instead of *voutp*).

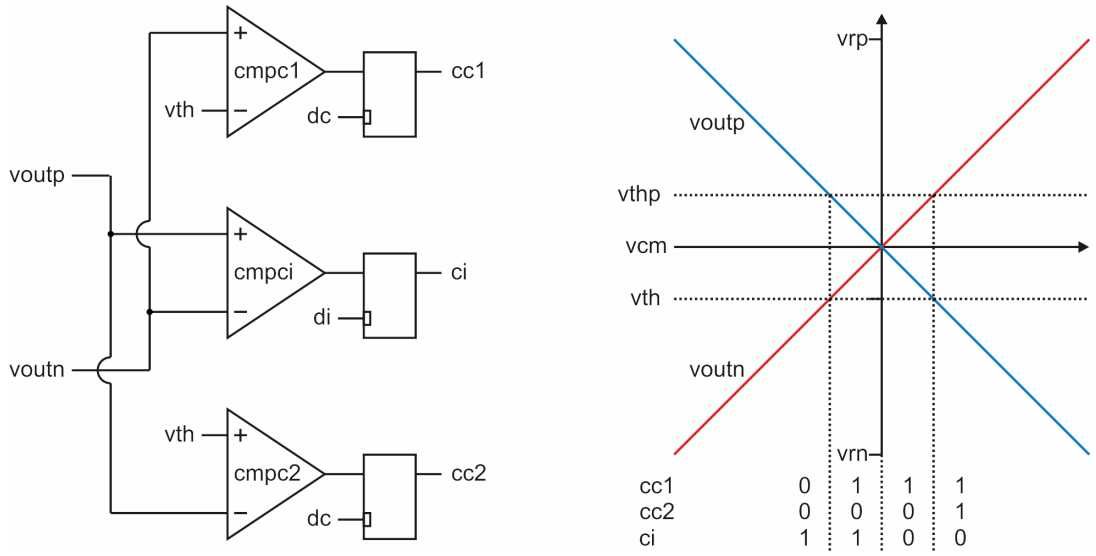

Figure 4.20 : Connecting the comparators.

The threshold voltage has to be generated on-chip. A capacitor divider circuit is implemented as shown in Figure 4.21 to create the threshold voltage *Vth*. It is clocked by signal $\phi 1$ and $\phi 2$ which are non-overlapping clocks. The capacitors *C1* and *C2* are respectively 50 fF and 420 fF and act as a capacitor divider. Capacitor *C3* is 540 fF and is operated as a memory during phase $\phi 1$.

Simulation of the threshold is shown in the Figure 4.22. A few microseconds are necessary to stabilize the output.

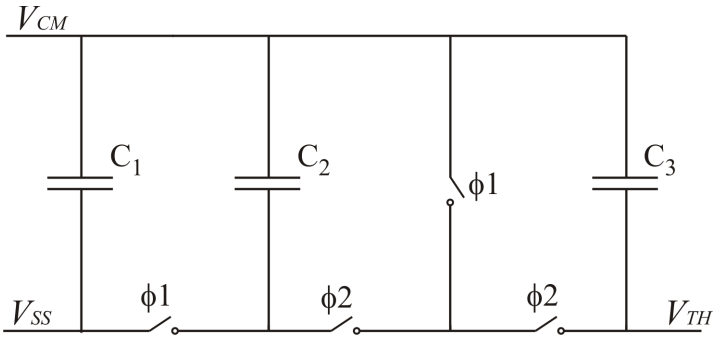

Figure 4.21 : Schematic of the circuit for Vth generation.

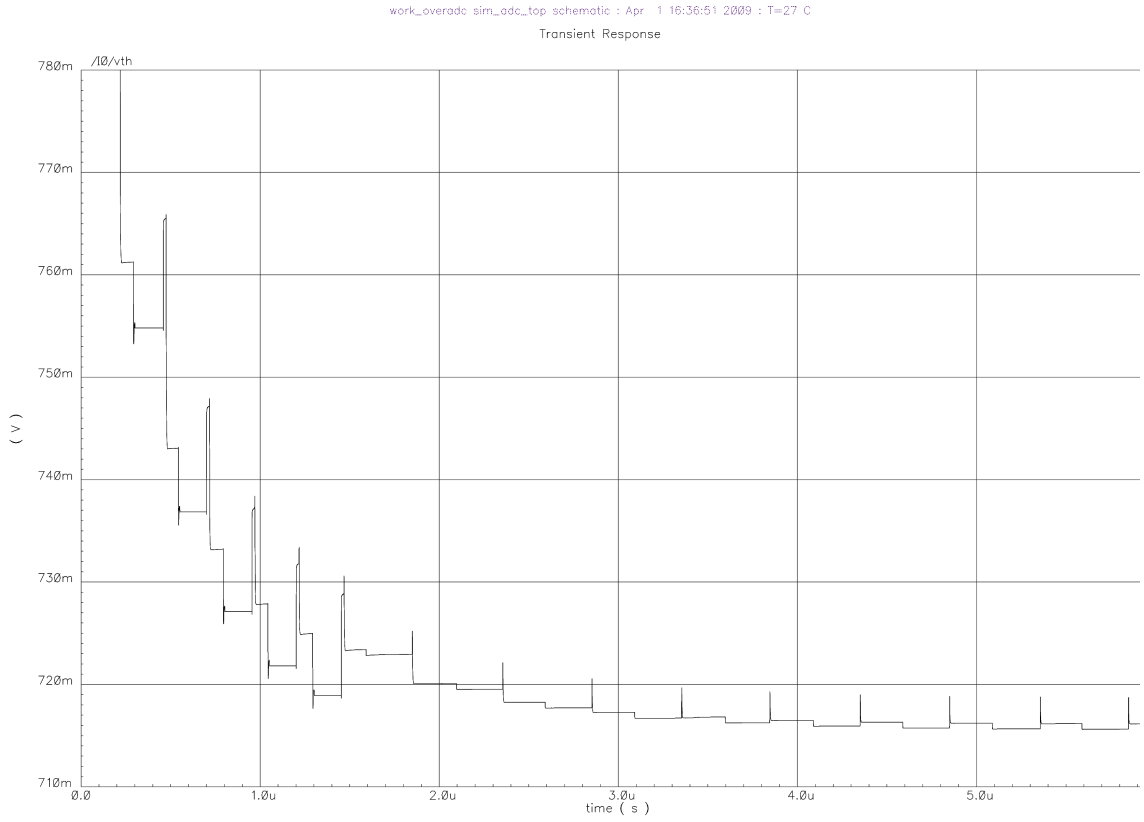

Figure 4.22 : Simulation of the threshold voltage.

4.7 Digital design

The ADC logic is described in VHDL. Its purpose is to:

- Control the overall operation of the ADC (modes, resolution, etc.).
- Generate the signals for the 44 switches of the ADC.
- Collect the bit stream from the comparators and convert it into an integer value.

The main clock frequency is 4.288 MHz. This clock is divided by 16 to provide a slower clock (*adc_ck* at 268 kHz) that will be used as reference for one cycle. The high frequency clock is used to create delays between opening or closing of some switches.

4.7.1 States

Two main operation modes are running depending on an enable signal:

- INACTIVE: All clocks are switched off.
- ACTIVE:

In the ACTIVE mode, a finite state machine is implemented to perform the conversion.

- IDLE: this is the state after a reset or after a conversion. In this state, all signals going to the ADC are at 0, except control signals *s25*, *s26* and *s41* which are at 1, ensuring that the OTA inputs are connected to *vcm*, which is a correct input voltage for CMFB operation.

- RESET: this is the state after a reset or after a conversion. In this state, the OTA inputs are connected to *vcm* and capacitor *C2* is reset via *s26* and *s28*.
- INTEGRATION1: Positive integration. The length of this state depends on the configuration value (see Table 4.1), and is a multiple of 16**adc_ck* cycles.
- INVERSION: Inversion of the residue. Lasts for 3*16 *adc_ck* cycles.
- INTEGRATION2: Negative integration.
- RSD: Cyclic conversion.
- READY: at the very beginning of this state is issued the *adc_ready* signal (duration: 1 *adc_ck* clock cycle) during when the output result is updated.

4.8 Layout

The layout of the analog part is shown in Figure 4.23. We have a totally symmetrical structure regarding switches, capacitors and their routing wires. All analog connections are done from the left, and all digital connections are on the right side. Maximal shielding between analog and digital signals has been implemented using Met2 or Met3. The overall size is 303 μm x 346 μm, representing an area of 0.105 mm^2.

We have three capacitors of nominal value and capacitor *C3* that have a smaller value. The capacitors have been carefully drawn for maximal matching and minimal coupling with other nets, such as the bulk or digital nets. An array of 4 x 4 capacitors of 0.3 pF each has been drawn with dummy capacitors. For drawing *C1*, *C2* and *C4* (1.2 pF), three capacitors are connected together using equal length connections

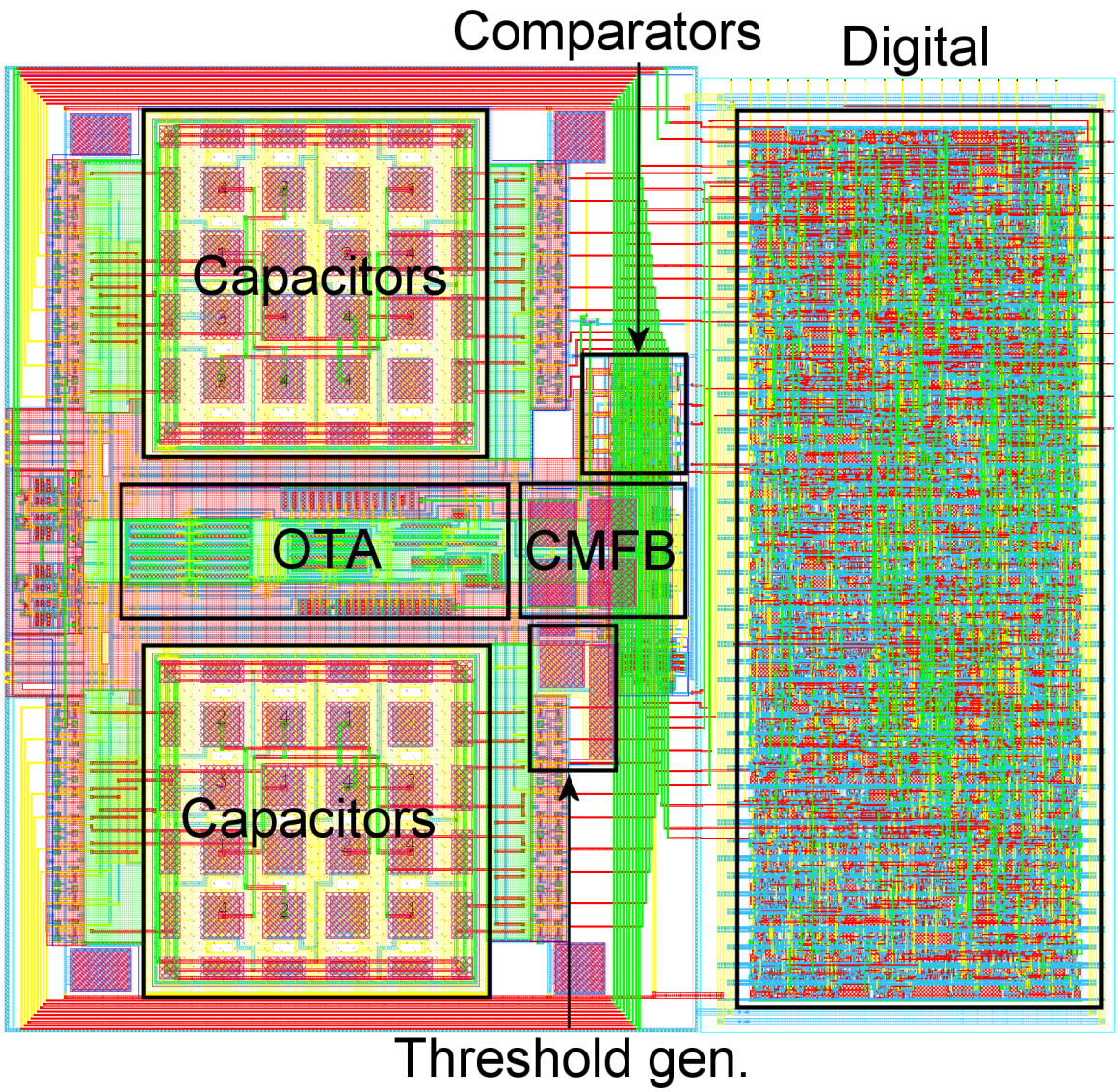

Figure 4.23 : Layout of the ADC.

in Met3 and Met4 so as to avoid mismatch due to parasitics. For *C3* (0.4 pF), a unit capacitor is connected in parallel with a dummy capacitor of value of 0.1 *pF*. The mismatch is less important. Centro-symmetry of *C1*, *C2* and *C4* is ensured by proper distribution around the center of the array.

Shielding is guaranteed by a Met2 plane, ensuring that all parasitic capacitors towards ground are the same for all capacitors. An n-well biased to *Vdd* is placed below the network to prevent any substrate noise to be coupled into the network. The routing of low impedance nodes is done with an external ring passing over the dummy capacitors, while the routing of the high impedance nodes is done by a shorter routing ring in Met3 and Met4 passing in the middle of the array, with equal lengths for all capacitors.

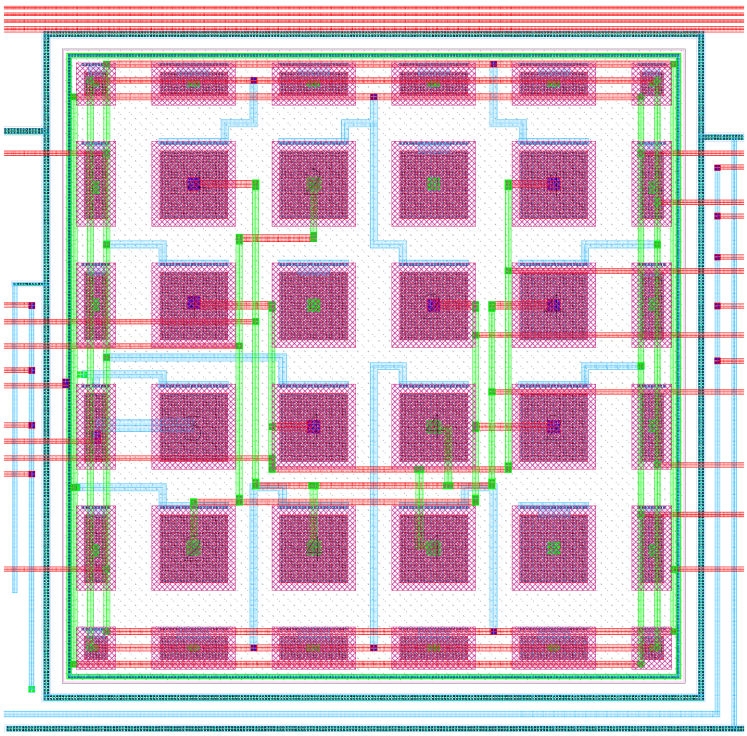

Figure 4.24 : Layout of capacitor network.

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[1] J. Goes, *Systematic design for optimisation of pipelined ADCs*, The Kluwer international series in engineering and computer science ;, Boston: Kluwer Academic Publishers, 2001.

[2] O. Choksi and L. R. Carley, "Analysis of switched-capacitor common-mode feedback circuit," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 50, no. 12, pp. 906–917, 2003.

Chapter 5

Second realization

A second circuit was realized to verify the proposed structure developed in Chapter 3. The prototype has been realized in 0.18 μm CMOS technology. The circuit implements a structure that can run a second-order or a first-order incremental converter before a cyclic conversion. All the digital signals are generated outside the chip with a programmable circuit (FPGA). This allows a larger flexibility on the digital signal sequencing. This chapter discusses specific implementation details including analog and layout issues.

5.1 Technology

The prototype was fabricated using UMC 0.18μm L180 process through EUROPRACTICE [1]. The process has standard threshold voltage levels of 0.5 V and -0.5 V for NMOS and PMOS devices respectively. The voltage supply is 3.3 V. The technology provides 1 poly and 6 metals. Linear capacitors are produced by metal-metal (MiM). The capacitance of these capacitors is approximately 1 $fF/\mu m^2$. The substrate consists of low-resistance $p+$.

[1] http://www.europractice-ic.com/

5.2 Implementation

The proposed implementation of the conversion principle is shown in the schematic diagram of Figure 5.1. A common, switched-capacitor implementation which operates on a two-phase clock is chosen. A second-order incremental converter is implemented but a first order operation is also possible, in this case amplifier *1* is disabled. In this design the reference voltage *vr*, used in the incremental conversion and *vr_rsd*, used in the cyclic conversion are differentiated but they still have the same value. All the differential inputs can be inverted. This is not shown here for simplicity.

The input signal (*vinp*;*vinn*) is fed by switch *s11* on *C1* and the reference voltage (*vrefp*;*vrefn*) is sampled on the **same** capacitor by *s12*. Capacitor *Cf* is the feedback capacitor. For the inversion of the positive integration result, capacitor *C3* is used. In cyclic mode, the only difference is that the reference voltage is provided with *vr_rsd* by switch *s32*.

The operation of the first order is similar to the one presented in the first realization. The second-order incremental occurs also on 4 phases, described below:

Phase A: initialisation

The two feed back capacitors *C2* and *Cf* are reset through *s6*, *s26* and *s28*.

Phase B: positive integration

The integration begins in the first integrator with a positive input signal. The first cycle needs 4 steps. Capacitor *C3* is charged with the input signal and then transferred into feedback capacitor *C2*. At the end of these two steps, a comparison occurs on the intermediate output

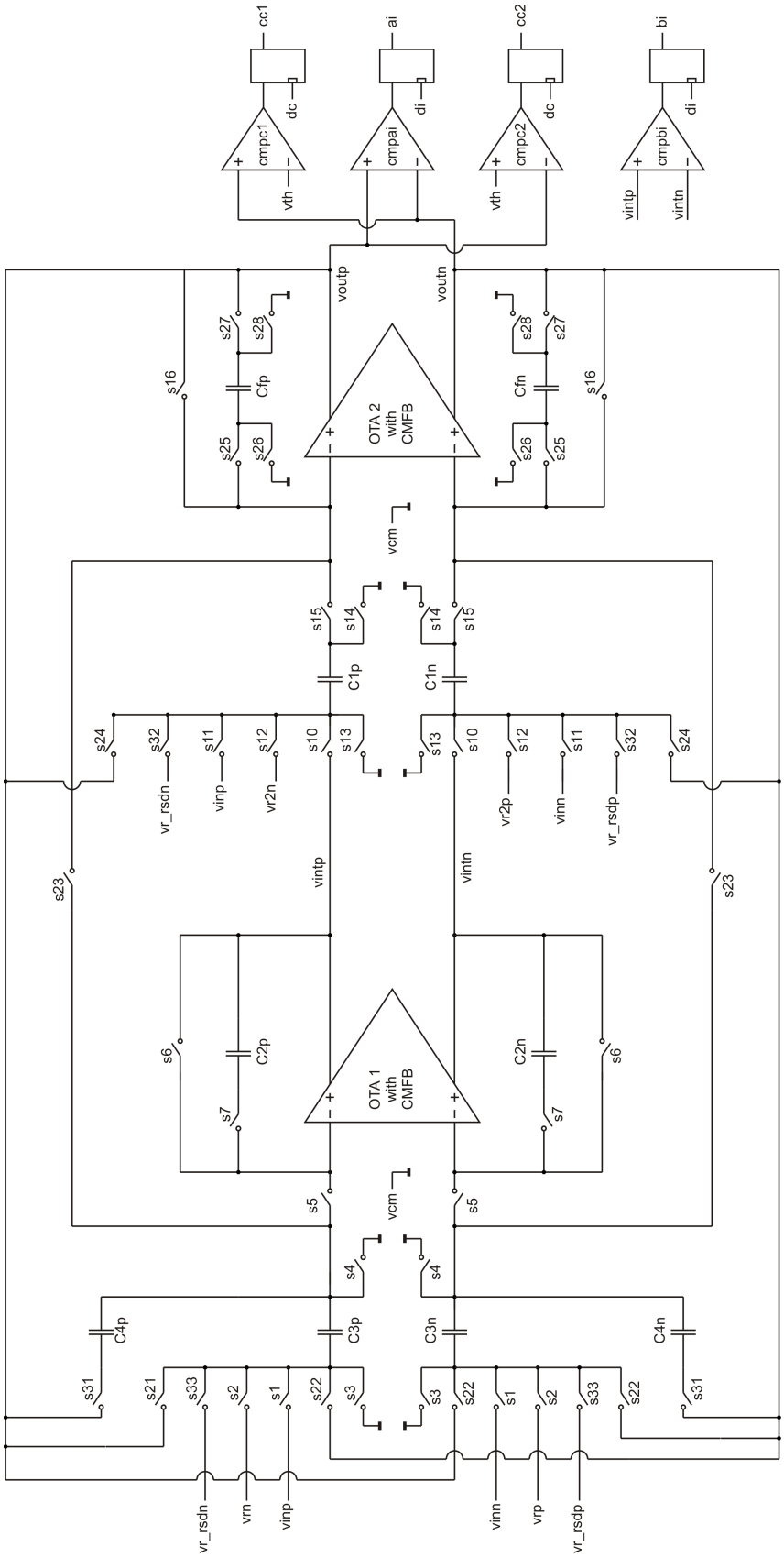

Figure 5.1 : Schematic of 2^{nd} order implementation.

voltage *vint* through comparator *cmpbi*. Depending on this decision, a positive or negative reference voltage is applied on *vr*. In the third step, capacitor *C3* is reset through *s3* and *s4* and in the fourth step the reference voltage is applied through *s2*.

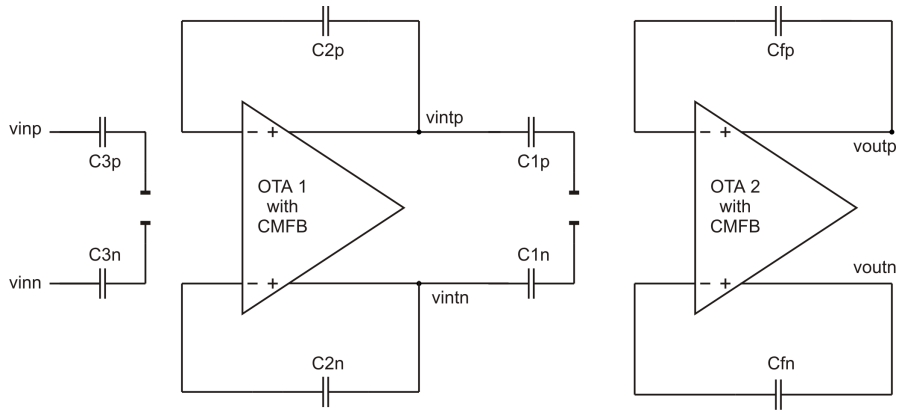

Figure 5.2 : Detailed schematic of the first step of the integration.

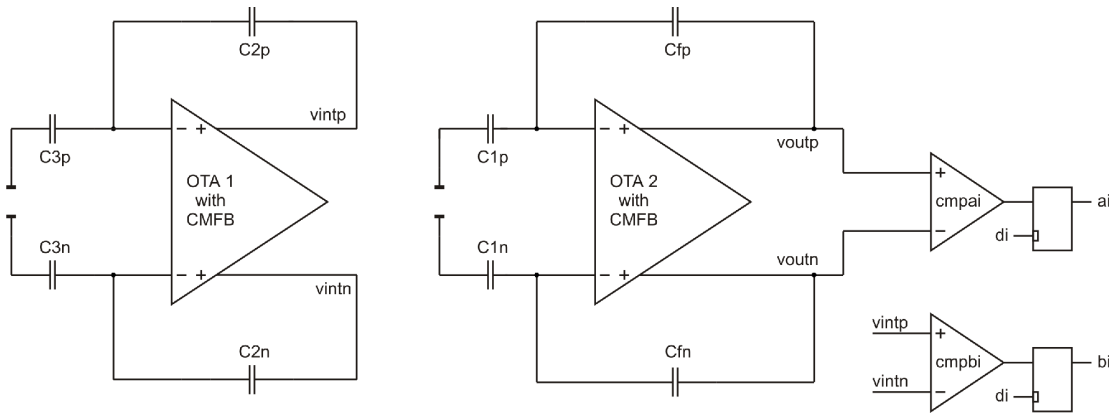

Figure 5.3 : Detailed schematic of the second step of the integration.

The second cycle occurs in four steps too. Capacitor *C3* is again charged with the input signal and at the same time switch *s10* is activated to charge capacitor *C1* of the second stage. Now the two stages operates in parallel with the integration and transfer of the charge.
After $2^{k/2}$ cycles (for k bits of resolution), one more integration cycle is needed for the second stage to complete the same number of cycles.

Phase C: inversion of the residue voltage

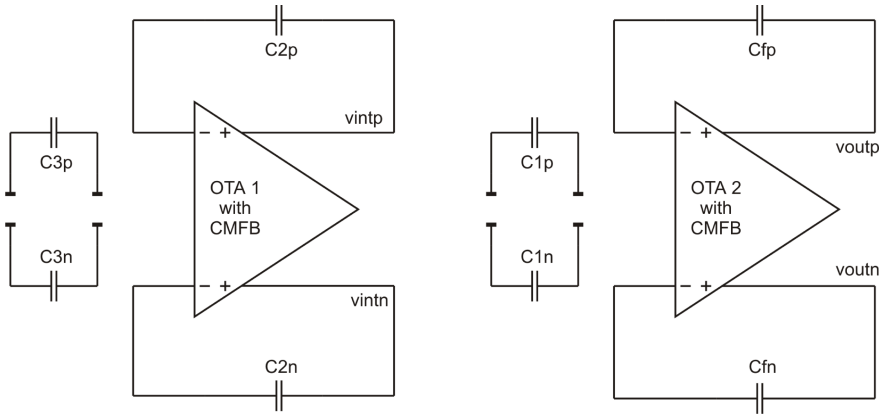

Figure 5.4 : Detailed schematic of the third step of the integration.

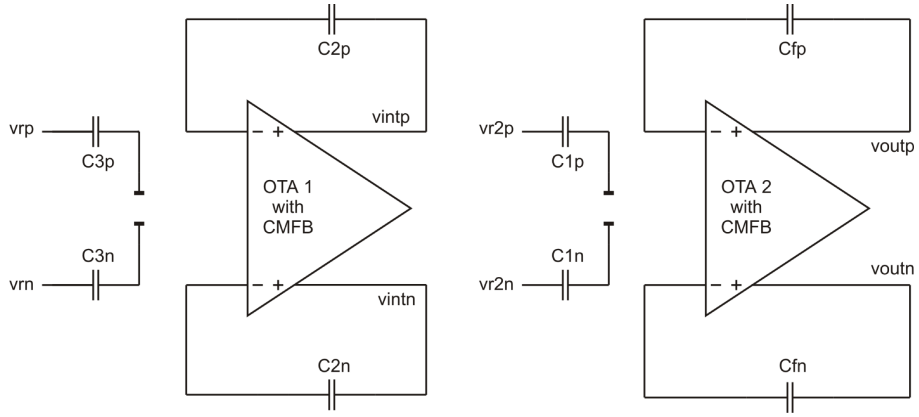

Figure 5.5 : Detailed schematic of the fourth step of the integration.

Like in the first order implementation, the residue the second stage is inverted in three cycles, while the first stage is totally reset.

Phase D: negative integration

The negative integration is exactly the same as the positive integration except that the input voltage *vin* is inverted.

The following cyclic conversion is executed in a same way as described in the previous chapter.

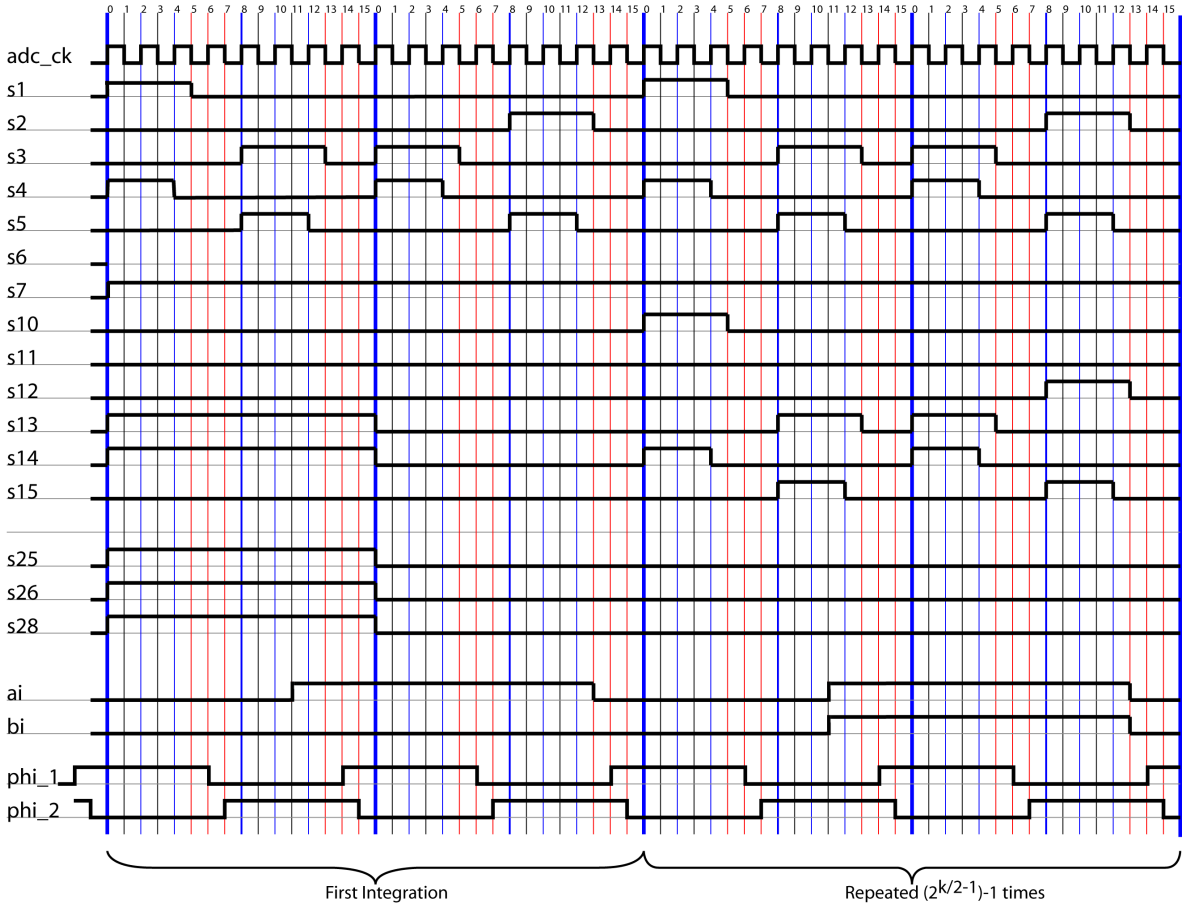

Figure 5.6 : Timing of the integration phase.

5.3 Detailed Design

The data rate is not specified as this circuit is implemented mainly to see the feasibility of the structure. A clock frequency of 5 MHz is specified. The non-overlapping clock $\phi 1$ and $\phi 2$ are not generated any more on-chip but are provided externally. This implies less clock cycles for the integration and transfer process, as it can be seen on timing diagram.

Based on calculations of the previous chapter, a nominal value of 1 pF is chosen for the capacitors. The switches are drawn with the minimal length of 0.34 μm and the width is sized depending on if the

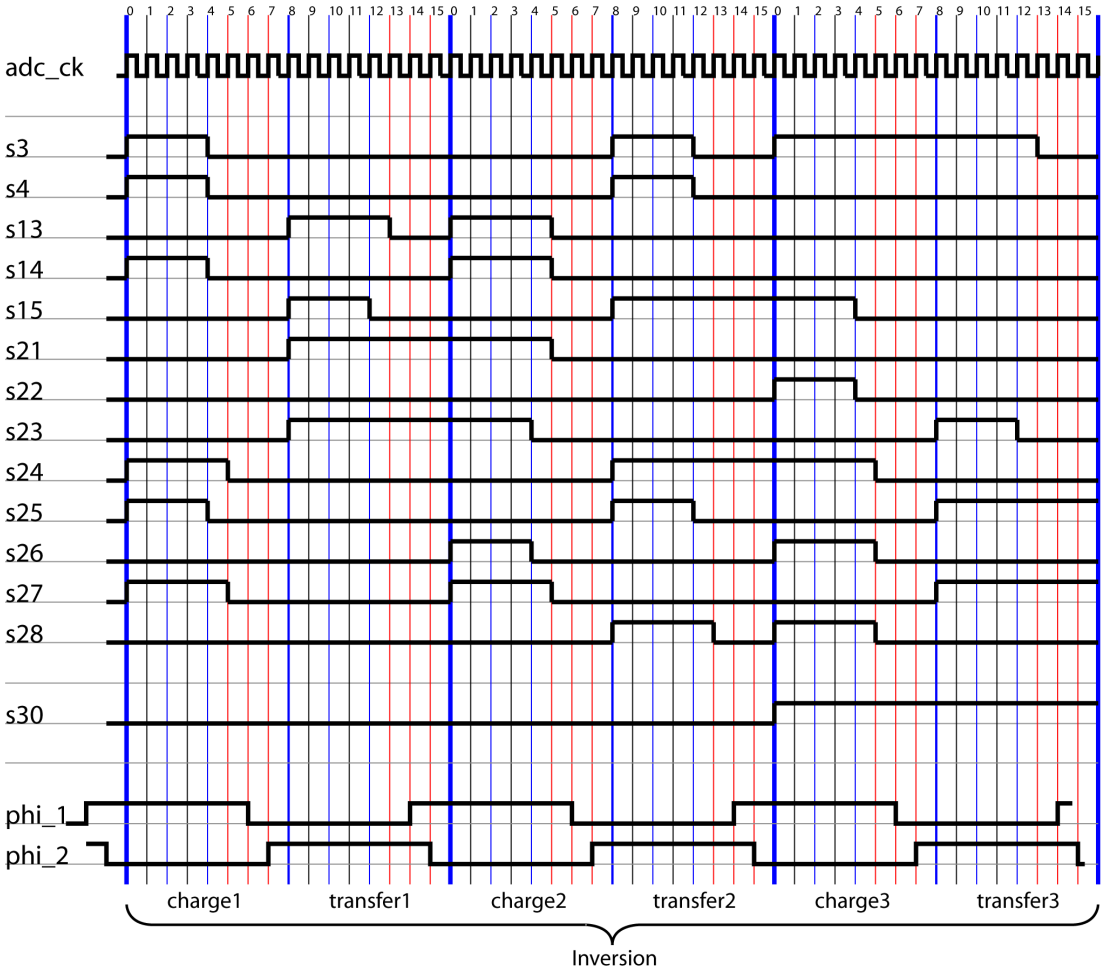

Figure 5.7 : Timing of the inversion phase.

switch is connected to high impedance node or not.

	N	P
High impedance node switches	0.25	0.25
Other switches	1.0	1.0

Table 5.1 : Length of the gate of the transistors in μm.

5.3.1 Amplifier

The proposed OTA structure is the same as the first realization, with the difference of a supply voltage fixed to 3.3V, so a complementary

input stage is not necessary.

Slewing and settling time

The slewing and settling times are fixed at half a clock period, multiplied by 3/8 because not all the half clock cycle is available. In our case, we can specify that about $300ns$ will be dedicated for slewing and $300ns$ will be dedicated for settling. We obtain a minimal GainBandWidth of around 10 *MHz* for a 16 bit precision ADC.

Structure

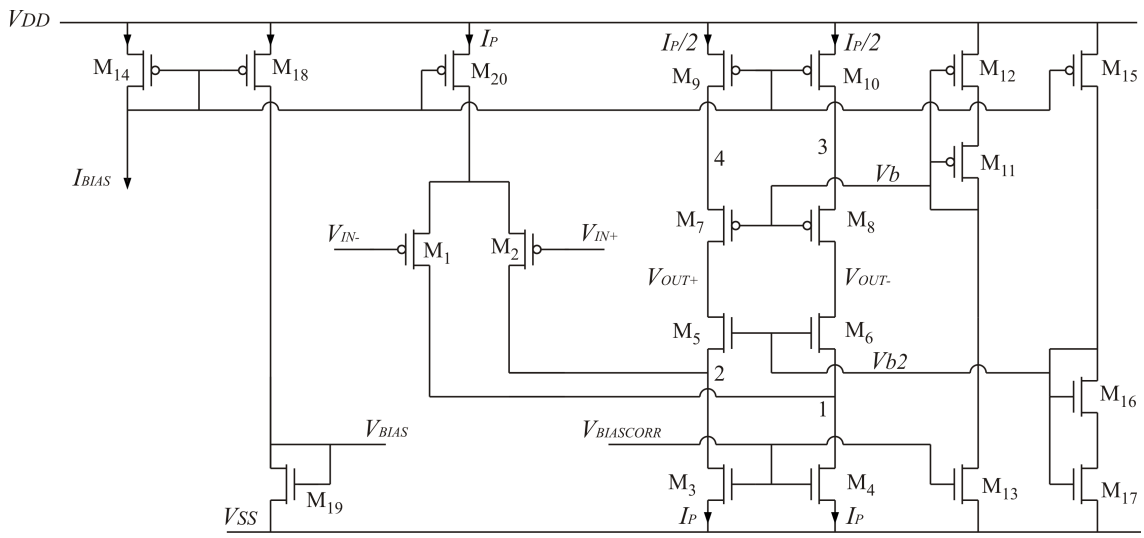

Figure 5.8 : Folded-Cascode amplifier.

M1 and *M2* are the input driver transistors. The cascode transistors are realized with transistors $M5-M8$. The bias currents are defined by NMOS *M3*,*M4* and PMOS *M20*, *M9*, *M10*. The common-mode feedback (CMFB) is achieved by controlling the bias voltages of *M3* and *M4*.

With the previous specification about GainBandWidth and Slew-rate and the initial specification for the gain, we can determine the value of the various transistors sizes. The ratio of the current were set so that $I(M20) = 2 \cdot I(M9)$. The slew-rate requirement gives the minimum

value for the current *Ip*.

$$Ip = SR \cdot C_L \tag{5.1}$$

The current *Ip* is set to 25 μA. The minimum length of all mirror transistors is set to 1 μm for matching considerations. The biasing current that flows through *M14* is set to 5 μA. Transistor *M20* is set in strong inversion with inversion coefficient (IC) of 10, which implies a maximum width of 5 μm. Thus implies a length for *M20* of 25 μm.

Transistor *M19* is set to *W/L* ratio of 4 and *M3−M4* are set to a *W/L* ratio of 20. Here the IC of these transistors is reduced to 5. Indeed with this change we have a smaller V_{DSsat}, which is important for output swing.

The minimum length for the input transistors is set to 1 μm and their width is set to 99 μm. They are working in medium inversion (IC=1.3). The design of the other transistors is executed the same way as described in the previous chapter.

The transistors sizes are summarized in Table 5.2.

Thermal Noise analysis

The main contributor of the noise in such a structure is the differential input stage. The thermal current-noise density in a transistor is equivalent to:

$$i_{nth}^2 = (8/3) \cdot g_m \cdot k \cdot T \tag{5.2}$$

Where g_m is the small-signal transconductance. We can get the equivalent input-mean-square voltage-noise by dividing by g_m^2:

$$v_{nth}^2 = \frac{i_{nth}^2}{g_m^2} \tag{5.3}$$

The noise density must be multiplied by 2 (two input transistors)

Transistor	width [μm]	length [μm]	Id
M1	99	1	2.5 Ib
M2	99	1	2.5 Ib
M3	20	1	5 Ib
M4	20	1	5 Ib
M5	10	2	2.5 Ib
M6	10	2	2.5 Ib
M7	25	2	2.5 Ib
M8	25	2	2.5 Ib
M9	12.5	1	2.5 Ib
M10	12.5	1	2.5 Ib
M11	25	2	Ib
M12	4	10	Ib
M13	4	1	Ib
M14	5	1	Ib
M15	10	2	Ib
M16	18	3	Ib
M17	25	1	Ib
M18	5	1	Ib
M19	4	1	Ib
M20	25	1	5 Ib

Table 5.2 : Amplifier transistors dimensions.

and integrated over the bandwidth of the amplifier, then we take the square root to get the total RMS thermal input noise:

$$v_{nth} = \sqrt{2 \cdot \int_0^{GBW} v_{th}^2 \cdot df} \tag{5.4}$$

Values of 41 μV and 42 μV are obtained with respectively 5 μA and 10 μA of bias current.

Simulations

Figure 5.9 shows the AC simulation with a load of 1.5 pF on each output node and with typical conditions.

The next table shows the performances of the amplifier with two different bias currents. The thermal noise here is not simulated but

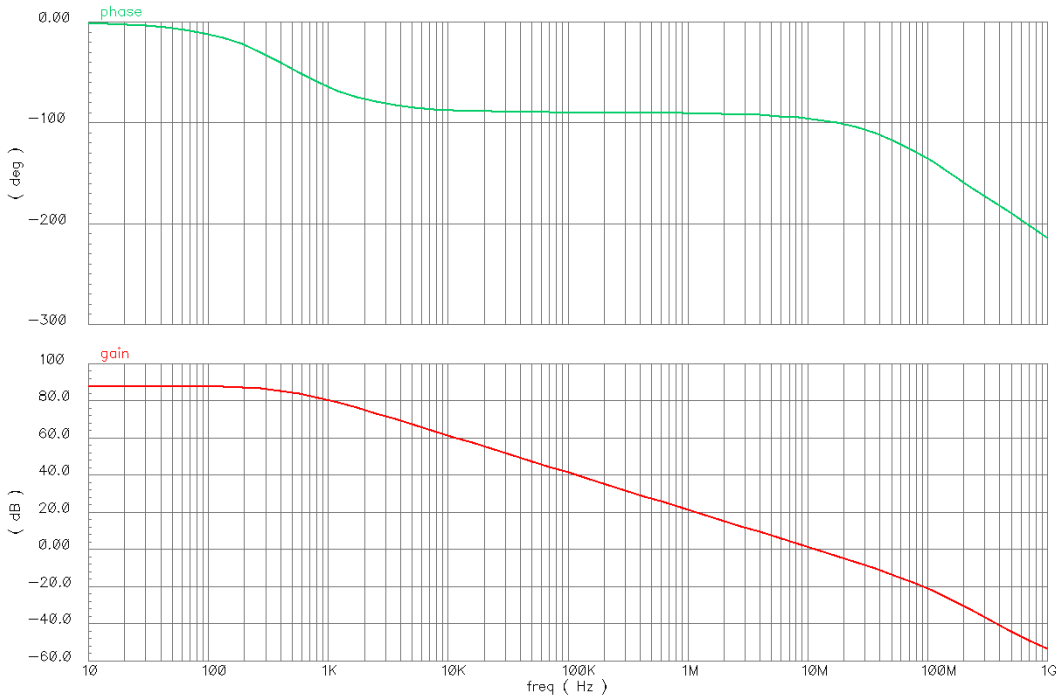

Figure 5.9 : Phase and gain of the amplifier with 5uA bias.

obtained by calculation.

Bias Current	$5\mu A$	$10\mu A$
Open loop gain	87.7 dB	90.7 dB
GainBandWidth	11.7 MHz	19.5 MHz
Phase margin	86.7°	86.3°
Current consumption	$65\mu A$	$130\mu A$
Thermal noise	$41\mu V$	$42\mu V$

Table 5.3 : Amplifier performance.

5.3.2 Comparator

The comparator is the same as designed in the first realization. It is even simpler as the threshold generator is not present but provided externally.

5.4 Digital control

The digital control is generated outside the chip on a programmable board. It has three main purpose:

- Control the overall operation of the ADC (modes, resolution, etc.)
- Generate the signals for the switches of the ADC.
- Collect the bit stream from the comparators and convert it into an output value.

The advantage of using an external logic control is a larger flexibility. Modes and resolution are not limited and errors can be easily corrected. The disadvantage is a large number of digital signals (around 40) and corresponding pads generating a lot of noise.

5.5 Physical design

The final layout of the prototype ADC is shown in Figure 5.10. Even if the layout is not optimized, the active area of the ADC is 0.28 mm^2. All analog paths were drawn differentially to increase the rejection of common mode noise, such as substrate noise and supply voltage fluctuations. In this layout, the following approach is taken. Separate supply rails are used for the digital and analog power signals. Because an n-well process was used, the digital and analog PMOS transistors are naturally isolated by separate wells. The NMOS transistors, however, interact via the common, low-resistance $p+$ substrate.

For the analog NMOS transistors, it is important that the source-to-body voltage is constant. Otherwise, if these voltages move relatively to each other, the drain current is modulated through the body effect. Therefore, it is important to locally have a low-resistance path

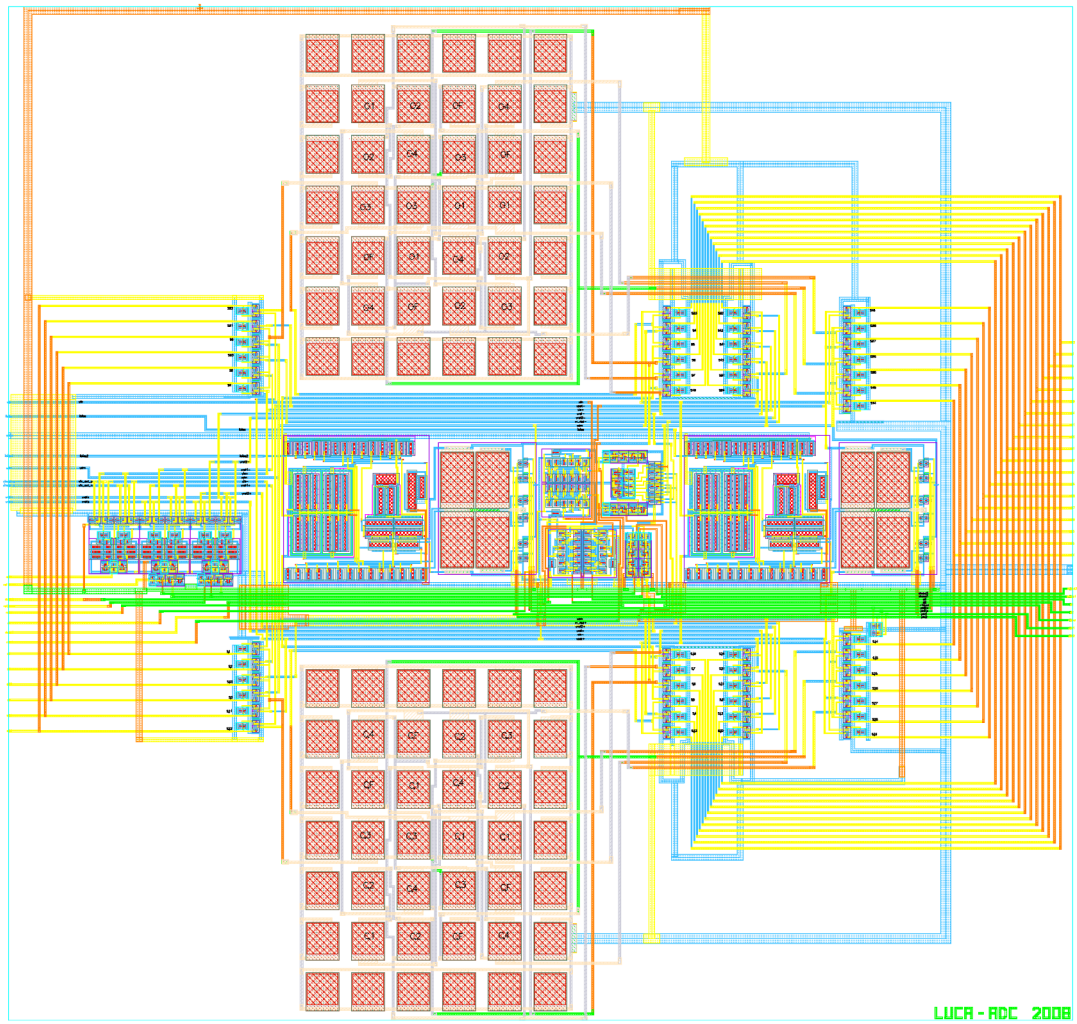

Figure 5.10 : Layout of the overall chip.

from body to source. In the layout, a $p+$ substrate contact is placed near each NMOS analog transistor. This contact was then contacted to ground, which is the same potential as the source for common-source devices. This helps keeping the potential of the source and the body to be identical.

The differential inputs and all other analog signals enter the chip from the left. The amplifier stages are clearly visible in the middle. Two rows below and above are the routing of the digital signals such as clocks and data outputs. Using this arrangement, there is a minimum of analog

and digital signal line crossing.

Capacitors are implemented with metal-metal technology. The capacitors are split into 4 and then designed in an array of 4 x 5 capacitors with dummy capacitors all around. A common-centroid layout as been used as displayed on Figure 5.11 to have a good matching between the capacitors. Coupling noise is reduced by avoiding routing or placing active elements under the capacitors. Figure 5.12 shows the full chip die.

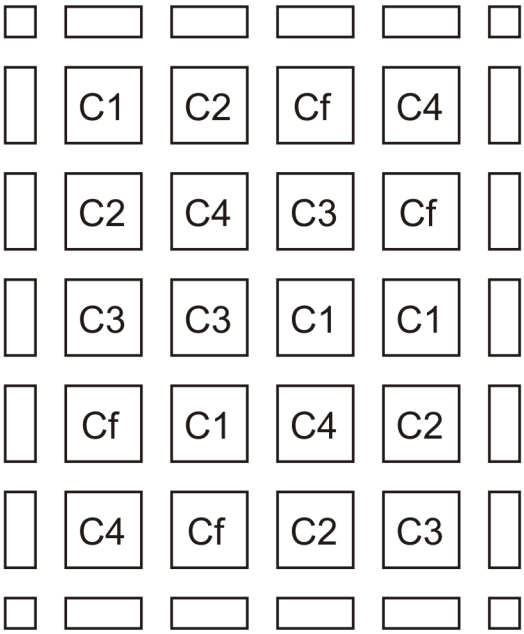

Figure 5.11 : Capacitors layout.

The ADC is part of a multi-project asic and a lot of unrelated project are present on the die. The die is encased in a 68-pin JLCC ceramic package.

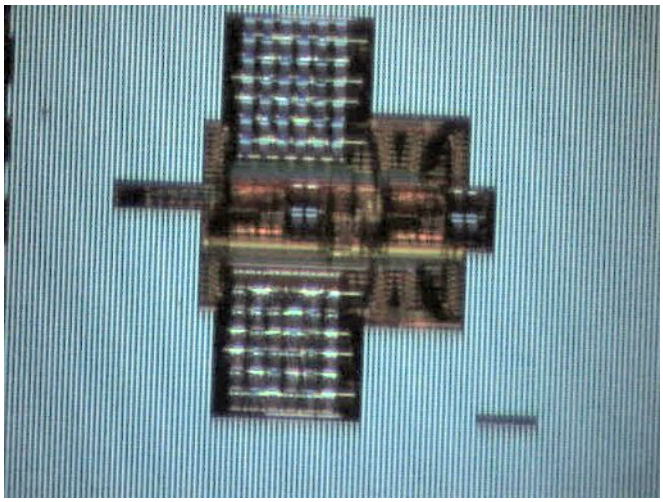

Figure 5.12 : Die photo

Chapter 6

Results

6.1 Test methodology

This chapter explains the methodology to characterize an ADC and to obtain the main parameters described in 1.2.1. The purpose here is not to list all the methods but simply the ones that are used in this work.

6.1.1 Histogram method

The histogram test is based on a statistical analysis of the probability of appearance of output code of the converter.
The first step is to create the histogram with an input signal with a known voltage distribution. Generally a sinus or a linear (ramp or triangle) input is used with a non-coherent frequency with the sampling frequency. The value of the histogram is directly proportional to the width of the code. The DNL is equal to the difference between the code width and the average code width. If we take a normalized histogram, the DNL is simply the histogram value minus 1. The INL is obtained by accumulation of the DNL. Both DNL and INL can be deduced from histogram method with an accuracy inversely proportional to the average number of hits per code.

It is necessary to have all the codes being hit, for a valid histogram. While the amplitude of the input is not easy to deal with, codes of the extremity could be not present at the output of the ADC. To avoid this problem, the amplitude of the input signal is chosen to be higher than the input range of the converter. In our test a value 10% higher was chosen.

There are two ways to perform a histogram. The first is to provide a rising or a falling linear ramp and collect samples at a constant sampling rate. The ramp moves slowly from one end to the other end of the input range. The ramp should move slowly enough to ensure that each code is hit several times. Any non-linearity of the ramp influences the histogram and causes errors mainly on the INL.

The second one is to generate a sinusoidal signal. Since it is easier to produce a sinusoidal wave than a perfectly linear ramp with very high accuracy, sinusoidal histogram is preferred. The distribution in a sinusoidal histogram is not uniform like in a linear ramp histogram, but exhibits a shape with lower and upper codes appearing more often (see Figure 6.1). It is then necessary to normalize the histogram to extract the ADC parameters. Hereafter, the process of the normalization for sinus input is described. A sinusoidal input with an input range higher than the ADC input range is fed to the converter. This results in a saturated histogram at minimum and maximum value of the converter. Let us denote the histogram as *H(i)* with *i= 0,1,,*$2^N - 1$ for an N-bit ADC. For each value of *H*, we have the number of hits for the corresponding code. The method and equations are derived from [1]. First the mismatch of *H(0)* and *H(*$2^N - 1$*)* gives an indication about the offset of the input signal, while the total number of hits gives the amplitude. The next equations express the offset and amplitude in terms of LSB.

$$offset = \left(\frac{C_2 - C_1}{C_2 + C_1}\right)(2^{N-1} - 1) \tag{6.1}$$

Figure 6.1 : Histogram with an overrange sinus signal.

and

$$peak = \frac{2^{N-1} - 1 - offset}{C_1} \tag{6.2}$$

where

$$C_1 = \cos\left(\pi \frac{H(2^N - 1)}{N_S}\right) \tag{6.3}$$

$$C_2 = \cos\left(\pi \frac{H(0)}{N_S}\right) \tag{6.4}$$

N_S represents the total number of samples.

Once the value *peak* and *offset* are known, the ideal sine wave distribution, denoted HS, can be calculated. This represents the distribution of an ideal ADC excited by a sinusoidal input. Excluding the lower and upper code, the value for each code is given by:

$$H_S(i) = \frac{N_S}{\pi}\left(\sin^{-1}\left(\frac{i + 1 - 2^{N-1} - offset}{peak}\right) - \sin^{-1}\left(\frac{i - 2^{N-1} - offset}{peak}\right)\right) \tag{6.5}$$

The ideal histogram, like if a linear ramp had excited the ADC, is obtained by dividing the histogram by the ideal sine histogram. Extreme

codes can not be calculated by this method and are by default set to 1.

The total number of samples should be large enough so that each code is hit a minimum number of times. In general to compute the number of samples N required to measure the static linearity to within $\pm\beta$ LSB at the n bit level is given by [2]:

$$N \geq= \frac{\pi \cdot 2^{n-1} \cdot Z_{\alpha/2}^2}{\beta^2} \tag{6.6}$$

where α is the probability that error exceed β
$Z_{\alpha/2} = Z : F(Z) = 1 - \alpha/2$
$F(Z) = \int_{-\infty}^{\alpha/2} \frac{1}{\sqrt{2\pi}} e^{-t^2} dt$

For example, $n = 14$ bits, $\beta = 0.1$ LSB, $\alpha = 0.05$ ($Z_{\alpha/2} = 1.96$) requires around 10 millions samples to be recorded. For converter that has low frequency sampling, it represents hours of data collecting and additional source for noise and errors.

One disadvantage of the histogram method with converter without sample and hold in front of the circuit, is that no static input is measured. In fact, some artifacts or sparkle codes could be masked or attenuated when the converter average the input.

6.1.2 Spectral analysis

The dynamic and noise performance of the converter can be measured by a spectral analysis. The principle is to apply a sinusoidal signal at the input of the ADC and the measurement of the dynamic linearity is achieved by performing a Fast-Fourier Transform (FFT) of the output codes.
The spectral analysis needs to be applied on a temporal window of the signal and if care is not taken, artifacts called leakage appears. These errors can be totally removed for an input signal frequency known and

having a special relationship with the sampling frequency. In fact, the spectrum is also sampled and the step is directly derived from the number of samples used for the FFT:

$$\Delta F_{step} = \frac{F_S}{N_S} \tag{6.7}$$

where Ns is the number of samples and Fs the sampling frequency.
If the frequency of the input signal is equal to k times (with k whole number) the frequential step ΔF_{step} then the frequency of the signal would coincide with a point of calculation of the FFT. This is equivalent to say that the temporal window contains an integer number of periods of the input signal. Theoretically this condition can not be ensured in all the cases and it is better to apply a windowing (other than the rectangular one) to minimize the leakage effects. The FFT is computed using a Hanning window on samples of 1'024 to 16'384 samples depending on the availability of number of samples. Data is then analyzed using the formulas described in section 1.2 to extract SNR, SNDR, THD and ENOB.

6.1.3 Conclusions

We are in presence of multiple tests for characterizing the ADC behavior. The histogram method is based on statistical analysis and furnishes information on the transfer characteristics of the ADC. The spectral analysis is a powerful test to obtain information about the dynamic behavior of the ADC. Most tests are realized with a sinusoidal input which can be generated with a very high linearity. These tests are globally complementary, since they can determine different functional parameters.

6.2 First Realization Test

All measurements have been performed under 1.65V. The input signal is single-ended and provided externally by a high precision function generator Applicos 7002[1]. A testboard controlled by Labview[2] is used to collect and transfer the signal to a PC. Data are then analyzed with Matlab.

6.2.1 Issues

Non-linearity errors

Peaks or discontinuities appeared when a ramp was provided to the comparator. After several measurements, it appears that:

- Two peaks are spaced out by the double of the dynamic of a cyclic conversion: every 512 LSB in 8-8 mode or every 256 LSB in 9-7 mode.
- The height of the peak is constant from one chip to another for the same resolution mode, but it is proportional to the resolution of the cyclic conversion.
- The positions of the peak compared to the transition points of the incremental converter are randomly spreaded.

The peak appears one out of two in a cyclic conversion. This leads us to deduce that this problem is not from the cyclic conversion; otherwise it would have appeared at every cyclic conversion.

Matlab simulations have been carried out to find the root of the apparitions of these peaks. It appears that those peaks can be related to

[1] http://www.atx7006.com/atx7002
[2] http://www.ni.com/labview/

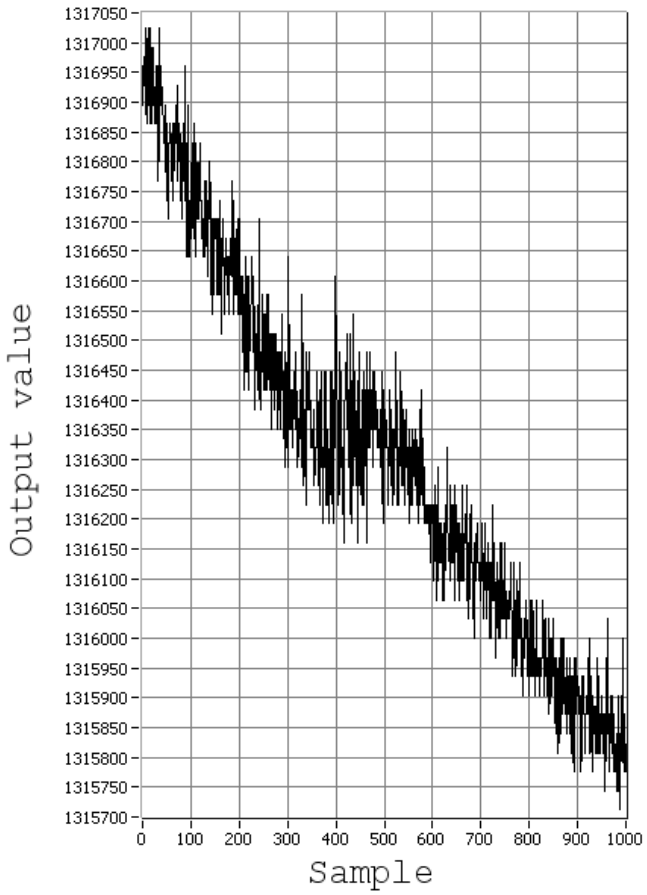

Figure 6.2 : Apparition of a peak on the output value when a descending ramp is applied to the input of the converter.

gain error in the inversion of the residue in the middle of the incremental phase. In the incremental phase the input is integrated 2^{k-1} time. After the positive integration cycle we have:

$$Vout_{[2^{k-1}]} = 2^{k-1} \cdot Vin + N_1 \cdot Vr \tag{6.8}$$

The residue is then inverted. The inversion of the residue is theoretically very precise due to a special method in three cycles where only second order mismatch error is present. We can introduce a mismatch Λ in the inversion process. After the negative integration we have:

$$Vout_{[2^k]} = -(1+\Lambda) \cdot 2^{k-1} \cdot Vin + (N_2 - \Lambda \cdot N_1) \cdot Vr \tag{6.9}$$

Observations from the simulations are the following:

- The peak position is dependent on the offset of the comparator used in the incremental phase and also on the offset of the amplifier. In the absence of offset the peak is situated in the middle of a cyclic conversion.
- The height of the peak is dependent on the gain error in the residue inversion and the resolution of the cyclic conversion.

The simulation allowed to reproduce exactly the errors observed during the tests. We observed a peak of about 1'200 LSB (with 21 bit resolution) with 6-10 mode. This corresponds to 37 LSB with a 16 bits resolution. A simulation was carried out to find the same figure and this could be verified by applying a gain of -1.05 in the inversion residue. On

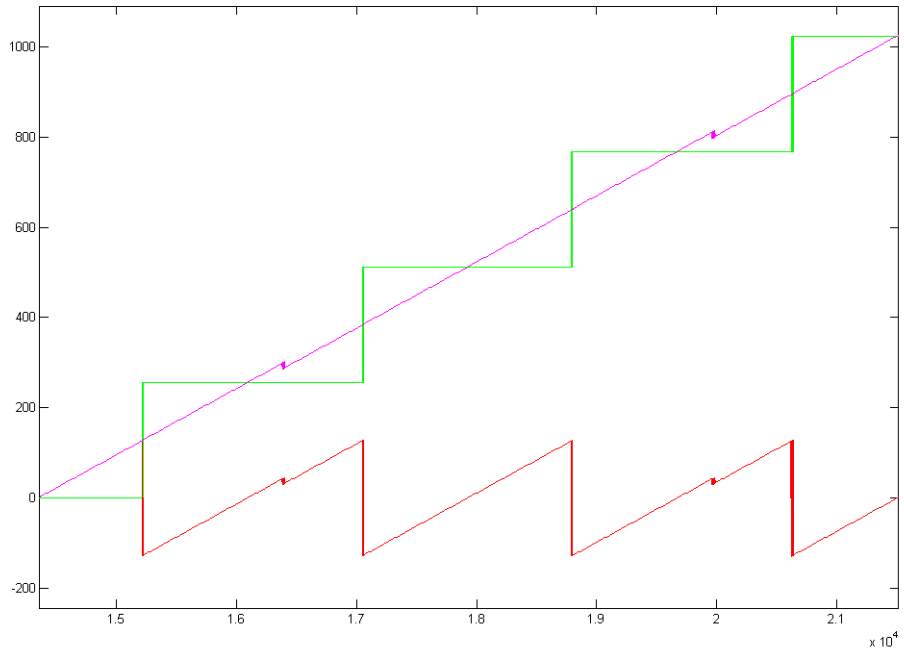

Figure 6.3 : Simulation of the ADC in 4/7 mode with gain inversion set to -1.05.

transistor-simulation of the inversion phase a maximum error of -1.005 was observed, which is a tenth of the observations.
Simulations with a post-layout schematic including all the parasitic ca-

pacitors, which was not done previously, have been performed and showed a gain of -1.05 during the inversion phase. This gain confirms that parasitic capacitors are the main source of this error.

In the inversion phase, the charging of the residue into capacitor *C4* was performed in an opposite way. Indeed the capacitor is charged from the side that is connected to the amplifier input, to allow the inversion of the value, whereas in all the other charge operations, the side connected to the amplifier output is used instead. Poly-Poly capacitors do not have symmetrical parasitic capacitors and the "left" side of the capacitors presents a $50fF$ capacitors that influences the inversion operation. Indeed, when only this parasitic is included in the simulation, we can observe a -1.05 inversion gain. In Figure 6.4 is shown the old architecture. The corrected implementation uses the differential structure to charge the capacitors *C4P* and *C4N* by crossing the output wires.

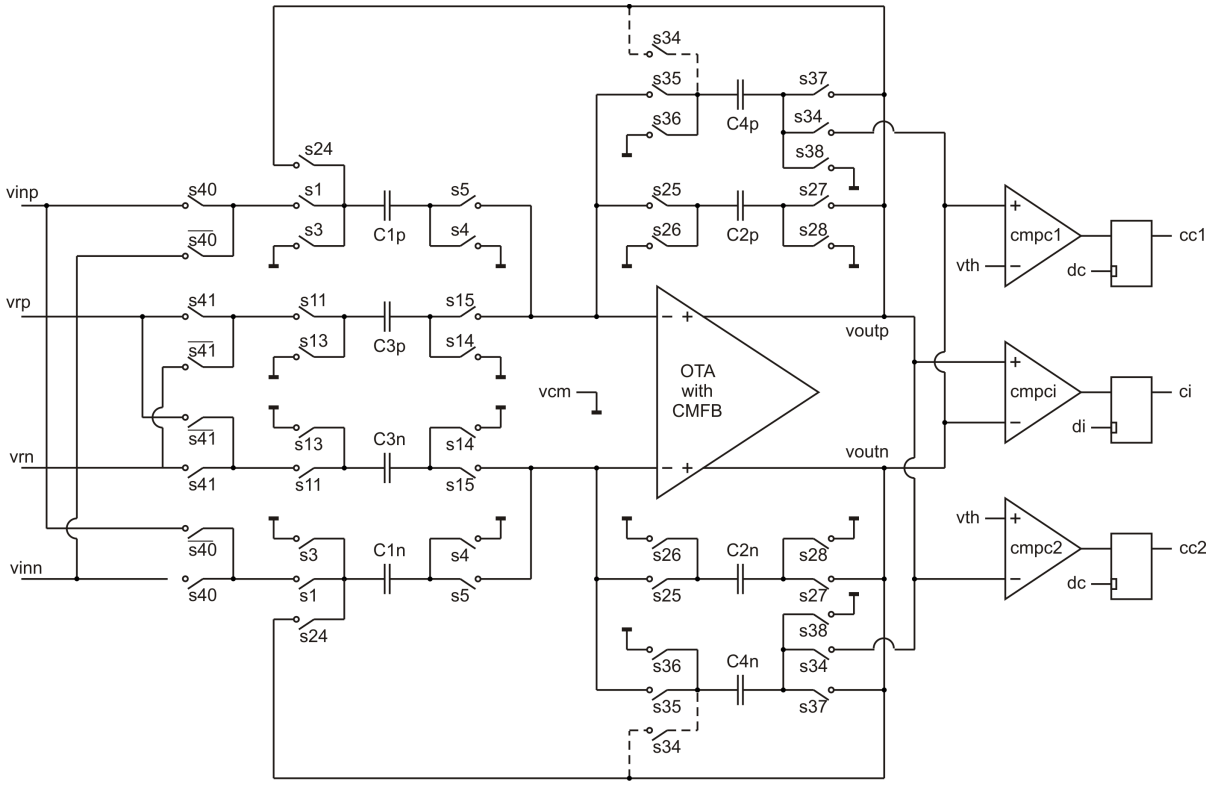

Figure 6.4 : First order architecture with the old switch *s34* in dashed line.

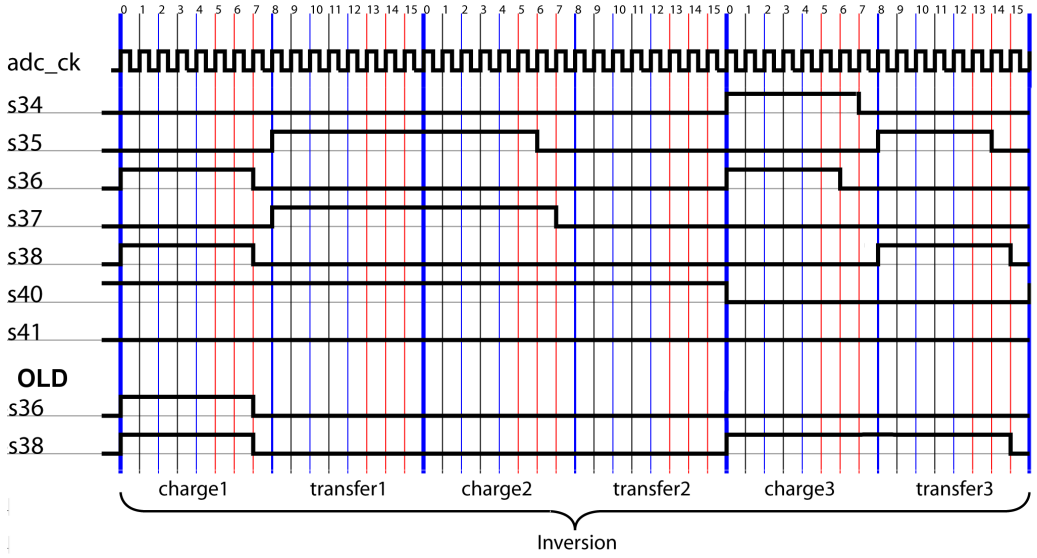

Figure 6.5 : Corresponding timing for new and old version.

After this improvement, post-layout simulations have been performed and the gain in the third phase was of -0.99988.

Mid-code error

After the correction of the peaks, another error appeared with a peak near the mid-code of the ADC. This error was hidden by the previous one. The step transition amplitude varies from one circuit to another: from 0 to 12 LSB. Their positions is observed in general at -1 (in incremental code) and $+1$. The code 0 correspond to the mid-code. For some circuit, it has been observed also at -3 and $+3$. These steps are observed in mode 8-8, 9-7 and 10-7.

After investigation to find the cause of the error, it appeared that the gain of the amplifier was too small. The models of the transistors used during design were inaccurate. The real devices had a higher threshold voltage, which led to reduced performances. A plot of the gain in function of the input voltage is plotted in Figure 6.7. The input signal range is between 0.6V and 1V and is clearly decreased for these extreme

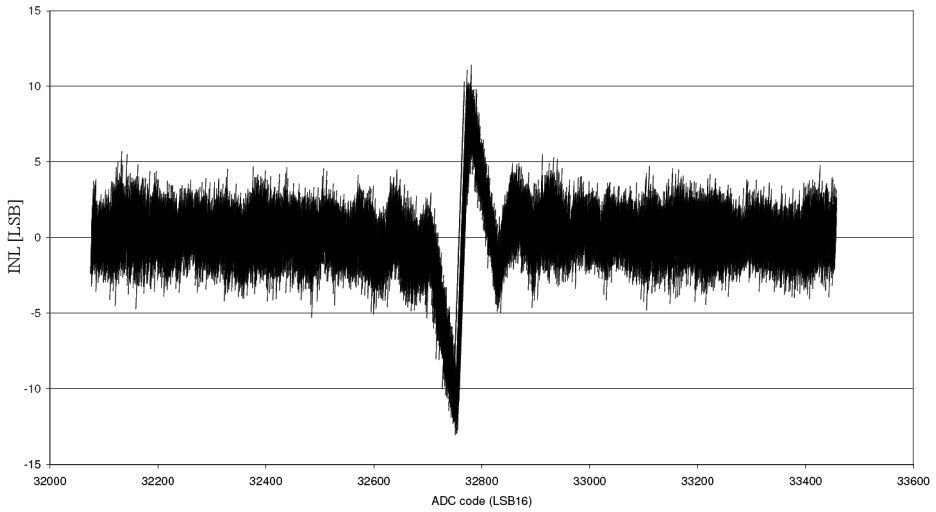

Figure 6.6 : Discontinuity in the middle of the output code.

value.

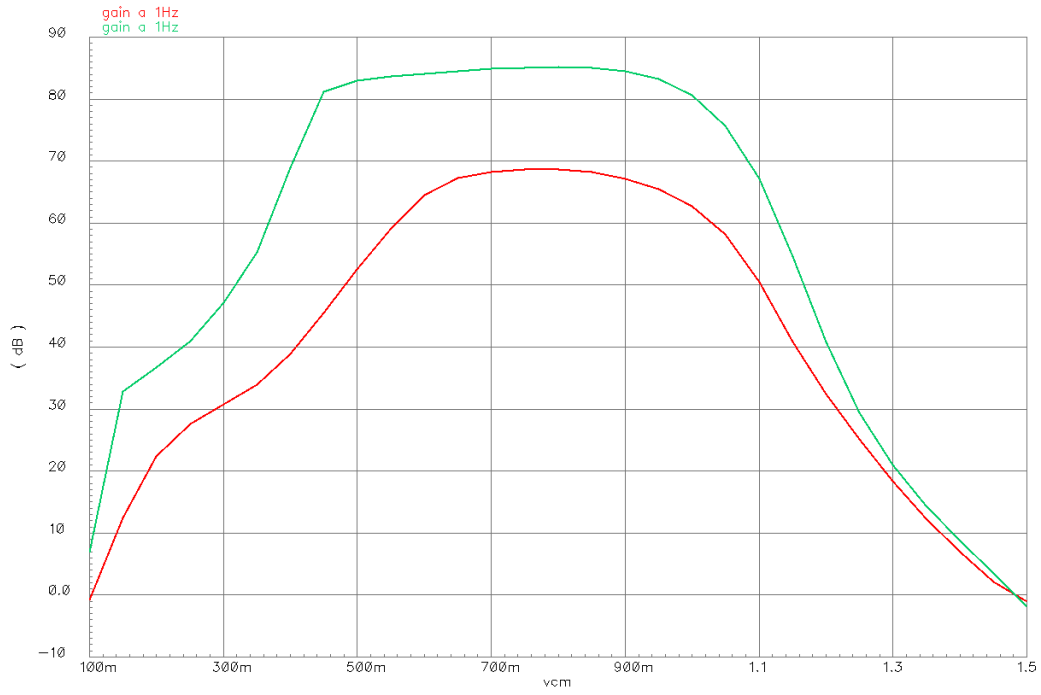

Figure 6.7 : Open loop gain of the amplifier with respect to input voltage. In green with old models and red new models.

The discontinuity in the middle of the input range can be explained

if we take an input value near 0. In the integrator, the voltage will alternate between 0 and $+Vr$ or $-Vr$. The gain of the amplifier within the extreme value is really degraded and the integration process is more affected.

Simulations have been performed with a degraded gain with Matlab and a peak in the middle of the output range is clearly visible in Figure 6.8. Since no full-metal revision could be made but only a few layer,

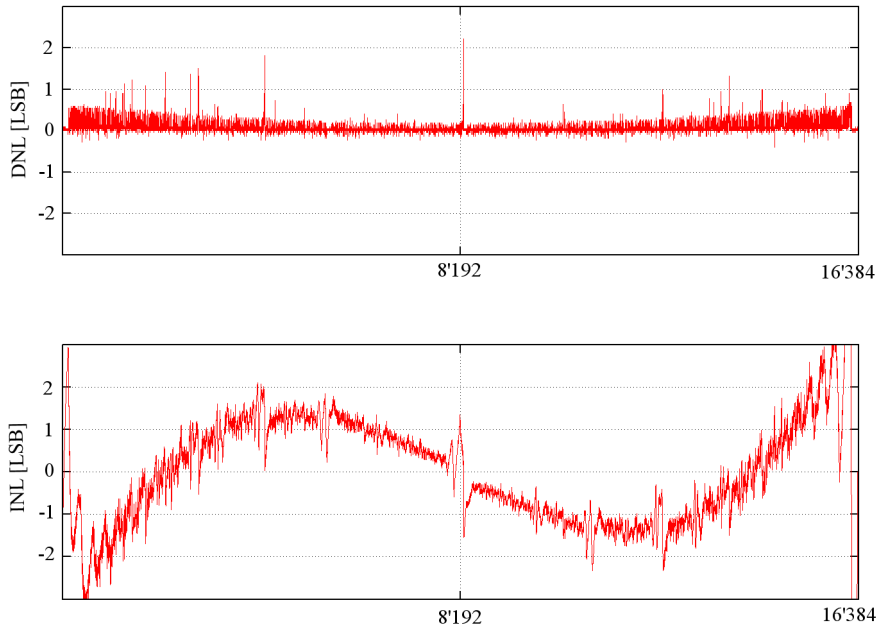

Figure 6.8 : Simulation of a the ADC in mode 6-8 with amplifier degradation.

the amplifier has not been entirely redesigned. Bias current has been adapted to increase the gain of the amplifier. Capacitor *C3* has been decreased to reduce the input range and to benefit of the higher gain near the common-mode voltage. After this correction, the peak in the middle of the range was strongly reduced, but the DNL curve is still affected by the residual gain error.

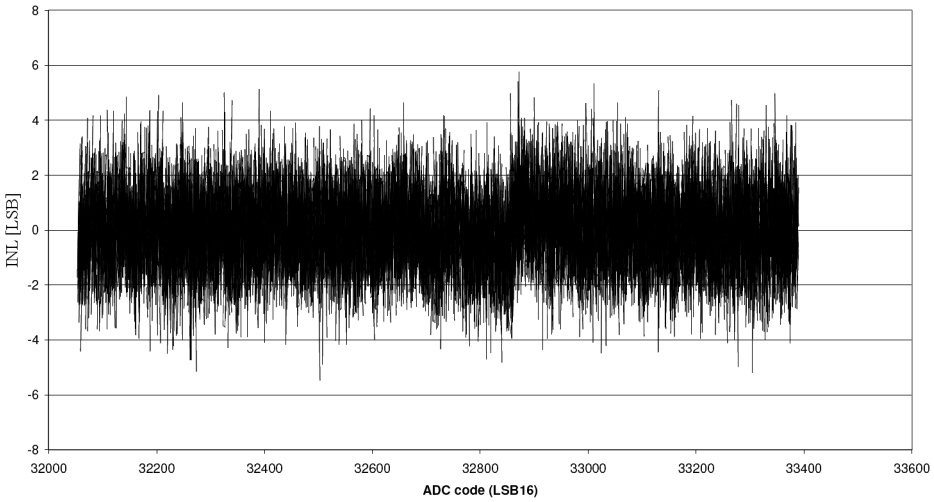

Figure 6.9 : Discontinuity in the middle of the output range has disappeared.

6.2.2 Measurements

Noise

To measure the amount of input-referred noise, the inputs of the ADC are shorted and a large number of output samples are collected. Since the noise is approximately Gaussian, the standard deviation of the collected data, which can be calculated, corresponds to the effective input RMS noise. Effect of quantization error should appear when the noise is under 1 LSB and is not taken into account in our measurements.

mode 7-7	mode 6-8	mode 5-9	mode 4-10
0.45	0.67	0.9	1.3

Table 6.1 : 14 bit ADC. Noise measurements in LSB

mode 9-7	mode 8-8	mode 7-9	mode 6-10
0.75	1.1	1.3	1.7

Table 6.2 : 16 bit ADC. Noise measurements in LSB

The inputs of the ADC are shorted internally. Measurements with inputs shorted externally were also performed. The difference is that an internal block (a pre-amplifier extern of this project) is present on the

path and it generates noise. For a 14 bit configuration: in mode 7-7 the noise grows from 0.45 LSB to 0.95 LSB of standard deviation. In mode 6-8, the noise is increased from 0.67 LSB to 1.4 LSB. Standard-deviation noise is doubled with this block. Limitation is from thermal noise, in fact noise due to mismatch should appear in a repetitive mode as shown in simulation.

Linearity tests

The linearity were performed on a 16-bit configuration with the 9-7 mode.
A linear ramp was applied to the ADC input. The output code was then compared to the best fit line to compute the INL. An averaging was computed on the data to reduce the noise and better observe the INL curve. Error is within -2/+2.2 LSB. We can observe a certain similarity with Figure 6.8. The way of the curve oscillate along the output range is similar to the simulation where the gain of the amplifier was reduced. This shows that the limited correction of the gain could not solve completely the gain problem of the OTA, which still degrades the performances.

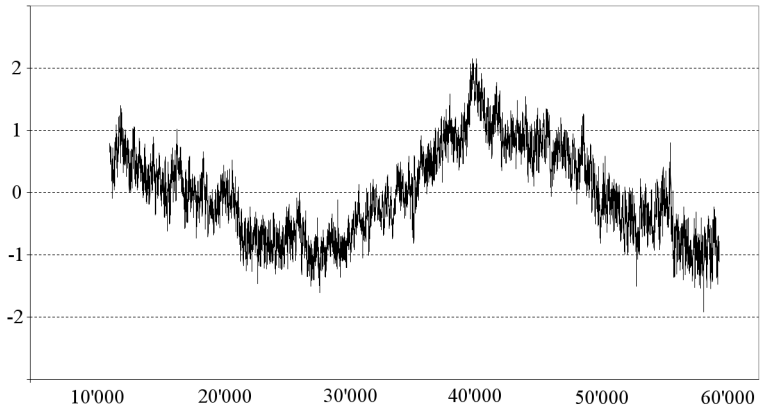

Figure 6.10 : INL of the ADC in mode 9-7.

For DNL characterization, the histogram method was used. Measurements were performed on around 2 millions points. The DNL is

within -0.9/+1.7 LSB.

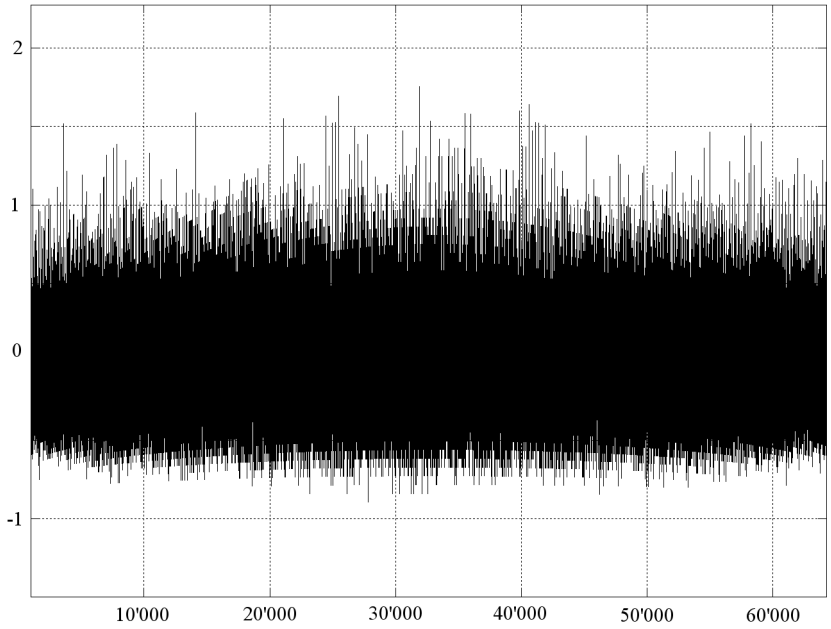

Figure 6.11 : DNL of the ADC in mode 9-7.

Dynamic tests

Dynamic tests were processed with a 500mHz single-ended sine wave. The result were calculated with a Hanning window. In Figure 6.12, we have the spectrum for a 16 bits ADC with mode 9-7 after all the corrections. Different mode were tested for a given resolution. The SNDR is calculated from the spectrum. ENOB and FOM are also shown in the next Tables.

Mode	**Rate**	**SNDR**	**ENOB**	**FOM**
	[kS/s]	[dB]	[bits]	[pJ]
6-6	3.48	70.4	11.4	16.6
5-7	5.82	69.8	11.3	10.6
4-8	8.64	68.5	11.1	8.2
3-9	11.17	67.5	10.9	7.3

Table 6.3 : ADC 12 bits. Dynamic results.

For 12-bit resolution, the maximum SNDR is around 70 dB, which

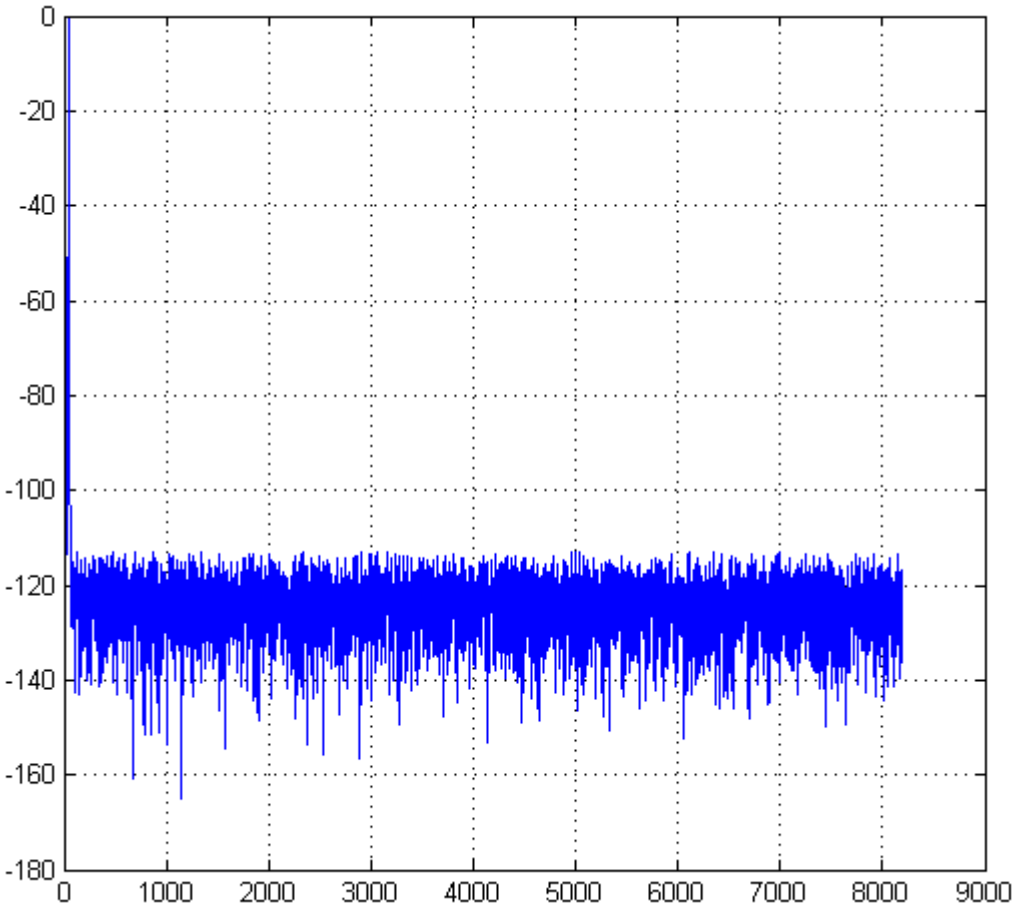

Figure 6.12 : ADC spectral plot of the 16 bits ADC in mode 9-7.

Mode	**Rate**	**SNDR**	**ENOB**	**FOM**
	[kS/s]	[dB]	[bits]	[pJ]
7-7	1.89	78.1	12.7	12.4
6-8	3.39	76.7	12.4	8.5
5-9	5.58	75.0	12.3	5.5
4-10	8.12	73.0	12.0	4.7

Table 6.4 : ADC 14 bits. Dynamic results.

Mode	Rate	SNDR	ENOB	FOM
	[kS/s]	[dB]	[bits]	[pJ]
9-7	0.51	84.8	13.8	21.4
8-8	0.99	82.5	13.4	14.6
7-9	1.86	80.3	13.0	10.2
6-10	3.3	77.0	12.5	8.1

Table 6.5 : ADC 16 bits. Dynamic results.

is equivalent to a 11.4 bit ADC. The SNDR is degraded when more bits are solved by the cyclic converter as expected. For 14-bit and 16-bit, performances are degraded by respectively around 2 and 3 bits of effective resolution. An important part of this noise is supposed to be added by the pre-amplifier which is in front of the converter input and to the limited gain of the OTA.

6.2.3 Measurments discussion

The realized circuit proves the feasibility of the new cascaded architecture of incremental and cyclic converter.

The design of the amplifier is not optimal. The gain is reduced and also degraded when input value move away from the common-mode voltage. The input range has been reduced by lowering the reference sampling capacitor. This implies an increased kT/C noise due to *C3*.

Mismatch of capacitor is not visible in our test and is drawn by the noise even with a 10-bit cyclic conversion. Peak should appear regularly at the transition points of the incremental converter. Even if mismatch is not an issue for this circuit, an implementation with metal-metal capacitor is an alternative to reduce parasitic coupling capacitors.

The output results have too much noise. The internal pre-amplifier in front of the ADC is responsible for most part of it. On-resistance of switches is a possible source of noise. From noise and linearity measure-

ments it is possible to evaluate the loss of resolution of the converter to at least 1 LSB in 16-bit mode.

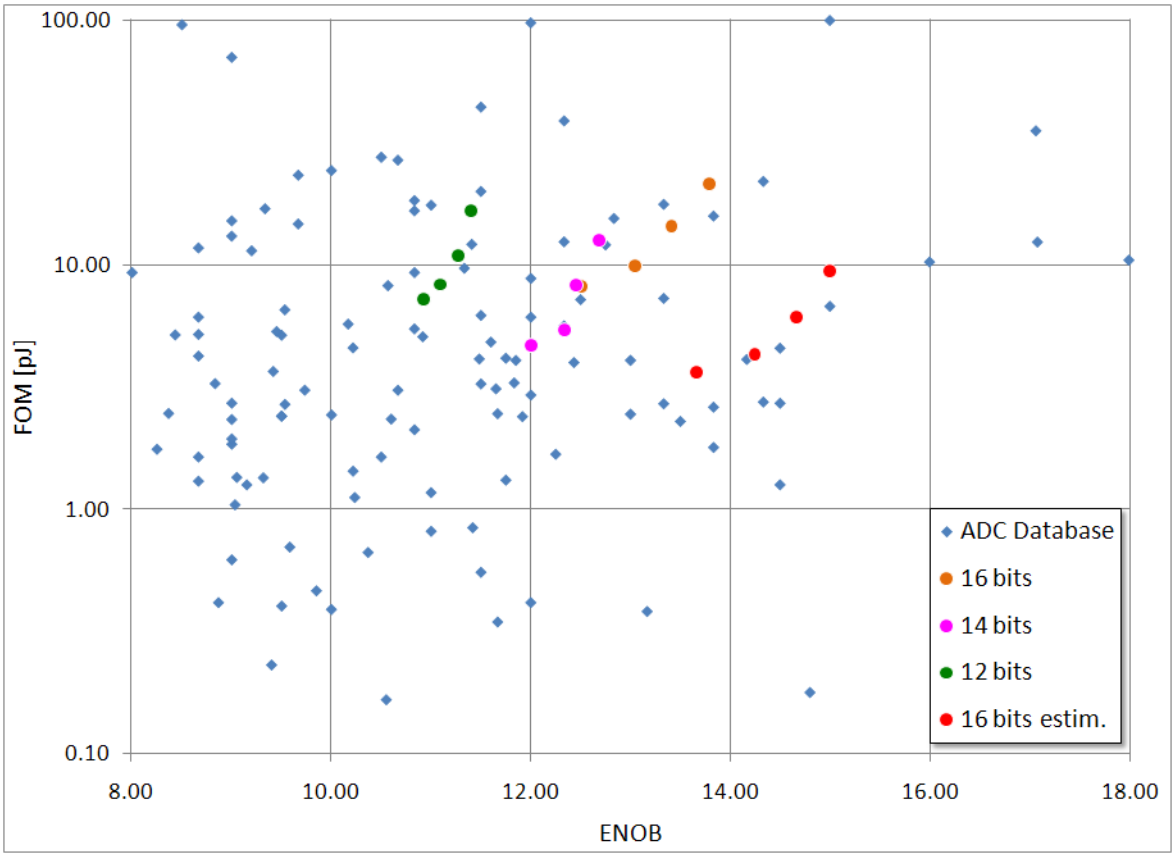

Figure 6.13 : FOM vs ENOB with the measured ADC and supposed value for the 16-bit ADC.

The efficiency of the ADC has been plotted in Figure 6.13 with the different configurations exactly as in Figure 1.10. A 16-bit configuration with an expected performance without noise from pre-amplifier is also plotted. Four mode for each resolution are plotted. The top-right point always represents the mode with the higher resolution with the incremental, as it can achieve an higher resolution.

For 12-bit of resolution, the ENOB is around 11 bits and the FOM around 10 pJ. The fact to allow more resolution to be solved by the cyclic converter is more efficient. From configuration 6-6 to 3-9, the loss

of ENOB is only 0.5 bit while the rate has tripled. However, in the chart, this solution seems not to be the most efficient one. Efficiency of state-of-the art converter are below 1 pJ. For the 14-bit configuration, the ENOB is above 12 bits and FOM is even better than for 12-bit. For the 16-bit configuration, the ENOB has a larger range between each mode. Considering the fact that for each increase of 1 bit of the ENOB, the FOM should increase of 2 for equal efficiency, the four modes are more or less identical in efficiency. The estimation of the 16-bit configuration without the noise of the preamplifier has been also plotted. ADC effective resolution is between 14 and 15 LSB and efficiency under 10 pJ. These values are relatively efficient and competitive with other solutions, with the benefit of a small circuit.

6.3 Second Realization

A four-sided printed circuit board (PCB) was fabricated to evaluate the performances of the circuit. All the digital signals are on the bottom layer of the PCB, while analog ones are on the top layer. An internal ground plate is provided to protect from electronic coupling. Four power supplies are generated on-board from an external source: a 3.3V digital power, a 3.3V IO power for the supply of the pad ring of the chip, a 3.3V analog power for analog power, reference and common-mode voltage and a 5V general purpose power.

Two separated biasing input are present with a potentiometer for the possibility of trimmering the current value. All power supplies and biasing are decoupled with $10\mu F$ and $100nF$ capacitors. The differential input is provided by two SMA connectors directly.

The differential input is generated by an AudioPrecision SYS-2322A[3]

[3] http://ap.com/

which can generate very low-distortion sine wave. The digital signal generation is ensured by a FPGA board Nova Engineering 20KE[4] with its own clock at 40 MHz. The board is plugged under the developed PCB. A logic analyzer from Intronix[5] is used for signal verification and data acquisition. This analyzer provides 34 sampled channels allowing to observe the multiple control signals. Data are transfered via USB to the PC for analyze manipulations.

6.3.1 Measurements

The measurements are compromised due to design errors during preliminary test on the chip. It appeared that the two comparators with the external threshold input are not working proprely and give erroneous results. This issue prevent to use the RSD-cyclic conversion and only incremental mode is functional. Another problem appeared when using the second-order incremental conversion. Integration with the two amplifiers are working correctly when they are separate but shows problems when intermediate voltage is connected to second integrator.

Noise

Noise on the incremental converter has been measured around 0.25 LSB of standard deviation with a 12 bits resolution.

SNDR vs input

The converter has been put in incremental mode with 12 bits of resolution. The SNDR is computed over 1'024 points, with a Hanning window. The SNDR has been measured versus the input signal power: the result is shown in Figure 6.14. It can be seen that the maximum SNDR is about 71dB, which is equivalent to 11.5 effective number of bit.

[4] http://www.nova-eng.com/Inside.asp?n=Products&p=Constellation20ke
[5] http://www.pctestinstruments.com/

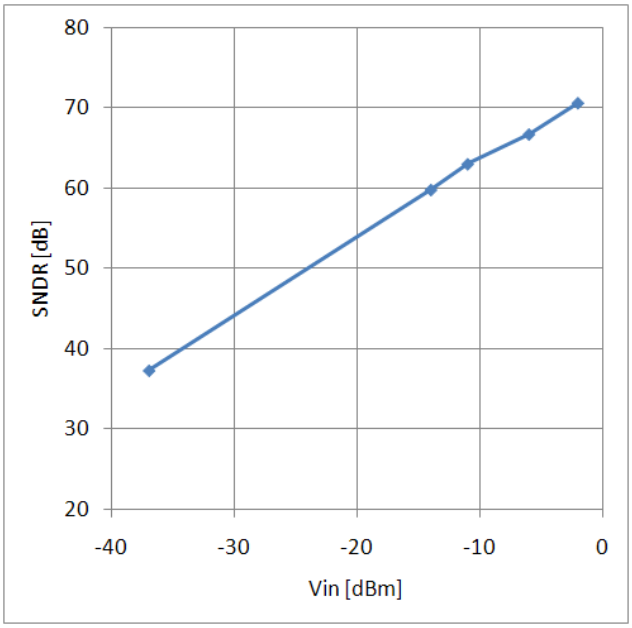

Figure 6.14 : SNDR versus input for the 12 bit integrator.

6.3.2 Discussion

Only first-order incremental mode could be measured. It shows good accuracy and low noise level.

The first error comes from the comparators connected to the external threshold. The converter has been configured to perform a simple one cycle integration and then comparison is performed on the output. Input voltage is swept on the whole range. The comparator used in the incremental mode is working fine, but not comparators connected to the external threshold. The output does not change, whatever the input voltage. As all the comparators are exacteley the same, the error is due to a bad intern connexion of the threshold signal.

The second problem appears when the second order mode is powered. First-order incremental mode with amplifier one or with amplifier two is working. Thus indicating that charge transfer of the two switched capacitor systems are working fine independentely. The problem appears

when the two systems are connected together. Transistor simulations shows normal behaviour and the only difference between measurments and simulation is the digital signals generation. An error in the digital control is the most probable reason to explain this error. Investigation has been performed in this direction but time has not allowed to determine the exact position of the problem.

6.4 Summary

This chapter presents the measurements of the two realizations integrated in a CMOS 0.18 μm. The first realization shows that the functionality of the first-order cascaded incremental and cyclic is achieved correctly. The circuit has a target resolution of 16 bit and a conversion frequency of 500 Hz. A maximum SNDR of 84.8 dB, equivalent to an ENOB of 13.8 bits, is measured. Power consumption is 150 μW with a 1.65 V supply. An efficiency around 10 pJ is achieved which is competitive with other solution for high resolution. The active area is 0.1 mm^2 and compared to other solution it is one of the most compact topology for ADC above 12 bits. Noise from an internal block and a non-optimal amplifier are reducing the performances.

The second circuit is unfortunately not working properly and it is not possible to evaluate the benefit of the second order implementation.

Bibliography

[1] M. Burns and G. Roberts, "An Introduction to Mixed-Signal IC Test and Measurement," 2001.

[2] J. Doernberg, H. S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," *Solid-State Circuits, IEEE Journal of*, vol. 19, no. 6, pp. 820–827, 1984.

Chapter 7

Conclusion

Summary

The main objective of this work was to explore the feasibility of a novel architecture for high resolution ADCs.

Basic ADC architectures are presented with their benefits and drawbacks. Families of ADCs are identified and their optimum performance range is observed. For high resolution, converters based on delta-sigma modulators are identified. The incremental converter, which work in transient mode, is a well suited converter for sensor application where high resolution, low power and low offset is required. Nevertheless this architecture present a big drawback: it is very slow.

This thesis discusses the improvement of the incremental converter. A new structure is proposed to reduce the number of cycles of the incremental converter. It uses the fact that at the end of the conversion the quantization error is available in analog form and it is possible to further use this signal to refine the resolution. The incremental stage extracts the most significant bits of the result, and produces an analog residual voltage. This voltage is then passed to a cyclic converter, which

extracts the least significant bits of the result. The cyclic conversion needs only one cycle per bit of resolution, thus reducing drastically the total conversion time. The main hardware can be re-used for the cyclic conversion. Only a few switches, two comparators and a small logic is required in addition.

Another architecture is proposed for reducing the conversion time. The second-order incremental, which can already reduce the conversion time is used in the same way. A cyclic conversion is used to convert the quantization error of the incremental conversion.

Theoretical analyzes of both conversion principle are provided and simulations based on theoretical are performed. For a 16-bit configuration, it appears that for a first order implementation the time required is divided by 100 with the cascading of a cyclic conversion. The use of a second order incremental divide the conversion time by 200 at a cost of doubled power consumption and if we combine second order incremental with cascading of cyclic conversion, the conversion rate is divided by 1000.

A practical implementation is presented, based on switched capacitors. Two circuits are realized: the first one with a first order incremental converter followed by a cyclic converter and the second with a second order architecture. The first circuit has a target resolution of 16 bit and a conversion frequency of 500 Hz. A maximum SNDR of 84.8 dB, equivalent to an ENOB of 13.8 bits, is measured. Power consumption is 150 μW with a 1.65V supply. Different modes were tested showing a great flexibility with resolution and speed. Noise from an internal block and a non-optimal amplifier are reducing the performances. The targeted 16 bits has not been reached but the main limiting factors identified and it is very promising for a future redesign. The second circuit is unfortunately not working properly and it is not possible to evaluate

the benefit of the second order implementation.

The main contribution of this work is that it is possible to use the cascade of an incremental and a cyclic converter to reduce the conversion time of pure incremental ADCs. Two implementations have been developed and theoretical aspect has been analyzed.

Depending on the power- and area-consumption and the desired resolution, the family of converter to be used can be different:

- If medium to high resolution (10-16 bits) is needed, and the main requirement is to minimize the chip, then a first-order incremental with cyclic converter is usually optimal.

- If the main goal is to achieve high resolution (over 14 bits) with a reasonable speed and circuit complexity is less critical, a second-order incremental converter with cyclic may be eligible.

Nevertheless, depending on other requirements, choice of architecture is flexible.

Compared to other solution, the power efficiency of this architecture is competitive. The active surface of the converter, with 0.1 mm^2, is one of the most compact solution that we can find in literature with ADC over 12 bits of effective resolution. Only one ADC present a smaller surface with 0.06 mm^2 with a 13 bits of effective resolution [1]. The design complexity is also minimal. Even for second-order implementation,

digital filtering is extremely simple.

Contributions

The main contributions of this thesis are:

- A modification of the first order incremental converter by refining the quantization error by a cyclic converter. By this way the required conversion time to achieve a given resolution is considerably reduced while keeping the same power consumption.

- A modification of the second order incremental converter by applying in the same way, with a reuse of the quantization error by a cyclic converter. With a doubling of the complexity and the power, conversion time can be even further reduced.

- Same hardware for incremental and cyclic. The switched-capacitor implementation, composed of an amplifier, capacitors and comparators can be used by both conversion scheme. Complexity of the architecture is not increased by this new topology. The benefit is a very compact implementation.

- An inversion process of the residue voltage is proposed with a fully differential structure. The inversion needs 3 capacitors and 3 cycles. First order mismatch of capacitors are removed. By this way, it is possible to perform this inversion of the residue voltage in the middle of the incremental conversion to cancel the offset of the amplifier.

Future work

Further analysis of the proposed structure can be interesting to better characterize the architecture. Even though most influent imperfections has been taken into account, some of them are missing. In Matlab simulation, a static model of the converter was considered. A dynamic one with imperfection such as finite bandwidth of the amplifier may be useful.

On a practical way, the limitations of the second implementation have to be understood. It would be very interesting to know the performances of this architecture and compare it with a first order solution.

On a system level, a possible way to enhance the conversion rate is to use different or higher order modulator. Conversion time required by incremental conversion can be reduced even more. Conventional linear filtering is used here, however this is not the most efficient way. Recent research have shown that knowledge of the transfer function of the modulator can lead to design an optimal filter that can achieve the same performance as that of conventional $\Delta - \Sigma$ systems at lower oversampling ratio and hence lower power consumption. Digital filtering can also be used to suppress line frequency.

On a circuit level, it may be interesting to test some other design choices. Is it better to use a different amplifier topology to reduce power consumption. Digital is designed to provide a flexible configuration with multiple resolution. It is possible to reduce flexibility in order to reduce the size of digital part. Timing of switches is achieved by a high

frequency clock which is divided by 16. A clock frequency equal to sampling frequency and with internal delay to produce the different timing could be advantageous to increase the settling time of the amplifier.

Bibliography

[1] J. Goes, B. Vaz, R. Monteiro, and N. Paulino, "A 0.9V Delta-Sigma Modulator with 80dB SNDR and 83dB DR Using a Single-Phase Technique," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, 2006, pp. 191–200.

Appendix A

ADCs for comparison

A.1 Data

Reference	Res.	Type	Year	Rate	Power	Area	SNDR	Techno	ENOB	FOM
	[bits]			[MS/s]	[mW]	$[mm^2]$	[dB]	$[\mu m]$	[bits]	[pJ]
[1]	6	Flash	2001	1300	545	4.8	32	0.35	5.02	12.9
[2]	6	Flash	2002	21.73	0.48	0.3	33	0.13	5.19	0.61
[3]	6	SAR	2004	600	10	-	31	0.09	4.86	0.58
[4]	5	Flash	2004	10000	3600	9	26	0.18	4.03	22.09
[5]	4	Flash	2006	1250	2.5	-	23.8	0.09	3.66	0.158
[6]	4	Flash	2007	4000	608	0.88	22.7	0.18	3.48	13.61
[7]	5	Folding	2008	1750	2.2	0.017	27.6	0.09	4.29	0.064
[8]	8	Pipeline	1993	85	1100	25	41	1	6.52	144.2
[9]	8	Two-step	1993	13.5	150	2.9	44	1	7.02	85.8
[10]	8	Flash	1994	25	250	2.8	46	1	7.35	61.3
[11]	8	Folding	1995	45	45	0.7	44	0.8	7.02	7.72
[12]	8	Pipeline	1995	52	250	15	46	0.9	7.35	29.5
[13]	8	Folding	1996	80	80	0.3	44	0.5	7.02	7.72
[14]	8	Cyclic	1998	4.2	4	2	45	1	7.18	6.56
[15]	8	SAR	2000	0.05	0.34	3.2	49	1.2	7.85	29.5
[16]	8	Folding	2001	10	76	5	48	0.35	7.68	37.0
[17]	8	Pipeline	2001	80	268	10.3	43.8	0.5	6.98	26.5
[18]	8	SAR	2002	0.1	0.0046	0.053	47.8	0.25	7.65	0.229
[19]	8	SAR	2003	0.0041	0.00085	0.11	43.3	0.18	6.90	1.74
[20]	8	Folding	2004	2000	3500	12.25	46.6	-	7.45	10.0
[21]	8	Two-step	2004	125	21	0.09	47.5	0.13	7.60	0.867
[22]	8	Folding	2004	1600	774	3.6	45.7	0.18	7.30	3.07
[23]	8	SAR	2006	1.23	1.6	0.1418	49.4	0.5	7.91	5.39
[24]	8	SAR	2007	0.2	0.00247	0.062	47.4	0.18	7.58	0.064
[25]	8	Pipeline	2007	200	8.5	0.05	40.2	0.18	6.39	0.508
[26]	8	Pipeline	2008	10	2.4	0.85	48.1	0.09	7.70	1.16

Reference	Res.	Type	Year	Rate	Power	Area	SNDR	Techno	ENOB	FOM
	[bits]			[MS/s]	[mW]	[mm^2]	[dB]	[μm]	[bits]	[pJ]
[27]	7	Two-step	2008	150	0.133	0.055	39.7	0.09	6.30	0.011
[28]	10	Pipeline	1992	20	240	8.7	60	0.9	9.67	14.69
[29]	10	Two-step	1993	20	30	6.5	55	0.8	8.84	3.26
[30]	10	Pipeline	1994	0.55	20	2.5	56	2.4	9.01	70.53
[31]	10	Two-step	1994	20	135	7	56	0.8	9.01	13.09
[32]	10	Pipeline	1995	20	35	10.5	59	1.2	9.51	2.40
[33]	10	Two-step	1995	20	20	12.1	56	0.5	9.01	1.94
[34]	10	Pipeline	1995	40	85	4	54	0.8	8.68	5.19
[35]	10	Pipeline	1995	20	50	13	54	1.2	8.68	6.10
[36]	10	Folding	1997	50	240	1	54	0.5	8.68	11.72
[37]	10	Pipeline	1997	100	1100	50	58	1	9.34	16.95
[38]	10	Other	1998	0.2	7	5.5	53	0.6	8.51	95.90
[39]	10	Two-step	1999	25	195	0.66	56	0.35	9.01	15.13
[40]	10	Pipeline	1999	14.3	36	5.75	58.5	0.6	9.43	3.66
[41]	10	Pipeline	1999	2.5	3	1.1	56	1	9.01	2.33
[42]	10	Pipeline	1999	25	45	2.21	52.6	0.25	8.45	5.16
[43]	10	Subranging	1999	20	75	1.6	58.7	0.5	9.46	5.33
[44]	10	Pipeline	2000	40	70	2.6	59	0.35	9.51	2.40
[45]	10	SAR	2000	0.5	1	1.26	59.2	0.25	9.54	2.68
[46]	10	Pipeline	2001	200	280	7.4	56	0.5	9.01	2.72
[47]	10	Pipeline	2003	30	16	3.12	54	0.3	8.68	1.30
[48]	10	Pipeline	2003	25	21	2.24	48	0.35	7.68	4.09
[49]	10	Pipeline	2003	80	69	1.85	57.9	0.18	9.33	1.34
[50]	10	Pipeline	2003	120	208	3.6	54	0.25	8.68	4.23
[51]	10	Pipeline	2004	40	11.7	0.7	59	0.25	9.51	0.40
[52]	10	Pipeline	2004	150	123	2.2	52.2	0.18	8.38	2.46
[53]	10	Pipeline	2004	100	67	2.52	54	0.18	8.68	1.64
[54]	10	Cyclic	2005	5	12	1.4	50		8.01	9.29
[55]	10	Pipeline	2006	100	72	0.54	56.3	0.13	9.06	1.35
[56]	10	Pipeline	2006	20.5	19.5	1.3	56	0.35	9.01	1.85
[57]	9	SAR	2007	20	0.29	1.31	46.5	0.09	7.43	0.084
[58]	10	Pipeline	2007	30	4.7	0.32	58.4	0.09	9.41	0.23
[59]	10	Pipeline	2007	205	40	1	55.2	0.09	8.88	0.41
[60]	10	Pipeline	2008	30	21.6	0.7	56.91		9.16	1.26
[61]	9	SAR	2008	40	0.82	0.09	51.3	0.09	8.23	0.068
[62]	10	Pipeline	2008	100	4.5	0.1	59	0.065	9.51	0.062
[63]	10	Two-step	2008	60	19.2	0.98	56	0.13	9.01	0.62
[64]	10	SAR	2008	0.08333	0.0019	0.035	54.5	0.065	8.76	0.053
[65]	10	SAR	2008	0.1	0.0038	0.24	55	0.18	8.84	0.083
[66]	10	Pipeline	2008	50	27	1.21	51.5	0.18	8.26	1.76
[67]	12	Pipeline	1988	1	400	14	74	1.75	12.00	97.66
[68]	12	Two-step	1992	5	200	3.6	65	1	10.50	27.53

Reference	Res.	Type	Year	Rate	Power	Area	SNDR	Techno	ENOB	FOM
	[bits]			[MS/s]	[mW]	[mm^2]	[dB]	[μm]	[bits]	[pJ]
[69]	12	Two-step	1996	1	25	5	70	1	11.34	9.67
[70]	12	Pipeline	1996	10	250	15	62	0.8	10.01	24.30
[71]	12	Pipeline	1996	5	33	17.2	63	1.2	10.17	5.72
[72]	12	Folding	1997	60	300	7	66	1	10.67	3.07
[73]	12	Pipeline	1998	20	250	9.9	65.4	0.7	10.57	8.21
[74]	12	Pipeline	1998	10	335	14.5	67	0.5	10.84	18.31
[75]	12	Other	1999	0.8	1.9	2.13	65	2	10.50	1.63
[76]	12	Other	1999	0.125	16	5.9	71	1.5	11.50	44.14
[77]	12	Pipeline	1999	20	135	2.57	57.2	0.35	9.21	11.40
[78]	12	Two-step	2000	50	850	16	67	0.6	10.84	9.29
[79]	12	Delta-sigma	2000	12.5	380	5.34	67	0.65	10.84	16.62
[80]	12	Two-step	2001	54	295	1	63.3	0.25	10.22	4.57
[81]	12	SAR	2001	1	15	1.5	71.6	0.6	11.60	4.83
[82]	12	Pipeline	2002	30	48		71	0.35	11.50	0.55
[83]	12	Pipeline	2002	61	600		67.5	0.35	10.92	5.08
[84]	12	Pipeline	2002	21	35	2.5	68	0.6	11.00	0.81
[85]	12	Delta-sigma	2002	0.008	0.08	0.082	67	0.18	10.84	5.47
[86]	12	Delta-sigma	2003	4	4.5	0.55	72	0.18	11.67	0.35
[87]	12	Pipeline	2003	75	290	7.9	67	0.35	10.84	2.11
[88]	12	Pipeline	2005	80	755	22.6	71	0.25	11.50	3.25
[89]	12	Two-step	2005	0.03125	0.075	0.45	68	0.35	11.00	1.17
[90]	12	Pipeline	2005	110	97	0.86	64.2	0.18	10.37	0.67
[91]	12	SAR	2006	0.2	6.6	2	70.45	0.13	11.41	12.12
[92]	12	Pipeline	2006	120	315	1.03	60.4	0.13	9.74	3.07
[93]	12	Delta-sigma	2006	40	68	8.6	74	0.13	12.00	0.42
[94]	12	Pipeline	2006	100	55	5.78	56.2	0.09	9.04	1.04
[95]	12	Pipeline	2007	40	16	0.28	62	0.09	10.01	0.39
[96]	12	Pipeline	2007	75	273	7.9	65.6	0.35	10.60	2.34
[97]	12	SAR	2007	0.1	0.025	0.63	65.3	0.18	10.55	0.17
[98]	12	Delta-sigma	2007	0.05	0.027	0.11	59.5	0.09	9.59	0.70
[99]	12	Cyclic	2007	0.04	0.0684	0.041	63.3	0.13	10.22	1.43
[100]	12	Pipeline	2008	120	51.6	0.56	61.1	0.13	9.86	0.46
[101]	12	Delta-sigma	2008	2	2.7	0.42	63.4	0.25	10.24	1.12
[102]	13	Pipeline	1995	10	360	33.4	68	1.4	11.00	17.54
[103]	13	Pipeline	1996	5	166	28	80	1.2	13.00	4.06
[104]	13	Cyclic	1995	0.016	0.06	1.17	59	2	9.51	5.15
[105]	13	Other	1999	18	324	47.6	71	1.2	11.50	6.21
[106]	13	Delta-sigma	1999	2.2	55	1.3	74	0.7	12.00	6.10
[107]	13	Pipeline	2004	16	78	12.24	59.2	0.25	9.54	6.54
[108]	13	Delta-sigma	2005	20	240	4	73	0.18	11.83	3.29
[109]	13	Delta-sigma	2006	0.025	0.3	0.6	74	0.18	12.00	2.93
[110]	14	Incremental	1983	0.05	450	10	84		13.66	694.76

Reference	Res.	Type	Year	Rate	Power	Area	SNDR	Techno	ENOB	FOM
	[bits]			[MS/s]	[mW]	[mm^2]	[dB]	[μm]	[bits]	[pJ]
[111]	14	Pipeline	1996	2.5	500	23.7	76	2	12.33	38.78
[112]	14	Delta-sigma	1998	1.4	81	3.51	71	0.72	11.50	19.95
[113]	14	Delta-sigma	2000	2.2	248	4.3	79	0.35	12.83	15.48
[114]	14	Pipeline	2000	5	145	10	76	0.6	12.33	5.62
[115]	14	Pipeline	2000	5	320	10.9	76	0.5	12.33	12.41
[116]	14	Pipeline	2001	20	720	10.8	74	0.5	12.00	8.79
[117]	14	Pipeline	2001	75	340	7.8	72.5	0.35	11.75	1.32
[118]	14	Delta-sigma	2001	0.025	0.95	0.63	85	0.35	13.83	2.61
[119]	14	Delta-sigma	2002	0.18	5	0.4	82	0.4	13.33	2.70
[120]	14	Pipeline	2002	10	220	12.5	76.6	0.5	12.43	3.98
[121]	14	Pipeline	2003	70	1000	28.1	72.5	0.4	11.75	4.15
[122]	14	Delta-sigma	2004	25	200	0.95	72	0.18	11.67	2.46
[123]	14	Delta-sigma	2004	2	150	2.9	82	0.18	13.33	7.29
[124]	14	Pipeline	2004	12	98	10	75.5	0.18	12.25	1.68
[125]	14	Delta-sigma	2005	0.024	1	2.88	77	0.35	12.50	7.20
[126]	14	Pipeline	2006	80	1200		73.1	0.35	11.85	4.06
[127]	14	Delta-sigma	2007	2.2	182.5	2.8	78.5	0.25	12.75	12.06
[128]	14	Other	2007	2.5	66	0.55	83	0.13	13.50	2.29
[129]	14	Pipeline	2008	100	230	7.28	70.5	0.18	11.42	0.84
[130]	16	Incremental	1988	0.0001	0.325		92	3	14.99	99.87
[131]	15	Two-step	1997	5	130	27	85	1.4	13.83	1.79
[132]	15	Delta-sigma	1998	1	230	5.25	85	1	13.83	15.82
[133]	15	Delta-sigma	1999	1.1	200	5.06	82	0.5	13.33	17.67
[134]	15	Other	2001	0.02	9	80	88		14.33	21.92
[135]	15	Pipeline	2001	20	380	13.8	60	0.5	9.67	23.25
[136]	15	Other	2004	0.5	48	0.7	81	0.6	13.16	10.47
[137]	15	Pipeline	2004	40	400	20	71.9	0.18	11.65	3.11
[138]	15	Pipeline	2005	40	370	13.7	73.5	0.25	11.92	2.39
[139]	15	Delta-sigma	2008	0.024	0.121	0.72	90.8	0.18	14.79	0.18
[140]	16	Delta-sigma	1997	2.5	550	35.3	92	0.6	14.99	6.76
[141]	16	Delta-sigma	1998	0.016	0.04	0.85	62	0.5	10.01	2.43
[142]	16	Delta-sigma	2000	0.27	11.8	1.6	66	0.5	10.67	26.80
[143]	16	Delta-sigma	2001	2	150	10	87	0.5	14.16	4.10
[144]	16	Delta-sigma	2003	0.04	68	5.61	104.5	0.35	17.07	12.39
[145]	16	Delta-sigma	2004	1.1	62	5.76	88	0.5	14.33	2.75
[146]	16	Delta-sigma	2004	0.04	0.14		81	0.09	13.16	0.38
[147]	16	Delta-sigma	2004	0.02	300	12.6	111	0.35	18.15	51.71
[148]	16	Delta-sigma	2005	0.048	32	1.82	98	0.35	15.99	10.27
[149]	16	Cyclic	2005	1	105	1.6	89	0.25	14.49	4.56
[150]	16	Delta-sigma	2005	3	87	8.6	89	0.25	14.49	1.26
[151]	16	Delta-sigma	2006	0.01	0.2	0.06	80	0.18	13.00	2.45
[152]	16	Delta-sigma	2008	0.024	1.5	1.44	89	0.13	14.49	2.71

Reference	Res.	Type	Year	Rate	Power	Area	SNDR	Techno	ENOB	FOM
	[bits]			[MS/s]	[mW]	$[mm^2]$	[dB]	$[\mu m]$	[bits]	[pJ]
[153]	19	Delta-sigma	1997	0.001	2.7		116		18.98	5.23
[154]	20	Delta-sigma	2003	0.048	230	10	104.4	0.35	17.05	35.32
[155]	22	Incremental	2006	0.000015	0.6	2.08	120	0.6	19.64	48.92
[156]	22	Incremental	2004	0.000015	0.75		131.5		21.55	16.27

Table A.1 : ADC Database.

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Appendix B

Abbreviations

ADC	Analof-to-Digital Converter
Cox	Gate oxyde capacitance
CIFF	Cascaded-Integrators Feed-Forward
CMFB	Common-Mode Feed-Back
DAC	Digital-to-Analog Converter
DNL	Differential Non-linearity
ENOB	Effective Number Of Bits
FFT	Fast Fourrier Transform
FOM	Figure Of Merit
FPGA	Field Programmable Gate Array
FS	Full-Scale
GBW	GainBandWidth
IC	Inversion Coefficient
INL	Integral Non-linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
OSR	Over Sampling Ratio
RMS	Root Mean Square
RSD	Redundent Signed Digit

SAR	Successive Approximation Register
SNDR	Signal-to-Noise plus Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System on Chip
THD	Total Harmonic Distortion
$\Delta - \Sigma$	Delta-Sigma

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- L. Rossi, S. Tanner and P.-A. Farine, "A 16-bit, 150-μW, 1-kS/s ADC with hybrid incremental and cyclic conversion scheme", *IEEE International Conference on Electronics, Circuits, and Systems, ICECS, Medina, Tunisia, Dec. 13-16, 2009*, pp. 751-754, 2009.

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