Rui Ma

Reliable RF Power Amplifier Design Based on a Partitioning Design Approach

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To my family and my little son

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Rui Ma

Kassel, December 2009

Contents

List of Abbreviations and Acronyms

3G, 4G	Third Generation, Fourth Generation
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
BTS	Base Transceiver Station
CAD	Computer Aided Design
CW	Continuous Wave
DC	Direct Current
DiVA	Dynamic I(V) Analyzer
DUT	Device Under Test
EER	Envelope Elimination and Restoration
ESR, ESL	Equivalent Series Resistor, Equivalent Series Inductor
FD, FDTD	Finite Difference, Finite Difference in Time Domain
FEM	Finite Element Method
FET	Field Effect Transistor
GaAs, GaN	Gallium Arsenide, Gallium Nitride
HEMT	High Electron Mobility Transistor
IMD	Intermodulation Distortion
IMD3	Third Order Intermodulation Distortion
LSM	Large Signal Model
LTE	Long Term Evolution
MIC	Microwave Integrated Circuit
MoM	Method of Moment
PA	Power Amplifier
PAE	Power Added Efficiency
PAR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PDA	Partitioning Design Approach
RF	Radio Frequency
SDD	Symbolically Defined Device
SMD	Surface Mounted Device
SSM	Small Signal Model
THLR	Through, High and Low Reflection
TRL	Through, Reflection, Line
UMTS	Universal Mobile Telecommunication System
VNA, VSA	Vector Network Analyzer, Vector Signal Analyzer
WCDMA	Wideband Code Division Multiple Access

Abstract

In this research work, a novel RF circuit design concept, namely partitioning design approach, is proposed and successfully demonstrated. It is aimed to accomplish the reliable RF circuit design task in a straightforward way. Within the conventional design approach, circuit is realized in a single fabrication step after finishing the design procedure using CAD simulation software. However, it happens in practice very frequently that the measured circuit performance does not acceptably fit to the specifications predicted by simulation during its initial fabrication. Consequently, iterative post-fabrication tuning work has to be performed to find out the causes of the discrepancy, which is considerably experience-based. Moreover, circuit very often has to be modified and re-fabricated in several rounds to meet the design target. Thus, the entire design cycle and development cost are further increased.

In contrast to it, proposed partitioning design approach systematically decomposes a complex design task into small-sized, well-controllable and verifiable sub-tasks. It can provide RF designer the direct access to check each sub-part design in reality, thus to gain the detailed and true picture of every individual part from its corresponding measurement verification. The demonstrator of a class-AB RF power amplifier using AlGaAs/GaAs HEMT technology and operating at 2.14 GHz center frequency is designed following the proposed design strategy. The final entire power amplifier is therefore assembled through interconnecting each individually designed, fabricated, and measurement-verified sub-part. The critical factor of the interconnection technology is deeply tackled with investigation and comparison of versatile techniques in practice. For design purpose, nonlinear large-signal transistor chip model has been developed, and involved passive SMD components have been characterized and thoroughly analyzed as well. Individual sub-part design and the related problems have been discussed in a great detail. In the course of the demonstrator design, the importance and advantages of the missing link between simulation and measurement caught up by the partitioning design approach are clearly shown. At the end, outstanding comparison results between the constructed entire power am-

plifier measurement and its simulation predication fairly demonstrate the viability of partitioning design approach for achieving first-pass success in RF power amplifier design in an efficient manner.

Zusammenfassung

In der vorliegenden Arbeit wurde ein neuartiges Entwurfskonzept für Hochfrequenzschaltungen, bei dem eine komplexe Schaltung in ihre grundlegenden Bestandteile zerlegt wird (Partitioning Design Approach), erarbeitet und erfolgreich angewendet. Ziel des Verfahrens ist es, das Entwurfsziel auf direktem Wege und ohne zeit- und kostenintensive iterative Prozesse zu erreichen. Im konventionellen Entwurfskonzept wird die Schaltung nach dem Design und der Simulation in einem Schritt gefertigt. Dabei weichen die gemessen Parameter häufig von den gewünschten und von der Simulation vorhergesagten Daten ab. Daher muss die Schaltung in einem iterativen Prozess mehrfach angepasst und neu gefertigt werden, um das gewünschte Verhalten zu erreichen. Dieser Prozess erfordert neben viel Erfahrung auch eine mehrfache, kostenintensive Neufertigung.

Im Gegensatz dazu wird eine komplexe Entwurfsaufgabe beim aufgeteilten Konzept systematisch in kleine, leicht kontrollierbare und überprüfbare Teilaufgaben unterteilt. Diese Aufteilung ermöglicht einen direkten Zugriff auf einzelne Schaltungsteile, und führt dadurch zu einem genauren Verständnis der Gesamtschaltung. Die Demonstration erfolgte an einem 2,14 GHz Hochfrequenz-Leistungsverstärker der Klasse AB in AlGaAs/GaAs HEMT Technologie. Dieser wurde aus einzeln entworfenen, hergestellten und überprüften Teilschaltungen aufgebaut. Dabei tritt als kritischer Faktor die Verbindungstechnologie auf. Dazu wurden ausführliche Untersuchungen angestellt und verschiedene Möglichkeiten durch Versuche verglichen. Zu Entwurfs- und Simulationszwecken wurde ein nichtlineares Großsignalmodell des verwendeten Transistor Chips entwickelt und ausführlich getestet. Ebenso wurden die verwendeten passiven SMD Komponenten charakterisiert und ausführlich analysiert. Der Entwurf der einzelnen Schaltungsteile und die entstandenen Schwierigkeiten wurden ausführlich diskutiert. Im Verlauf der Entwicklung der Demonstrationsschaltung konnten die Vorteile des aufgeteilten Entwurfs, der in den einzelnen Designschritten eine Übereinstimmung von Simulation und Messung gewährleistet, verdeutlicht werden. Insbesondere zeigt die am Ende zusammengesetzte Schaltung die erwarteten elektrischen Eigenschaften, was nochmals die Wirksamkeit und Leistungsfähigkeit der hier vorgestellten Designmethode untermauert.

Chapter 1

Introduction

RF power amplifier (PA) is one of the key blocks in any radio transmitters. It has a crucial influence on the entire system performance in terms of output power, efficiency, as well as linearity [1]. With the rapid development of present 3G UMTS-LTE and future 4G (LTE-Advanced) broadband wireless communications, advanced power amplifiers with complex architectures (such like Doherty, EER, Outphasing, and Derivative superposition) have to be adopted in order to compile with the rigorous radio specifications [2-6]. However, design of these complex modern power amplifiers is exceedingly challenging RF circuit designers due to their increased circuit complexity.

To date, in practice it has been shown that circuit designers are continuously encountering numerous troubles and difficulties to obtain the first-pass success power amplifier design following the conventional design method [7-8]. As illustrated in Figure 1.1, in this design methodology essential bias networks and matching networks (and other sub-circuits, *i.e.* stabilization networks, if necessary) are designed using CAD simulation software based on the targeted impedances (obtained through either source- / load-pull measurement or CAD simulation), and then the performance of the designed complete power amplifier is simulated. Afterwards, the whole circuit is fabricated on one layout at one step. However, what comes out very frequently is that the measured real performance of the fabricated circuit does not satisfactorily meet the targeted RF specifications shown in the simulation [7-9]. Thereafter, additional

development time and effort must be invested to locate the true causes for the deviations in the circuit characteristics.

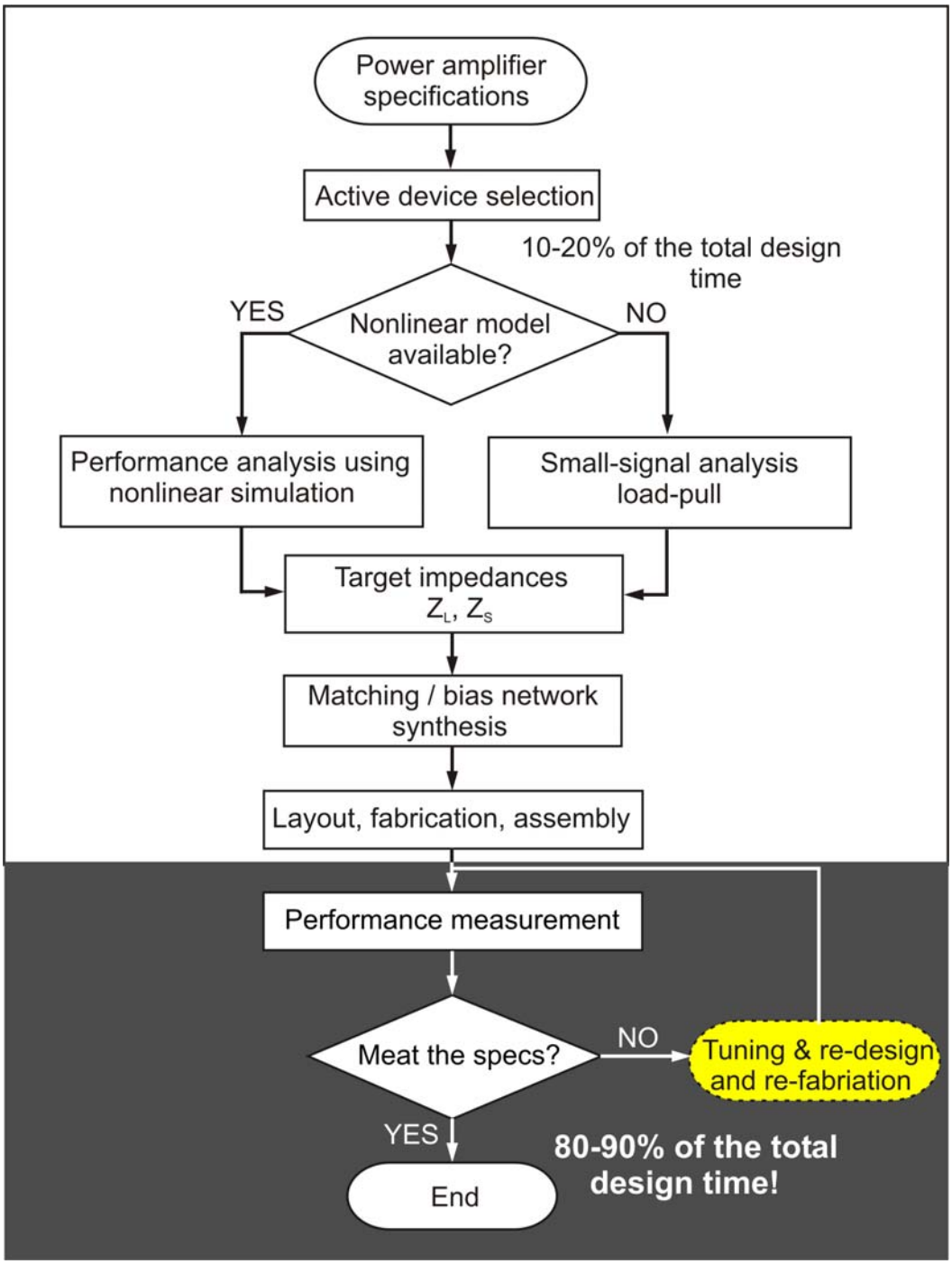


Figure 1.1 Conventional design methodology for power amplifier design [8].

In reality, there are indeed manifold possible factors causing those deviations, some of which are briefly listed as follow [9]:

1. Model accuracy of the active transistor device and versatile mounting and coupling effects from the final mounted application environment.

2. Model reliability concerning the passive component and its mounting parasitic effects.
3. Availability of the precise substrate parameters.
4. Correct modeling of the discontinuities and ground effects involved in the final realized circuit.
5. Proper consideration of thermal and packaging influences.
6. In addition, variation of technology tolerance and hand-manufacturability.

For the mentioned reasons, much time-consuming empirical post-fabrication tuning work has to be performed. Very often, re-design and re-fabrication cannot be avoided, which greatly increases the design cycle and cost.

Obviously, the situation becomes even much more challenging while designing complex architecture RF power amplifiers following this conventional one-step design method. Design difficulties are dramatically increased mainly owing to the *complex inter-action between multiple devices and sub-circuits* involved in these architectures, besides the possible reasons listed above [10 -11]. Hence, the iterative trial-and-error based conventional design approach appears rather powerless in these harder situations. It is clear that effective use of CAD design tools can only be possible under combination with an insightful design methodology to tackle the design tasks. Thus, RF designers need a new powerful design approach, which acts as a reliable and efficient methodology to accomplish the complex power amplifier architecture design and to deliver the expected results faster [12-16].

The developed partitioning design approach in this dissertation is a novel design methodology, which can highly facilitate the design procedure of complex architecture power amplifiers. It is able to effectively eliminate lengthy build-and-try iterations and to verify the final performance of the power amplifier circuit by measuring the performance already during the design stage [17]. This is, in particular, valid for the reliable design of prototypes amplifier. Furthermore, it addresses new technologies and respective new devices (e.g. GaN HEMT), for which the processing has not yet reached the desired maturity for mass production. In this case, as known from industry [18-19], the potential performance of a device is usually analyzed in the circuit level by careful

evaluation of a limited amount of typical transistors, with individually fine-tuned specific demonstration circuits. At this stage, partitioning design approach appears to be a powerful tool to construct a reliable test environment and it greatly assists the industry to minimize the time-to-market.

1.1 Principle of the Partitioning Design Approach

Partitioning design approach is aimed to systematically segment the complete circuit design into small-sized and well-controllable sub-parts. Following this fully flexible design method, each sub-part design can then be separately characterized and verified by measurement. In comparison with the aforementioned one-step conventional design approach, the proposed innovative multi-step design methodology gives the designer direct access to the interior of complex design problems and afterwards to fully control and confirm each intermediate design step. Thus, causes for performance deviations can be discovered earlier in the local part and can be trimmed rather easily. After the successful verification of the performance of any sub-module, the final circuit is assembled via interconnecting the fabricated individual blocks. It can be seen that the developed partitioning design approach can provide an unequivocal guide throughout the entire design process. Hence, it can guarantee the reliable design to be accomplished in a prompt straightforward way avoiding the time- and cost-intensive final post-fabrication tuning work.

The basic principles of the partitioning design approach are concisely illustrated in Figure 1.2 on the basis of a simple single-ended amplifier with input and output matching networks and respective bias networks. The transistor chip is wire-bonded, and characterized in a 50Ω environment (reference impedance may also differ from 50Ω) at the reference planes 1 and 2 very close to the transistor, including the bonding and mounting effects (see Figure 1.2(a)). The bias and matching networks are then designed to achieve the design specifications. The individually designed and fabricated bias networks and matching networks will be verified separately at the measurement planes shown in Figure 1.2(b) and Figure 1.2(c). After successful verification, the individually treated sub-blocks are interconnected to compose the final complete amplifier

(Figure 1.2(d)). Based on the full confidence of the design of each sub-block and the reliability of the interconnection technique employed, first-pass success design of the final entire power amplifier circuit can be obtained directly.

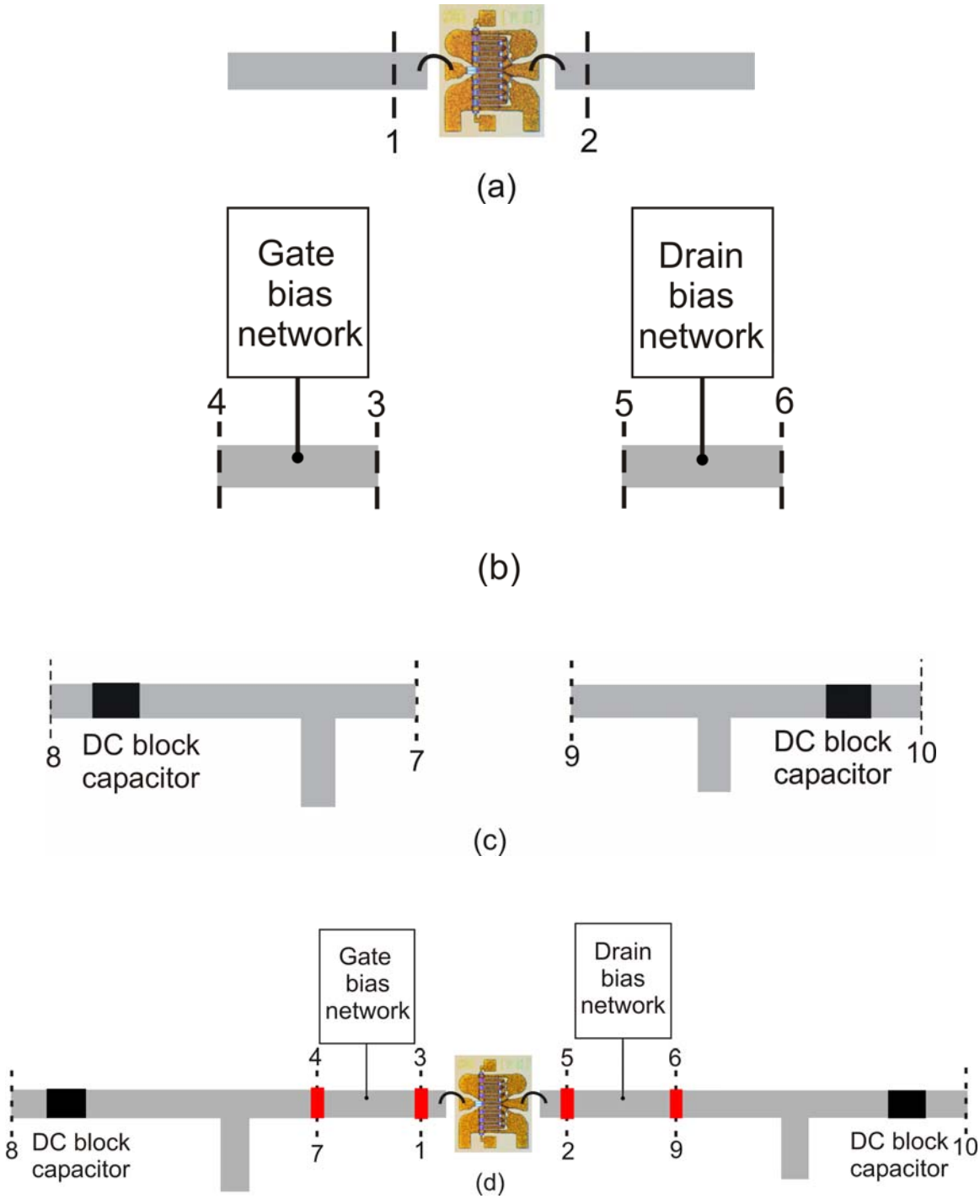


Figure 1.2 Amplifier design sequence demonstrating the principle of partitioning design approach: (a) Wire-bonded active device characterization and modeling, (b) bias network design, (c) matching network design, and (d) final assembly of the complete amplifier by planar interconnection of different blocks.

Some of initial ideas of partitioning design approach were already proposed in Cheng's work focusing on designing low-noise K band oscillator [20]. Regarding the critical interconnection technology, it was mainly analyzed on the simulation level. Practical feasibility, reproducibility, and reliability of different interconnection technologies still need further investigation. Furthermore, a complete detailed partitioning design procedure, which could be easily followed by designers, was not provided in this work.

1.2 Dissertation Organization

The overriding objective of this dissertation is to develop a new reliable RF power amplifier design method, through which designer can achieve the design specifications in an efficient and systematic way without iterative and tedious post-fabrication tuning procedures. Hence, issues and steps composing this proposed partitioning design approach will be tackled in great details in the following chapters. The dissertation is therefore sectioned into six chapters. In Chapter 1, the limitations and shortcomings of currently applied conventional design approach have been discussed. Moreover, motivation of developing a novel design methodology for reliable RF power amplifier design has been clearly addressed.

The success of the partitioning design approach depends strongly on the feasibility of high-quality and well reproducible interconnections between each individual designed sub-parts of the complete circuit. Therefore, planar-interconnection technologies will be thoroughly investigated both theoretically and experimentally in Chapter 2. Practical parasitic effects and potential troubles for active chip device mounting will be addressed first. The effects resulted from wire bonding for connecting the transistor chip pads to the peripheral transmission lines (in this case, microstrip line) will be analyzed. Versatile interconnection techniques for sub-circuit interconnection will be thoroughly investigated and compared with experiments, and one optimal technique will be chosen.

Passive components are definitely playing an important role in the fabrication of hybrid integrated RF circuits, with significance for RF power amplifier application. Within this partitioning design approach, it is a must to get to know the real performance of the specific passive SMD (**S**urface **M**ounted **D**evice) components adopted, and to master their real-world characteristics in the environment of final circuit. Analysis and modeling of adopted SMD passive components will be highlighted in Chapter 3.

Chapter 4 continues with the development of a nonlinear large-signal model for a 1.2 mm AlGaAs/GaAs HEMT chip transistor manufactured by TriQuint®. Measurement-based modeling procedures and verification assessment will be given. The large-signal model work is based on the previous research outcome obtained at the HFT department (now renamed as Microwave Electronics Lab). The description includes both small- and large-signal model parameter extraction including self-heating and trapping effects.

In Chapter 5, a demonstrator of one class-AB power amplifier operating at 2.14 GHz center frequency using AlGaAs/GaAs HEMT device (chip model developed in Chapter 4) will be built up stepwise following the proposed partitioning design concept. Design procedure will be illustrated and explained accompanying with results from each intermediate step. The distinctive advantages for RF power amplifier design following this partitioning approach will be clearly demonstrated at the end.

Finally, key research conclusions are drawn and future works will be pointed out in Chapter 6.

Chapter 2

Investigation of Planar-Interconnection

Planar-interconnection becomes a pre-requisite in the partitioning design approach, and it strongly influences the success of the whole design concept. In general, it includes two main aspects, integrating the chip transistor to the ambient environment and interconnecting the individually designed and fabricated sub-parts. In the former aspect, parasitic effects and reliability issues resulted from die attaching, strongly determine the final entire circuit performance, when hybrid technology is implemented [21-22]. In the latter case, quality, practical reproducibility, and feasibility of the adopted interconnection methods manifest themselves as a pivotal aspect in this approach as well [23]. Therefore, interconnection techniques to be implemented must be well analysed and mastered. To this end, influence of active device interconnection consisting of die attachment and chip wire bonding will be discussed in section 2.1 in great details. Comprehensive experimental investigation of diverse microstrip-to-microstrip interconnection techniques, such like soldering, multi-wire bonding, copper ribbon, and silver-painting will be conducted in section 2.2. Finally, optimum interconnection technique will be selected on the basis of the experiment outcomes.

2.1 Active Chip Device Interconnection

When manufacturing power amplifier circuit using hybrid technology, the bare active transistor chip normally has to be first attached onto a certain carrier and then be connected to the peripheral transmission lines. A package-like environment is then constructed for easy handling and measurement. But such procedures will definitely cause performance degradation on the package level compared with bare die [24]. The best package is thus no package because of the unavoidable additional parasitic effects introduced, but it is not practical [25]. Hence, in practice manifold efforts are contributed to minimize the associated packaging effects [26-27]. Wire bonding is one of the common methods used owing to its lost-cost, relatively high feasibility, and reliability [28-30]. Thus, it will be adopted to make connection from transistor chip pad to the peripheral transmission line, which is in the form of microstrip line in this research work. In the following two sub-sections 2.1.1 and 2.1.2, issues concerning die attaching and chip bonding will be discussed, respectively.

2.1.1 Die Attach

Very different from monolithic technology, where active device is inherently grown on the semiconductor substrate thus eliminating the mounting parasitic effects [31], the transistor chip has to be additionally mounted onto a carrier with great care in the hybrid case [21, 32-33]. Based on the practical experience obtained, special attention should be paid when using electrically conductive epoxy, which is although a common material applied for die attaching for low to medium power at RF/microwave applications [34]. It has the advantages such like easy to apply, low-volume resistivity (0.1 to 0.3 mΩ-cm) as well as good shelf life (at least six months). However, low parasitic and reliable bond made by epoxy glue depends on various factors in practice. One must strictly follow the technical instruction delivered by the foundry. Two-component epoxy has a longer shelf time and does not need refrigeration like one-component epoxy does. However, it has to be pointed out that mixing procedure is very critical when using this kind of filled systems. Each content (resin and hardner) must be thoroughly stirred before they are mixed together. Otherwise, there will be

substantial quantities of silver or gold powder that is not mixed together throughout the paste. Based on the experience during this research work, this will consequently causes high resistance (in the order of hundreds ohms) in some areas (where there is a low concentration of silver or gold powder) and areas of low resistance (in the order of several milliohm) in the areas (where there is high concentration of powder) in others. A high degree of consistency throughout the whole area can be accomplished only if each individual part is mixed thoroughly prior to mixing them together. Mixing ratio by weight (1:1) should be followed as well [22].

Moreover, following aspects have to be carefully considered when performing the die attach.

1. *Selection of carrier plate*

   One should be careful, when selecting the carrier plate for holding transistors, especially when using epoxy for mounting chip transistor. No real bond and random resistance value will be resulted on the surfaces if aluminium is chosen as the plate material (see Figure 2.1). It will cause a very bad ground connection for the transistor (for instance bad source grounding for FET transistor). The reason behind is, there are always passivation and growing oxidation layers on the aluminium [35]. The oxide layer is electrically non-conductive, and what is even worse, it has a very poor adhesion to the metal itself.

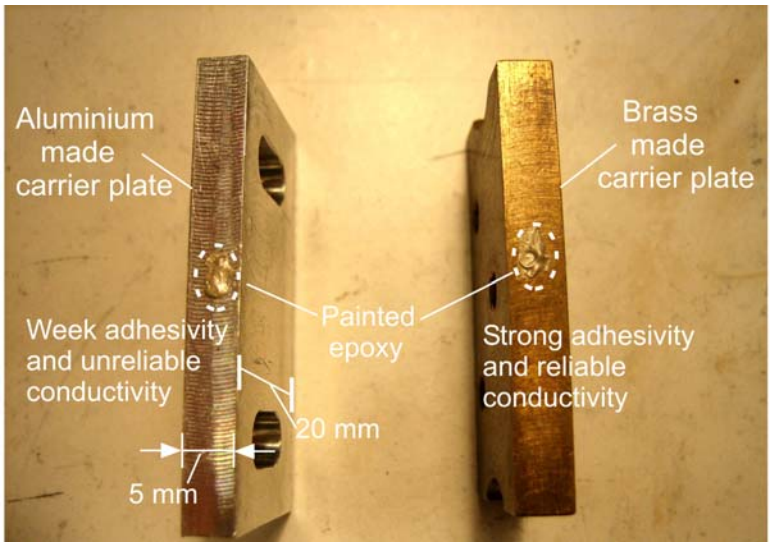


Figure 2.1 Epoxy painted on the aluminium and brass made carrier plate.

Another chemical problem is that the oxide tends to passivate the silver sheets on the top layer close to the metal-oxide. Thus, one will have a randomly dropped conductivity and long-term reliability problem [35]. This has been confirmed by the experiments done, in which significant change of conductivity of the bond using silver epoxy on aluminium plate, and very high impedance (above hundreds ohms to nearly open) can be found at some dots. The kind of bond has been shown with very week adhesivity as well.

Therefore, it is highly recommended to use brass instead of aluminium to construct the carrier plate to avoid facing any electrical and mechanical reliability problems, with providing an excellent ground (less than one ohm parasitic resistance) and strong adhesivity (see Figure 2.1) [22, 25 and 35].

2. Attaching

First, the attachment surface should be clean and flat. Second, epoxy should be distributed in a desirable pattern and amount on the bond location. The thickness of the epoxy should be kept at 0.001'' (25.4 μm) or less, since thick epoxy will have a less shear bond strength [22]. And then, a toothpick can be used to attach the chip on the epoxy. The chip is then carefully placed on the top of the epoxy dot and finally pressed into place (see Figure 2.2). The vertical black strip in the center of Figure 2.2 is due to the shadow of the brass bar, with a higher height (a cross-section view of the carrier plate is given in Figure 5.2). Care should be taken not to press too hard, because the epoxy may flow out and results in short circuit on the surface of the chip component. A gentle pressing is sufficient [22].

Another point is, the quality and performance of the epoxy should be checked prior using it for attaching die. This can be simply done by painting well-mixed epoxy on the metal plate, as shown in Figure 2.1. Thus, its electrical conductivity can be checked easily using a multi-meter. It has been found that the relative old epoxy (near to its expiration date) will show degraded and non-reliable performance. Thus, it is recommended to take fresh epoxy if available.

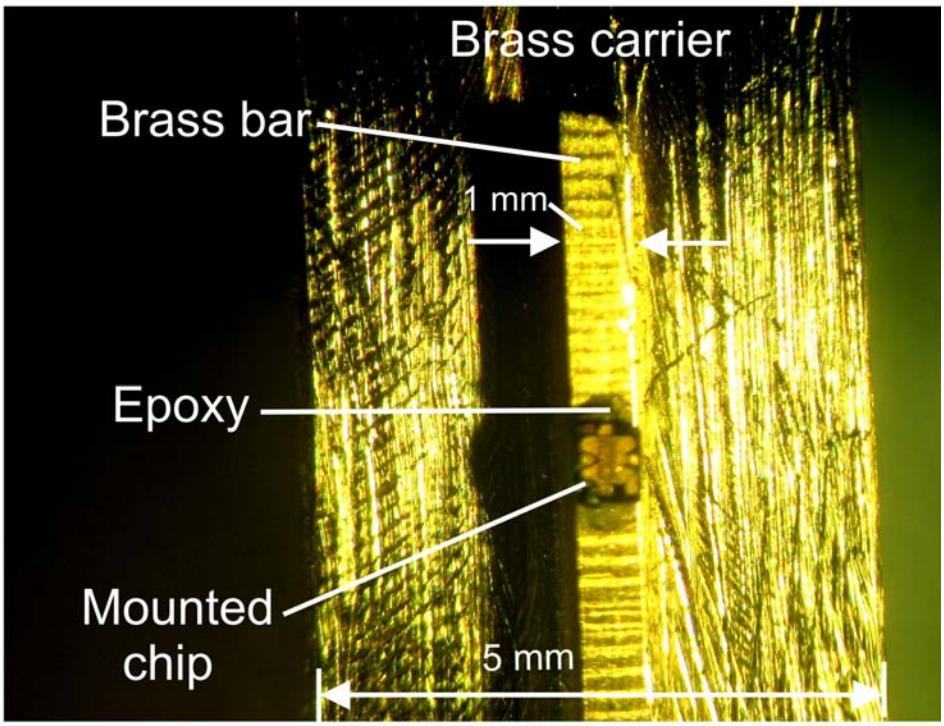


Figure 2.2 Transistor chip mounted on the brass-made plate using epoxy.

3. Cure

Proper temperature and time has to be set for curing the attached die in the oven strictly following manufacture's recommendation. However, one should be sure that the oven used is clean and has good airflow. The epoxy will not cure well if there are other solvent fumes in the atmosphere [36]. The specification concerning the operation temperature ranges of the epoxy should also be taken into account for high power amplifier applications, in which high temperature can arise beneath the channel thus affecting the surface of the bonding quality thermally [34].

The above-mentioned points have been thoroughly studied by own hands-on experiments. It seems that excellent die attaching needs experience and training, when one deals with epoxy. Epoxy bond electrical equivalent circuit can be expressed using resistor in series with inductor. It has also been found that the parameters of the parasitic effects are closely related with the quality of the epoxy material of the carrier plate and the mounting conditions, when used for transistor die attach [37]. The parameter extraction procedure thus should be carried out in the final specific circuit environment, where transistor chip is

already mounted [38]. Optimization can then be adopted to extract the final parameters, whose typical values have been found by experiments to be between 1Ω and 5Ω for resistive part and from 0.2 nH to 1 nH for inductive part, depending on the mounting conditions. The extraction procedure will be given in Chapter 5.

2.1.2 Wire Bonding Pad-to-Microstrip

Wire bonding is the most common technique adopted for connecting semiconductor chips in hybrid microwave integrated circuits (MICs) due to the numerous advantages mentioned above [39]. In this work, after the transistor chip being mounted on the carrier plate, it is then connected outside with a microstrip line at both gate and drain side, as shown in Figure 2.3. The source is already connected with the backside metal layer by internal vias for the chip used in this work [37] (see Chapter 4).

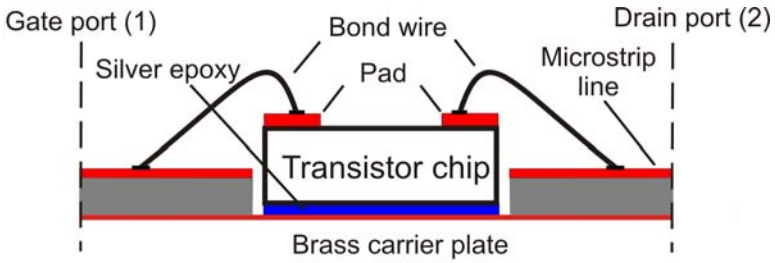
The bond wire normally has a small diameter from 0.5 mil to 1.0 mil (or 12.7 to 25.4 μm) made of gold or aluminium commonly. In most cases, bond wires are electrically short compared to the operating wavelength and can therefore be expressed as an inductance with a finite series resistance [40-41].

These are analytical equations reported, approximately expressing the inductance and resistance values in terms of the bond wire diameter, length, and material,

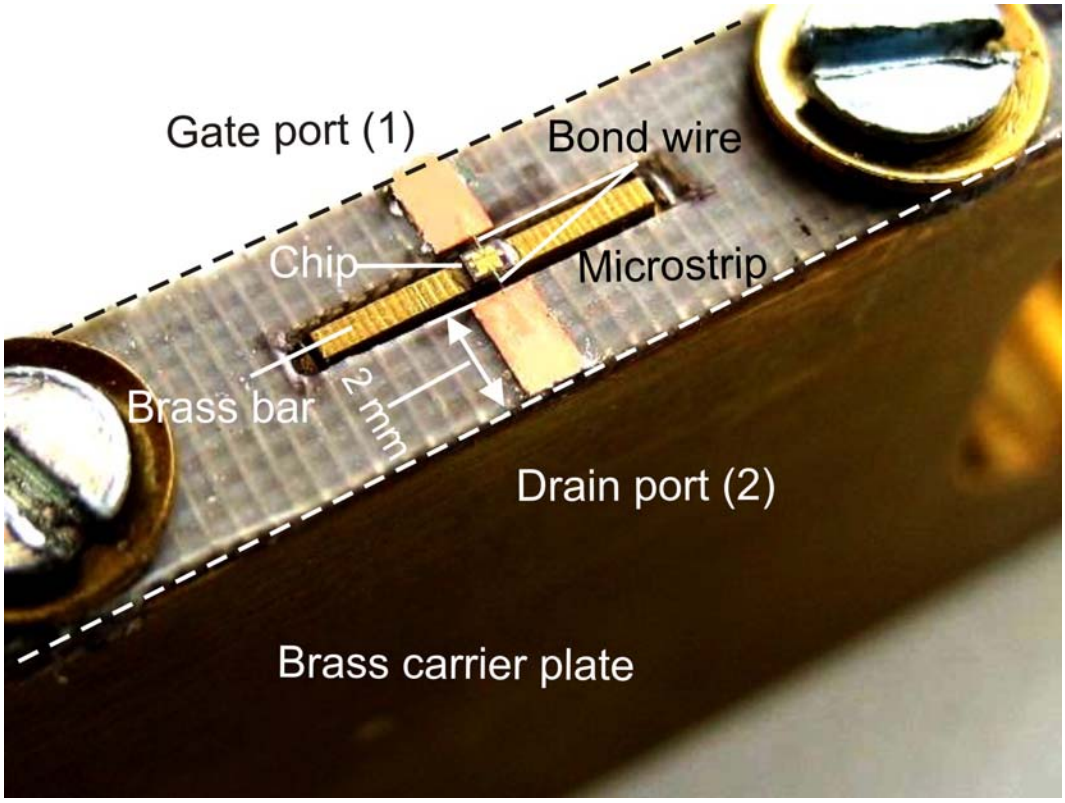
$$R = (4\ell / \pi\sigma d^2) \times [0.25d / \delta + 0.2654] \tag{2.1}$$

$$L = (\mu_0 \ell / 2\pi) \times [\ln(4\ell / d) + \mu_r \delta - 1] \tag{2.2}$$

where ℓ is the bond wire length, d is the diameter, μ_0 is the permeability of free space, μ_r is the relative permeability of the bond wire material, σ is the conductivity and δ is the skin depth. It can model the parasitic effects with a satisfied accuracy in the low microwave frequency range. Besides that, many EM field based numerical methods (such as FD, FDTD, MoM, and FEM) are reported to model the parasitic effects in a wider frequency range and with better accuracy [28, 42-47].



(a)



(b)

Figure 2.3 Mounted transistor chip device with gate and drain bond wire connections: (a) sketch, and (b) photograph**.**

In these simulation procedures, the geometry, dimensions and the bonding positions should be illustrated as exactly as possible to improve the accuracy, whereas it means a larger consumption of the computer resource and longer running time. One can also characterize the wire bonding connection experimentally [48-51]. Equivalent circuit of the connection can thus be developed based on the measurement data. Normally, S-parameters measurement should be precisely performed at the reference planes, where bonding connections are exactly made. To this end, in-fixture calibration method

is needed to shift the actual coaxial calibration plane to the reference planes needed (see Appendix A). These specific in-fixture measurement issues will be discussed in more details in next sub-section where microstrip-to-microstrip interconnection will be investigated.

In this work, the idea for extracting the parasitic effects of the bonding wire, connecting chip pads to the microstrip lines, can be explained according to Figure 2.4, in which the equivalent circuit of the bond wire block is illustrated. In order to extract the bond wire model parameters, two-port S-parameter measurement with the reference plane 1 and 2 will be performed including the bonded chip mounted on the carrier. It can be seen, the micro-package of the device consists of a short piece of microstrip line at the input and output side, gate bond wire, drain bond wire and the transistor chip itself. Furthermore, the epoxy mounting effects must be taken into consideration. First, the chip model for the transistor will be developed (in Chapter 4) based on on-wafer measurement data. Then, the real dimensions of bond wires will be measured and they are used to roughly estimate the parasitic parameters based on the analytical formula in (2.1) and (2.2). After that, the actual external parasitic elements (both bonding and mounting) in the equivalent circuits will be finally determined by optimisation procedures, with the goal of achieving minimum error between measured and simulated S-parameters [38, 49]. This approach has the advantage that it considers the true real mounting and bonding situations, which may differ from one batch to another.

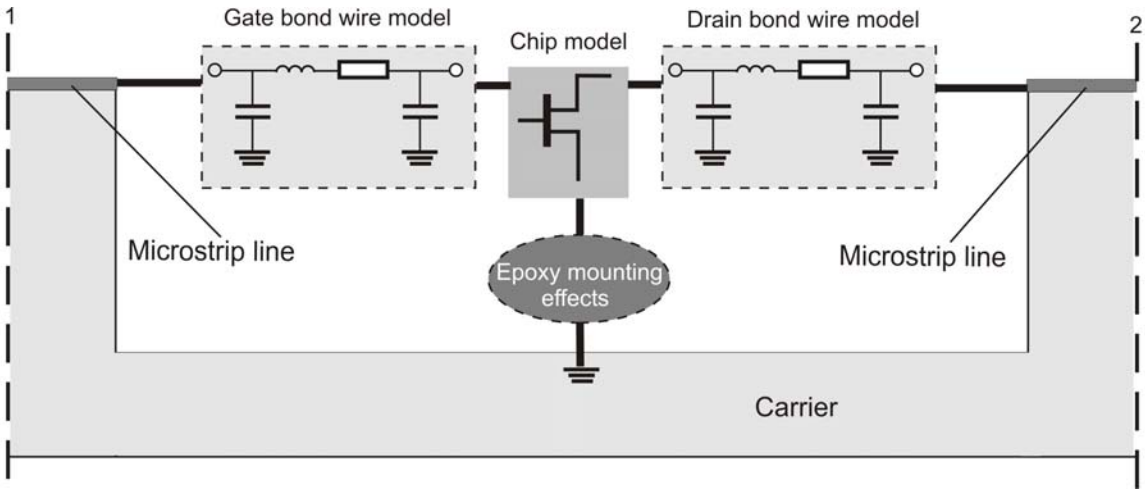


Figure 2.4 Schematic of the bond wire connection of mounted chip to its peripheral microstrip lines.

The final entire parasitic effects interacting with the active transistor chip, thus, can be well estimated and considered in this way. The detailed procedure will be shown in Chapter 5, when the micro-packaged device is discussed.

Also, there are other considerations in practice regarding the chip wire bonding procedure. First, the selection of the bonding wire material should be carefully done based on the metallurgical consideration of the bonding pads material. For instance, aluminium bond wire is not recommended to bond on copper, because a brittle intermetallic compound will be formed, which lowers the overall shear strength of the bond [22]. Also, bonding parameters such like force, time and power have to be set correctly to achieve reliable bonding without damaging the fragile chip. Besides that, the current handling capability of the bonding wire has to be checked, and at least around 30% safety should be kept when comparing the bonding wire fusing current with the maximum transistor operating current [32, 52]. In this work, the maximum output current of the chip is approximately 300 mA (referred to Chapter 4). Thus, a gold bond wire with 25 μm diameter (current handling capability of 600 mA) is used for making the bonding. The experience obtained in this work shows that the relative positioning of the chip and the microstrip lines are critical, because it determines the minimum bonding wire that can be realized in practice. The lengths of the bond wire made were in the range of 0.5 – 0.8 mm. Also, it is very important to check whether the bonding made is a true and reliable one, since especially unstable gate bonding may damage the FET device under active drain bias conditions. They are first checked visually under the microscope, and a very thin wooden stick is used to test the strength of the wire bonding. Also, a set of DC test is performed to further test the wire bonding, as listed below:

1. *Drain bond wire test*

   Device is biased at deep class-AB. A small positive drain voltage (approximately 1V) is applied. A drain current of several miliamperes should be measured. Then the current is slightly increased with the increment of drain bias voltage (2-3 volts), when the wire bonding is correctly done at the drain side.

Another simple method is to use a multimeter. A resistance of several ohms (for the GaAs HEMT used in this work, approximately 2 ohm) should be measured between drain and source terminal, when no voltage is applied at the gate side. This resistance is the series bulk resistance of R_d and R_s, as the channel is totally open, when V_{GS} = 0V.

2. *Gate bond wire test*

   This can be done by changing the gate voltage slightly, when the drain side is biased at a low voltage (up to 2V) for safety reason. With the change of the gate voltage, the current should also change correspondingly, which indicates a good connection of the gate wire bonding.

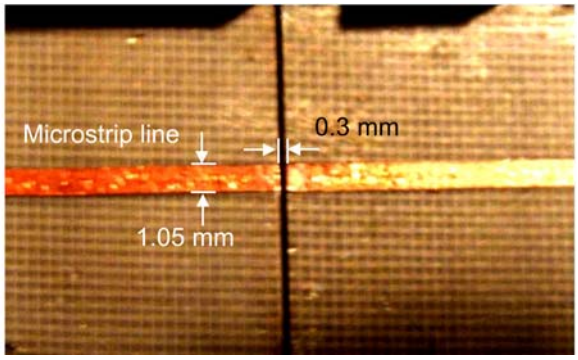
2.2 Microstrip-to-Microstrip Interconnection

In this part, the connection of the individual sub-parts will be treated. Mainly the practical performance of several microstrip-to-microstrip interconnection techniques will be investigated by measurement. Advantages and disadvantages of each method in this specific application will be discussed in details. A final optimum technique will be decided on the basis of the comprehensive practical performance comparison among them [53].

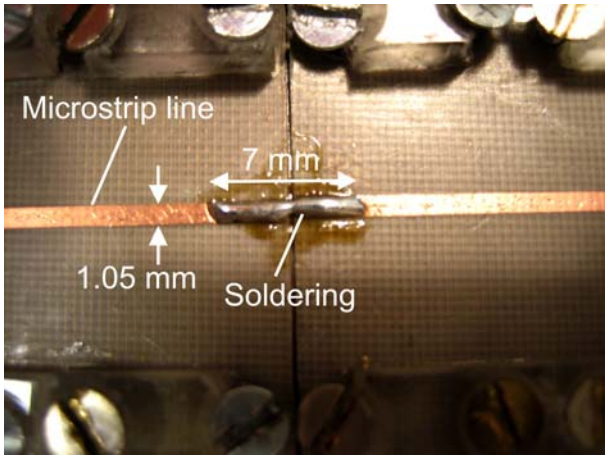
2.2.1 Soldering

Soldering is commonly used to mount SMD components on a PCB (**P**rinted **C**ircuit **B**oard) or in hybrid MICs [22, 54-55]. In principle, it could also be used for connecting microstrip lines in this application. However, it can easily happen in practice that the solder does not flow evenly, when one tries to connect two pieces of microstrip line. This results in a relative long soldering line, in the order of several millimeters, as can be seen in Figure 2.5.

What is even worse, solder can flow into the gap between the two microstrip lines (see Figure 2.5(a)), resulting a short connection to ground.



(a)



(b)

Figure 2.5 Microstrip-to-microstrip interconnection: (a) before soldering, and (b) after soldering.

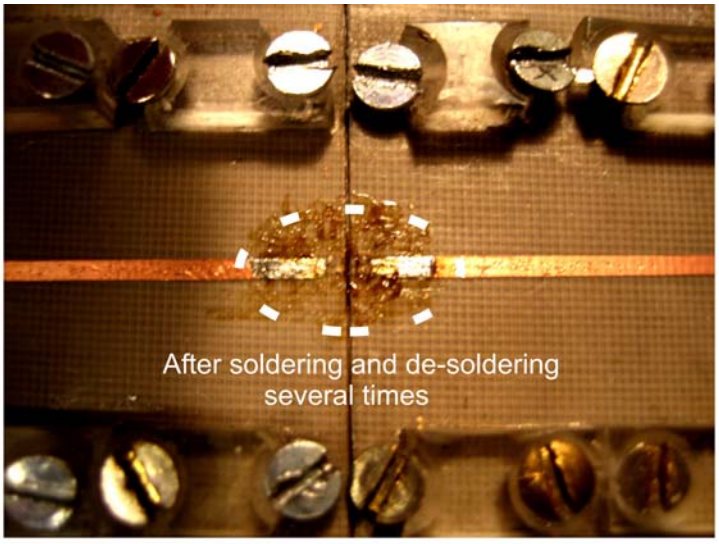


Figure 2.6 Photograph of the microstrip after several times soldering and desoldering.

It has also been found by experiments that the metal stripe of microstrip line can be removed by repeated heating, after several times of soldering and de-soldering processes (see Figure 2.6). However, in this partitioning design approach, one has to use the calibrated fixtures to measure each sub-circuit, which means the microstrip-to-microstrip line interconnection has to be performed several times. Hence, after observing such appearances, it has been decided not to consider the soldering technique any longer for this specific application.

2.2.2 Multi-Wire Bonding

Multi-wire bonding is normally used to lower the parasitic effects, because it has a lower effective inductance compared with the single bond wire, due to a number of parallel bond wire connections (see Figure 2.7). The power handling capability is also increased. Figure 2.8 shows the S-parameter comparison of the single bond wire (approximate length 750 μm) and three bond wires (average length 760 μm) interconnection. It can be seen that the interconnection performance is improved by increasing the number of bonding wires (lower reflection coefficient and higher transmission coefficient).

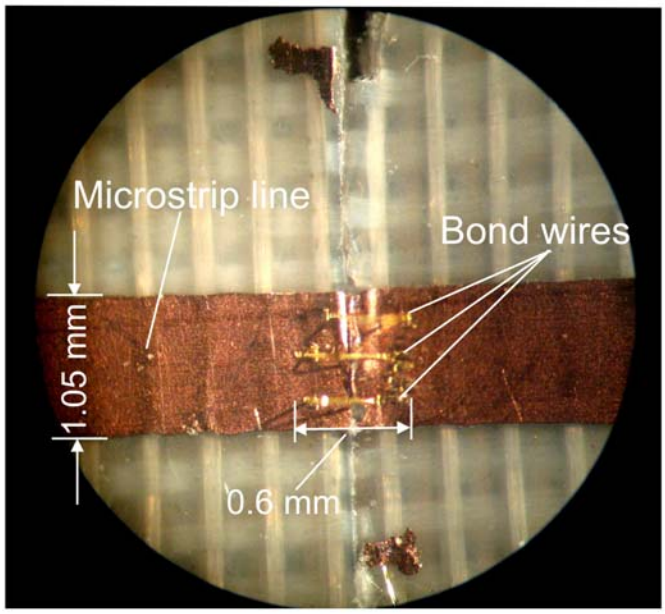


Figure 2.7 Multi-wire bonding for microstrip-to-microstrip interconnection.

However, it is notorious to precisely model the multi-wire bonding effects, because the coupling effects are strongly depending on the wire length, geometry, bonding angle, and positions, and also the separation distance and angles between the wires. So many sophisticated factors make the precise prediction of the multi-wire bonding connection in the simulation complicated [56-61].

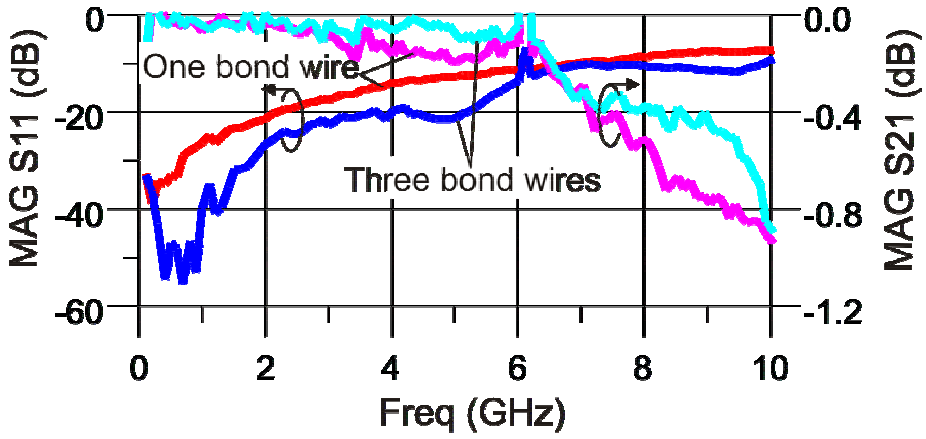


Figure 2.8 S-parameter measurement results of one bond wire (approximate length 750 μm) and three bond wires (average length 760 μm) made interconnection.

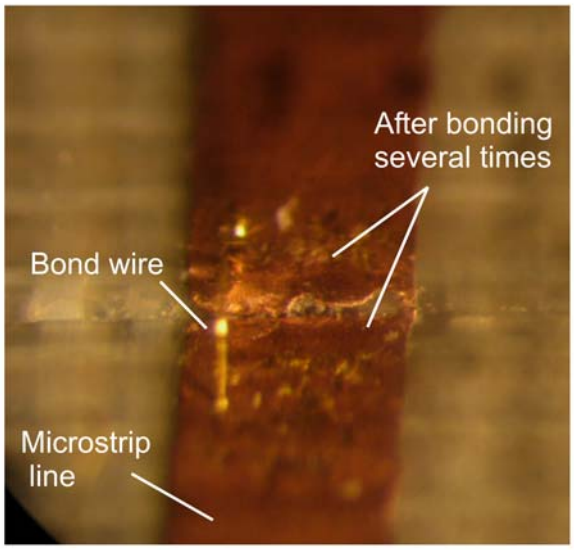


Figure 2.9 Photograph of the microstrip line after being bonded several times.

The high reproducibility of multi-wire bonding is also a great challenge. As proved by experiments, it is very hard to make repeatable reliable wire bonding

on the same copper surface (see Figure 2.9) after several times bonding on it, since the copper surface is damaged by the heating, bonding power and force from the previously made wire bonding. Thus, microstrip-to-microstrip interconnection using multi-wire bonding is not considered as an optimum solution in practice.

2.2.3 Copper Ribbon

As shown in Figure 2.10, a piece of hand made copper ribbon can also be adopted for making the interconnection between microstrip lines [62-64]. It has a much higher current handling capability compared to wire bonding. The challenge in this technique is from the copper ribbon placement. In this configuration shown, a plate is needed to press the copper ribbon tightly on the microstrip line surface. The shape of the plate is designed to minimize the overlap area with the circuit as shown in Figure 2.10(b).

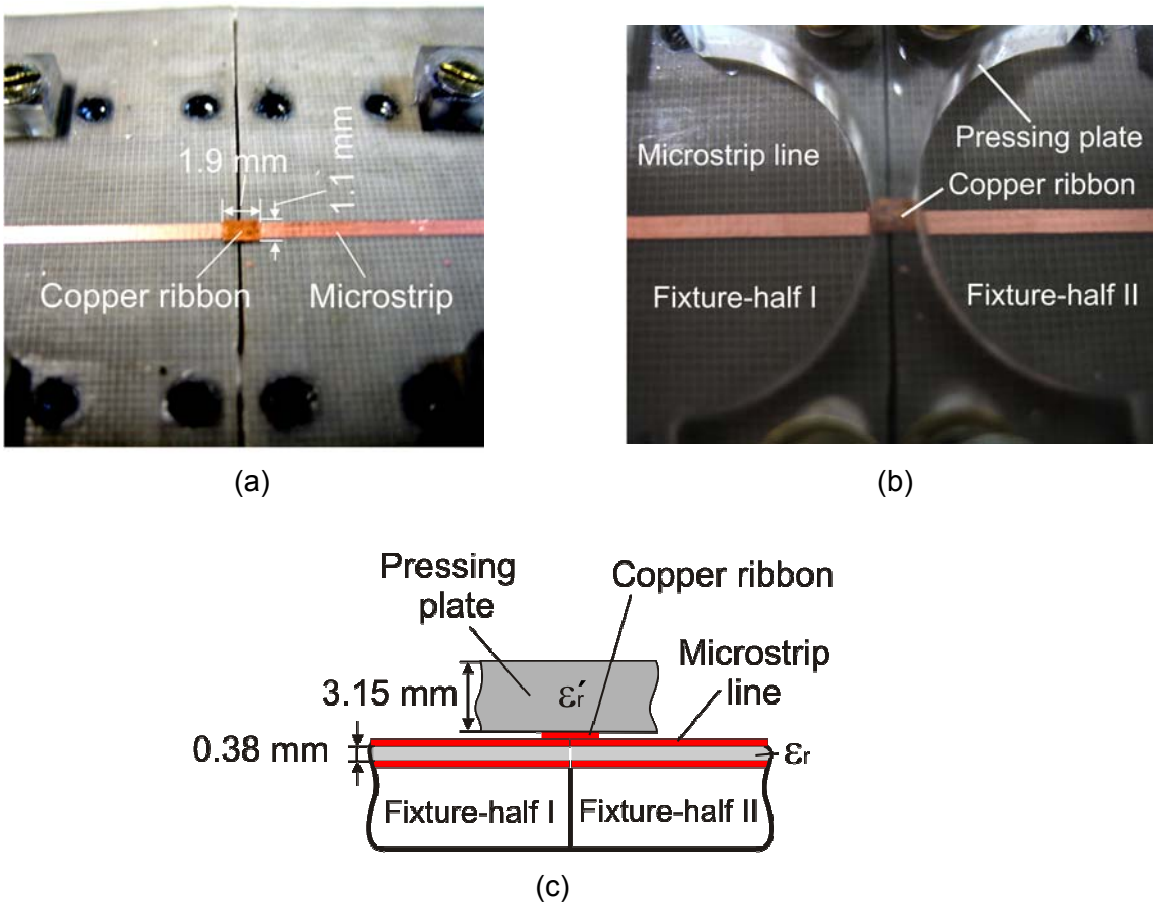


Figure 2.10 Copper ribbon for microstrip-to-microstip interconnection: (a) before covered, (b) after covered by pressing plate, and (c) side view.

The relative permittivity of the pressing plate (made of plexiglass, within the range of 2.6 to 3.5) is approximately three times that of air ($\varepsilon_r = 1$) [65]. Because of the difference of the permittivity from air and plexiglass, an impedance discontinuity is expected at the interconnection position resulting in degraded power transmission [64], with the increment of frequency. The amount of pressure on the copper ribbon changes the transmission coefficient as observed during the experiments. The stable fixing needs good handling.

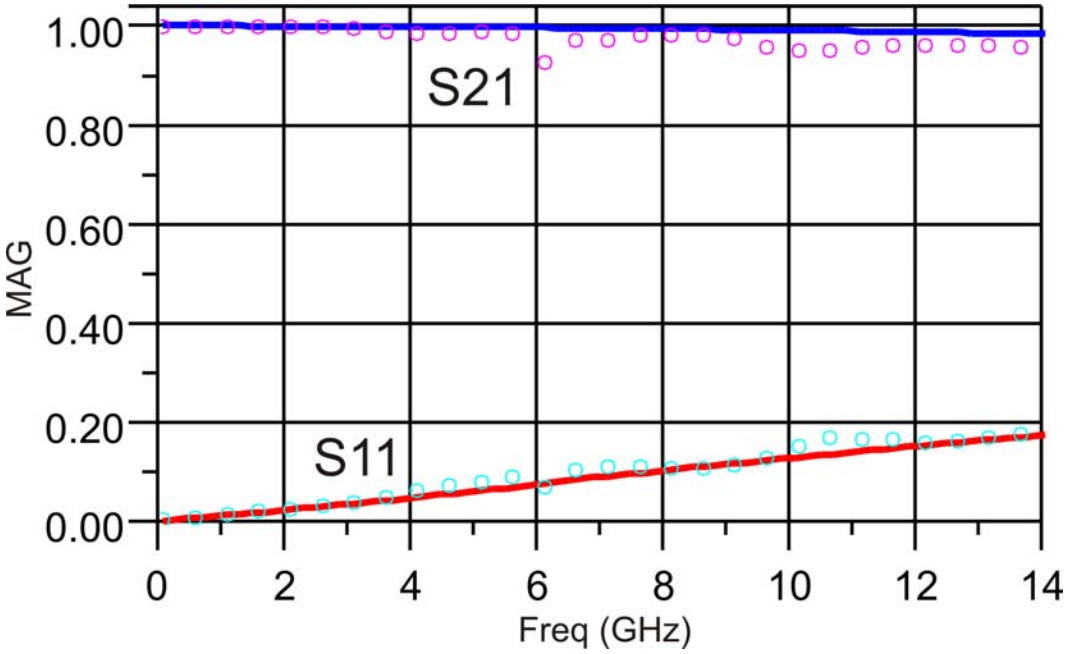


Figure 2.11 Measured (symbols) and simulated (solid lines) S-parameters of the copper ribbon made microstrip-to-microstrip interconnection.

The S-parameter measurement result of the microstrip-to-microstrip interconnection made by copper ribbon is compared with the momentum simulation in Figure 2.11. Good agreements are achieved in the frequency range up to 14 GHz. In principle, it has good performance with S11 less than 0.1 (approximately –20 dB) and S21 within 0.988 (approximately –0.1 dB) up to 5 GHz. It will be compared with the silver-paint made interconnection in next sub-section. Also, the difference of the characteristic impedances between the short piece of the pressed copper ribbon and the 50Ω microstrip line can be roughly estimated using the measured reflection coefficient. It has been found that there is approximately 10Ω difference at 6 GHz.

2.2.4 Silver-Painting

The adoption of silver-painting to make the interconnection between two pieces of microstrip lines is reported in [66]. It has been considered as an excellent candidate for making such connection owing to its high reproducibility and excellent conductivity [67-69]. Thus, it has been investigated extensively by hands-on practice in this work. Collected experience is reported in the following.

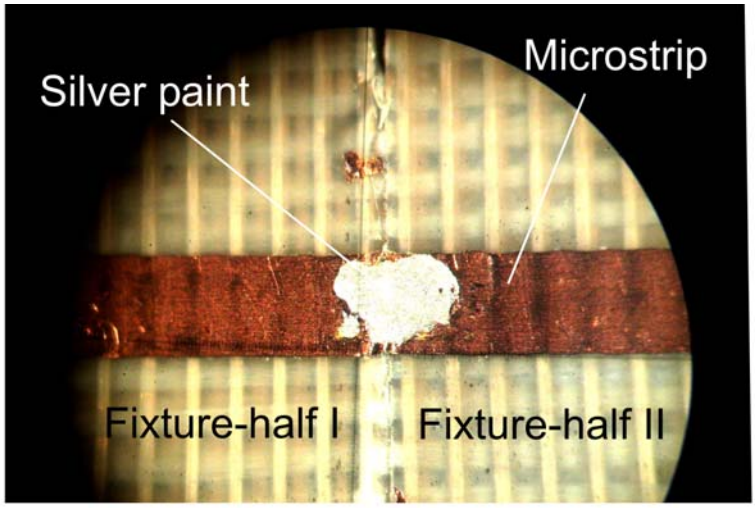


Figure 2.12 Silver-painting made microstrip-to-microstrip interconnection.

First, one should carefully drop the silver onto the microstrip line connection position using a microscope. Second, the concentration of the silver-paint mixture is a key factor in the utilization. If the concentration is too low, the thin silver-paint mixture will easily flow into the gap between the two sub-parts resulting in a short connection. Also, it may flow out the metal trace of the line, which alters the characteristic impedance. It has been found that one can pick up a drop of silver-painting using a wooden toothpick. Then one should wait for approximately 30 seconds for letting the diluter liquid, contained in the silver paint, vaporize. Thereafter, a proper concentration of the silver paint will be obtained. Then, one can coat the connection position slowly using the silver-paint mixture with a sharp toothpick, drop by drop. Importantly, sufficient time should be given for silver paint to get dry. Normally it takes around 30 minutes at room temperature for adequate drying; otherwise degraded interconnection performance will be observed. By following this instruction, reliable silver-painting connection can be done. Figure 2.12 shows the silver-paint made microstrip-to-microstrip interconnection under microscope. Then, the connection

is disconnected to check whether silver-paint liquid has flown into the gap between the two fixture-halves. As being observed under microscope (see Figure 2.13), no silver-paint has flown into the gap, when a proper concentration of the silver paint is controlled, as explained above. The applied silver-paint in this work is Leitsilber L204 from Ferro GmbH, and detailed information can be found in [70].

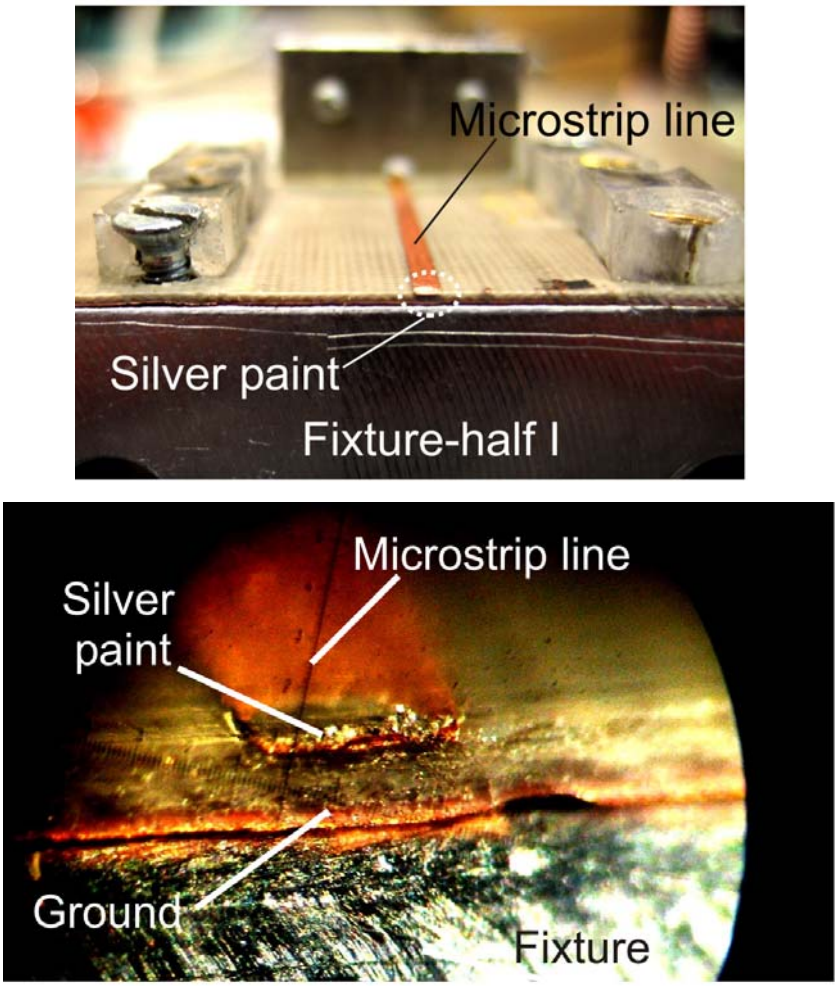


Figure 2.13 Cross-section of the fixture-half after being connected using silver-paint.

Applying the in-fixture calibration method, the real performance of the connection can thus be measured. Figure 2.14 shows four groups of S-parameter measurement of silver-paint interconnection up to 20 GHz. Excellent reproducibility is observed by the high overlapping of the measured four groups data. This method gives excellent interconnection quality, with S11 below –20 dB and S21 greater than –0.2 dB up to 10 GHz.

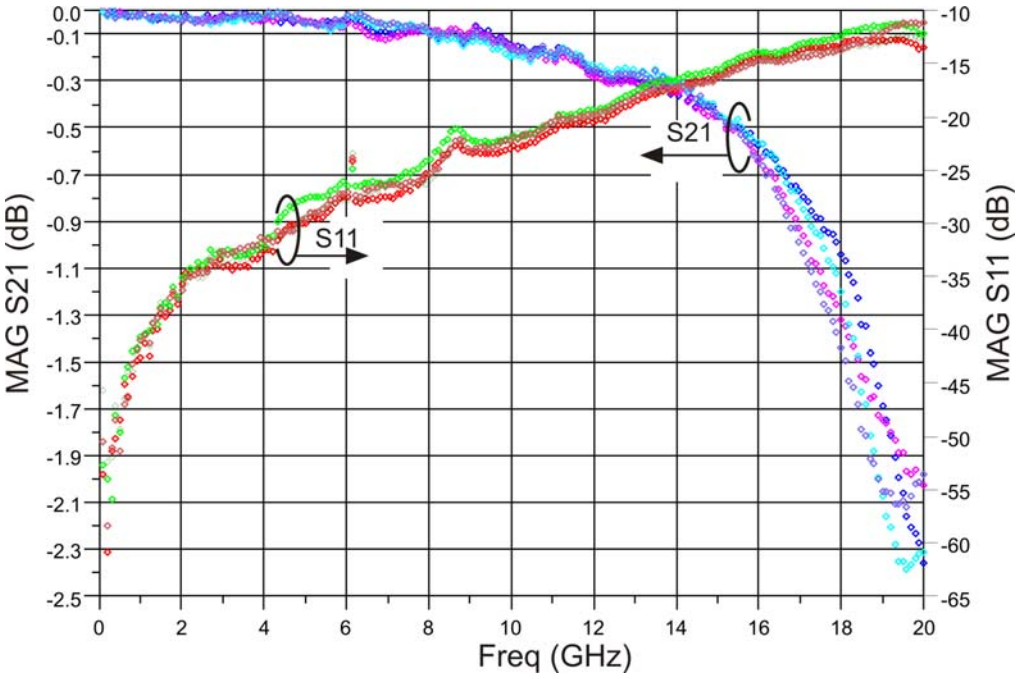
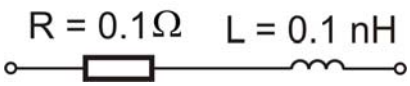


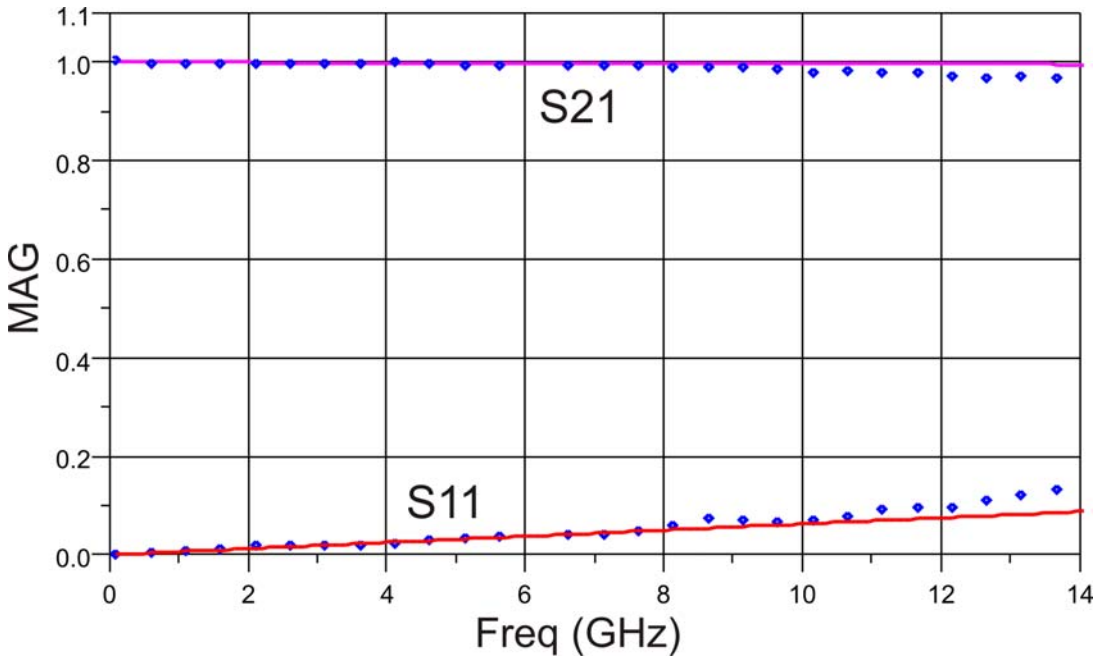
Figure 2.14 Four groups of S-parameter measurement of the silver-paint inter-connections of microstrip-to-microstrip.

The parasitic effects of silver-paint made interconnection have been equivalently modeled using a resistor and an inductor in series, as shown in Figure 2.15(a). The parameters have been extracted based on the in-fixture S-parameter measurement data. Final comparison is done between simulation result and the averaged measurement result. As seen from Figure 2.15(b), good fitting is achieved up to 8 GHz, which shows a sufficient accuracy for the application around 2 GHz.

In Figure 2.16, measured results of copper ribbon and silver-paint interconnection techniques are compared. Silver-painting connection shows less than –20 dB return loss and less than –0.2 dB insertion loss, which has a 10 dB lower return loss and 0.2 dB lower insertion loss in comparison with copper ribbon connection.



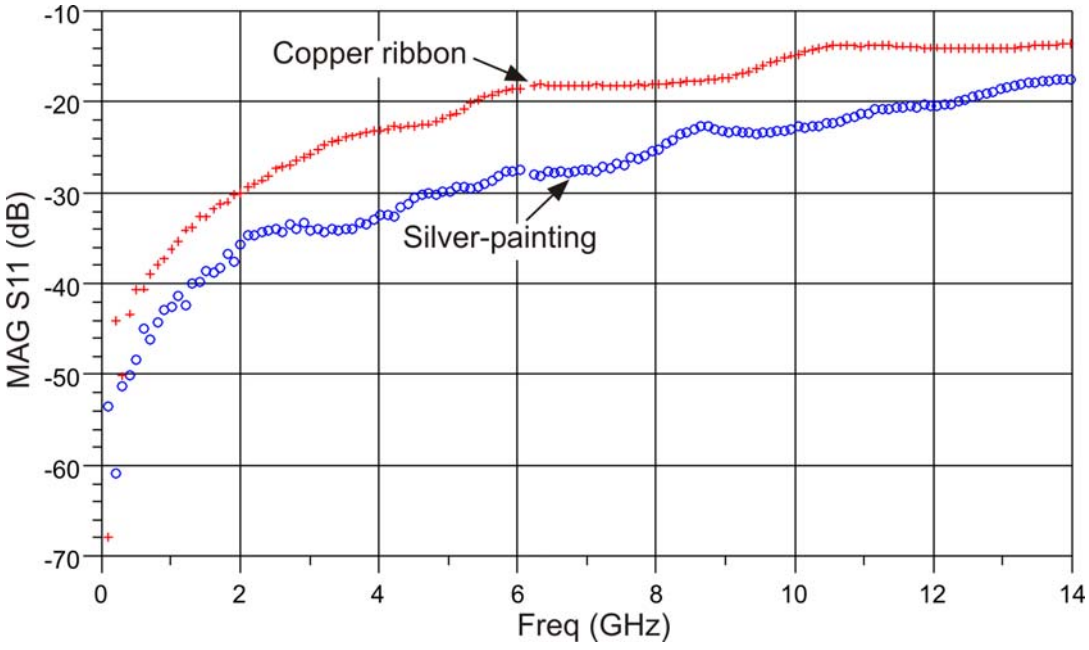
(a)



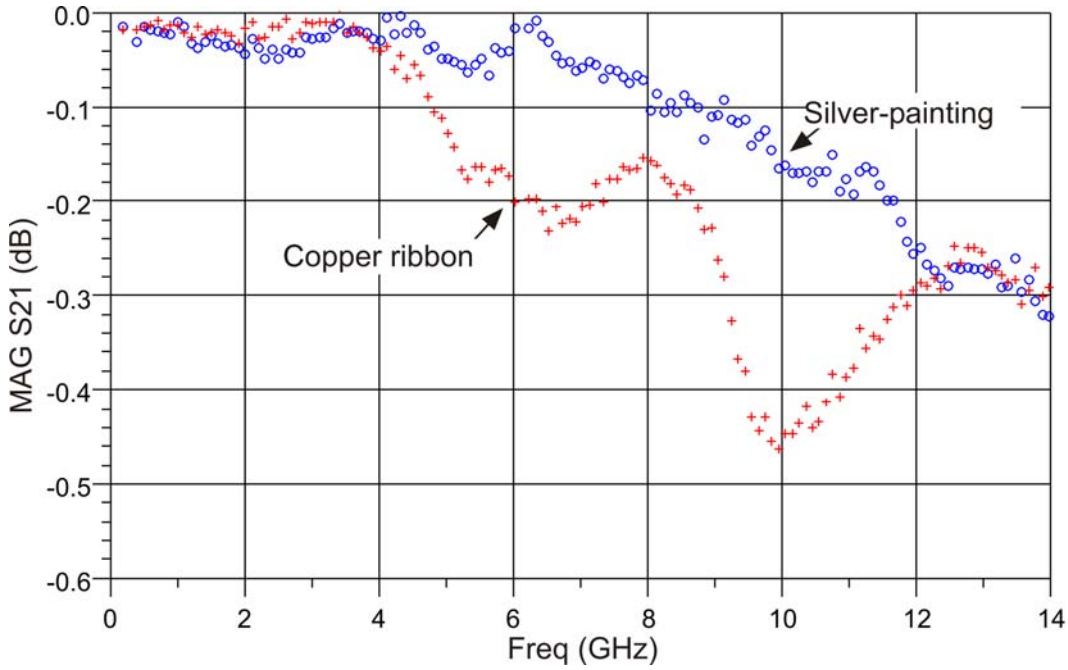
(b)

Figure 2.15 (a) Equivalent circuit of silver-paint interconnection, (b) comparison of the simulated (solid lines) and measured (symbols) S-parameter.

In a conclusion, all the investigated microstrip-to-microstrip interconnection methods are compared in Table 2.1, in terms of the practical reproducibility, power handling capability, transmission performance, mechanical stability, and operability [71].



(a)



(b)

Figure 2.16 Comparison of the measured copper ribbon and silver-painting made microstrip-to-microstrip performance: (a) magnitude of S11 and (b) magnitude of S21.

As can be seen from the table, silver-painting has the best performance for nearly all the criterias except its mechanical stability is lower than that of soldering. Hence, it has been chosen as the technique for making the microstrip-to-microstrip interconnection owing to its good performance and relative easy handling in practice.

Table 2.1 Comparison of different microstrip-to-microstrip interconnection techniques.

Interconnection technique	Reproducibility	Power handling capability	Transmission performance	Mechanical stability	Handmade ease
Soldering	Problematic (as discussed)	+ + +	+ +	+ + +	+
Multi-bond wire	–	+	+ + +	–	–
Copper ribbon	+ + +	+ + +	+ +	+ +	–
Silver-painting	+ + +	+ + +	+ + +	+ +	+

Chapter 3

Analysis and Modeling of Passive SMD Components

Passive components are crucial parts in the circuits for radio frequency applications [21]. It is well known that the passive elements are never function ideally in reality due to the associated parasitic effects [40]. Furthermore, care must be taken to the assembling of these passive components, since mounting effects will inevitably alter the true operating conditions [72-73]. Therefore, the ideal passive component models (ideal resistor, inductor, and capacitor) provided in the simulation software obviously cannot be adopted into the design procedure directly. Thus, for accurate and reliable circuit design, analysis, and modeling of these passive components become necessary. Although S-parameter measurement data or equivalent circuit of the passive component is available for certain components from the vendors, it is indeed essential to perform thorough analysis of the passive components in the real-world specific circuit level, to extract the reliable characteristics of each component when placed in the final hybrid environment [74]. Each passive component will be characterized and then compared with the simulation including mounting effect, which is an integral part of the real component in use. Consequently, later performance deviation on the circuit level is avoided.

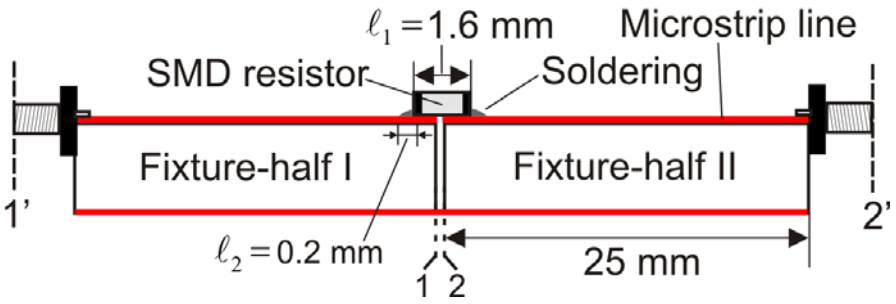
Surface mounted device is a common type of passive components used for RF hybrid MICs, because of the reduced component size and weight, good

frequency performance, and easy assembling [73]. To investigate the real practical performance of each component precisely, in-fixture measurement set-up is needed (refer to Appendix A). Finally, the equivalent circuit model will be extracted and verified by measurement [75]. Accordingly, the designer becomes confident about the performance of the utilized specific SMD components in the final circuit.

In sections 3.1-3.3, SMD types of resistor, capacitor, and inductor will be analyzed using the calibrated in-fixture measurement set up, respectively.

3.1 SMD Resistor

In RF/microwave circuits, resistors are normally used for attenuators, terminations and stabilization network design. They are available in both the coaxial and surface mounted forms [76-77].



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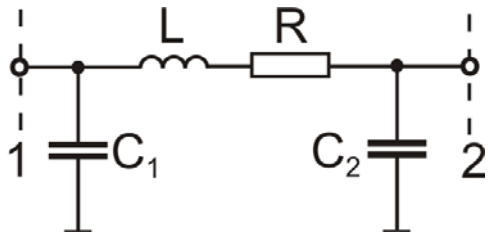


(b)

Figure 3.1 (a) SMD resistor measurement environment and (b) equivalent circuit topology [77].

Figure 3.1 shows the equivalent circuit of the surface mounted device, in which R describes the actual resistance, L represents the total parasitic series inductance, and C is the equivalent shunt capacitance resulting from mounting (mainly from the coupling to the ground plane of the boards) [77]. Since the size of the chip is much smaller than the operating frequency wavelength, it is proper to model the resistor as a lumped device to first-order approximation [40]. Normally, soldering is applied to fix the SMD component on microstrip metal strip. Soldering is a critical factor affecting the quality of integrating. Although it seems to be simple to perform soldering, there are versatile factors making decisive influence on the reliability of the soldering components in practice [54-55]. The experience has shown that, when the surface of the metal strip is not clean, bad adhesivity of the soldering will be formed. Also, it is recommended to polish the surface of the metal strip and to coat the surface with thin layer of tin before soldering the SMD component. This can increase the reliability of soldering. A temperature as low as possible should be kept while maintaining enough temperature to quickly solder a joint (approximately 2-3 seconds). Too much temperature will cause large flux of solder, which may flow out of the desired area and may cause short connection.

Within the partitioning design approach, the operator is able to evaluate the performance of the soldered SMD component on the circuit board by performing the in-fixture measurement, which gives a direct feedback concerning the soldering quality and reliability in a final application environment. As shown in Figure 3.1(a), the measurement will be done with respect to the coaxial reference planes 1' and 2'. Using in-fixture THLR calibration, the measured data can be transformed to the microstrip reference planes 1 and 2, thus, including the mounting and soldering influences in the device characterization.

Two SMD resistors (R_1 = 8Ω and R_2 = 10Ω) are chosen for designing the stabilization network, to ensure the unconditionally stable operation of the power amplifier (see Chapter 5, stabilization network design). These two chip resistors are produced in thin film technology with a low tolerance of 1%. Case size 0603 (valued dimension: 1.6 mm length and 0.8 mm width) is chosen because its width is compatible with the width of the used 50Ω microstrip line, which is 1.05 mm (h = 0.381 mm, ε_r = 2.54). The given relative permittivity of the microstrip

substrate has been determined using a ring resonator measurement approach (refer to Appendix B).

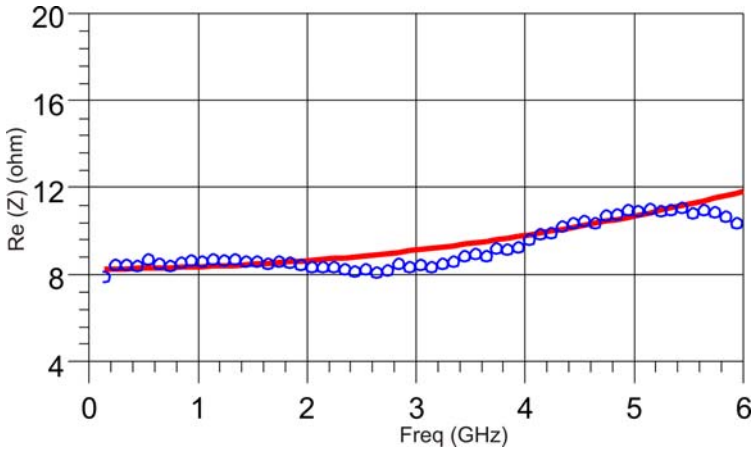
The resistor is mounted in the test-fixture as shown in Figure 3.1(a). S-parameter measurement is performed up to 6 GHz. S-parameters are then converted to Y-parameters, which are directly related to the equivalent circuit in Figure 3.1(b). Measurement results are plotted in Figure 3.2 in terms of real and imaginary impedance values, respectively. To model the real mounting situation, equivalent circuit (shown in Figure 3.2(c)) is implemented in ADS® simulation software, based on the circuit topology proposed in Figure 3.1(b). It can be noticed that the solder pad is included in the equivalent circuit, represented by the 0.2 mm microstrip line [77]. Then, parameters are extracted by optimization with the goal of achieving best fitting to the measurement data [78]. Similarly, the procedure is repeated also for 10 ohm SMD resistor. Excellent agreement is achieved between measurement and simulation for both resistors in the frequency range up to 6 GHz, which is sufficient for the power amplifier circuit to be designed around 2 GHz.

It can be concluded from Figures 3.2 and 3.3 that the real parts of the impedance values approximately equal the rated resistance values (8.25 ohm and 10.1 ohm). They are nearly frequency independent up to 3 GHz, and after that they are slightly increasing with frequency. However, non-ignorable inductive effects (in both cases, approximately 0.7 nH) should be included for modeling the parasitic effects, which mainly result from internal parasitic effects and soldering as well. A 0.01 pF capacitor is included at both sides to model the parasitic capacitances resulting from coupling effects to ground. Together with the 0.2 mm microstrip line for modeling the soldering pad connection, very good fitting for the reactive part is achieved for both mounted resistors. Thus, the derived device models (in Figure 3.2(c) and Figure 3.3(c)) will be adopted for the subsequent stabilization network design.

Table 3.1 summarizes the parameters of the equivalent circuits for both chip resistors.

Table 3.1 Parameters of the equivalent circuits for the two SMD chip resistors.

Resistor	R (Ω)	L (nH)	C_1 (pF)	C_2 (pF)
8 ohm	8.25	0.77	0.11	0.11
10 ohm	10.1	0.73	0.11	0.11



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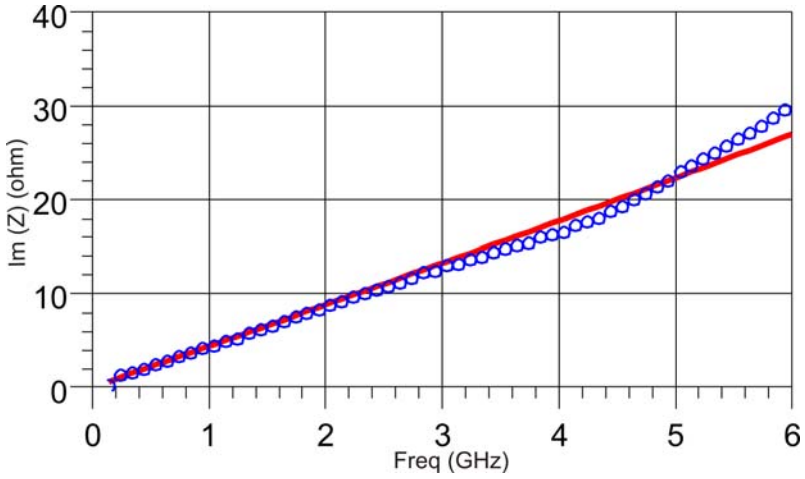

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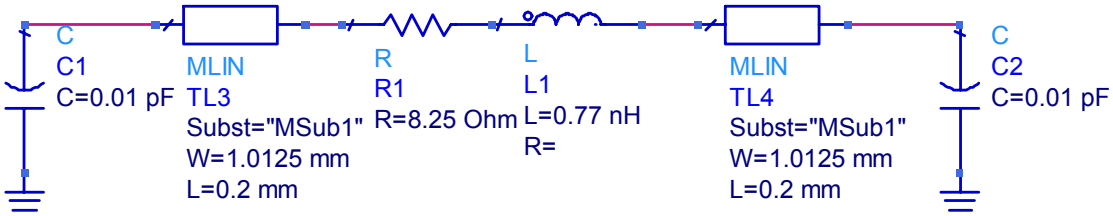
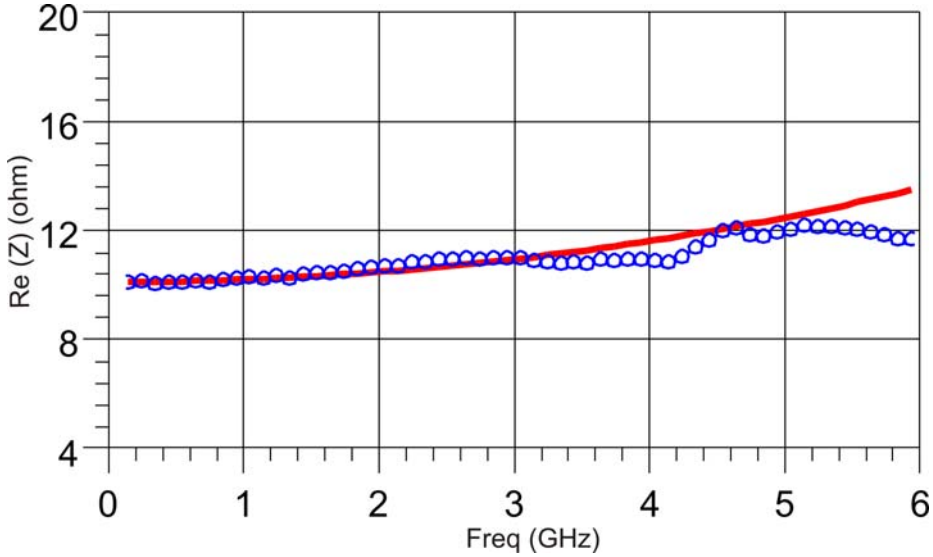
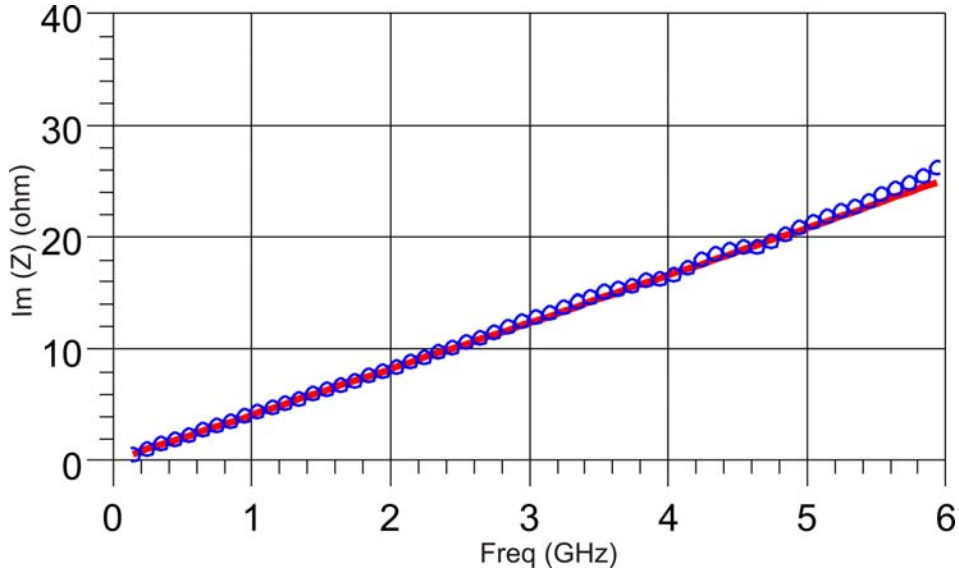


(c)

Figure 3.2 SMD 8.25Ω chip resistor simulation (solid lines) and measurement (symbols) comparison: (a) real part, (b) imaginary part and (c) its equivalent circuit.



(a)



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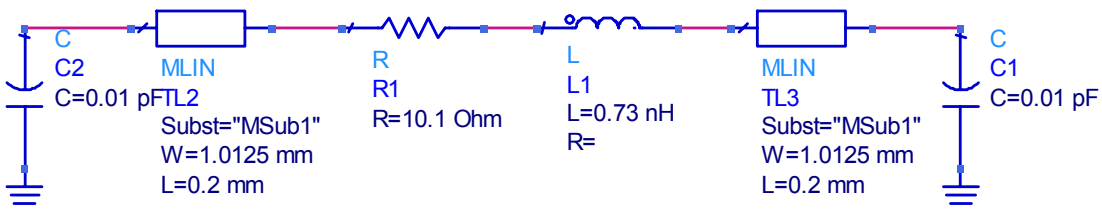


(c)

Figure 3.3 SMD 10Ω chip resistor simulation (solid lines) and measurement (symbols) comparison: (a) real part, (b) imaginary part and (c) equivalent circuit.

3.2 SMD Capacitor

DC blocking and decoupling purposes are major applications for capacitors used in RF circuits. For different application purposes, the selection criteria will also be different [79]. Capacitors used for blocking DC voltage should have minimum influence on the RF signal path. It means that capacitor should have extremely low impedance at the RF operating frequency, which is provided by choosing capacitor having the series resonant frequency around the RF operating frequency.

The equivalent circuit of a practical capacitor is presented in Figure 3.4. C_0 is the desired capacitance value. L_s and R_s represent the equivalent series inductance and the equivalent series resistance. C_p is the parasitic parallel capacitance associated with the parallel resonant frequency [80].

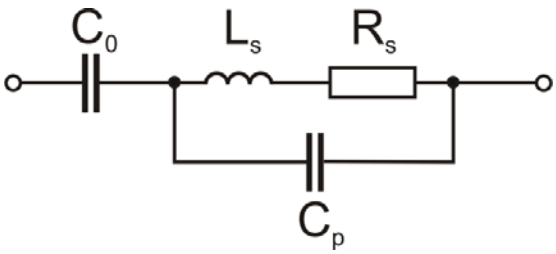
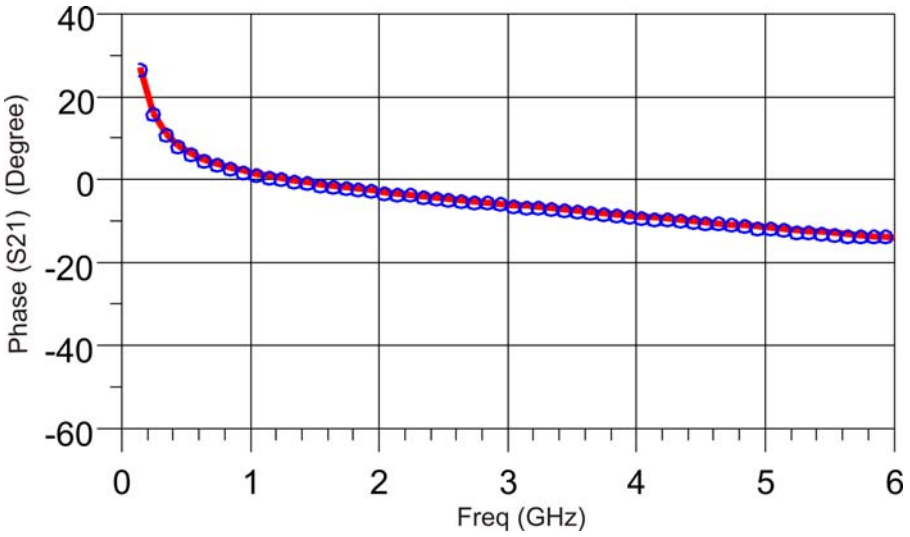
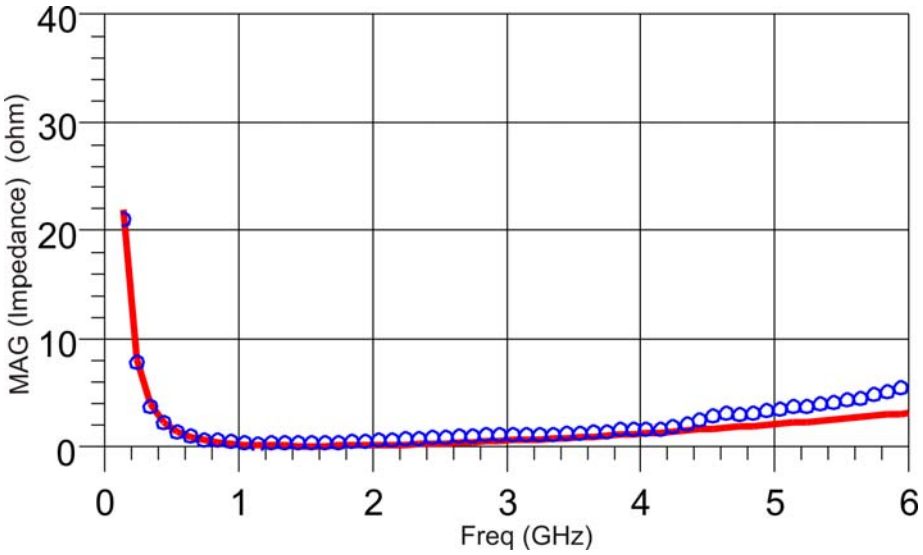


Figure 3.4 Equivalent circuit of a practical chip capacitor.



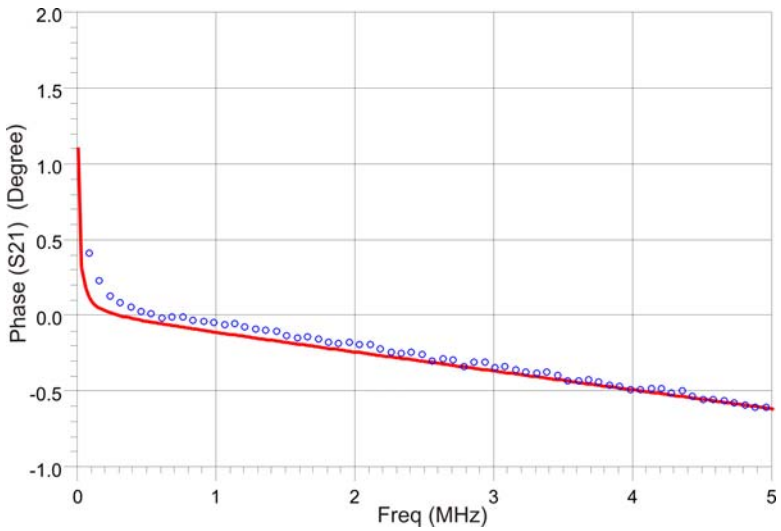
(a)



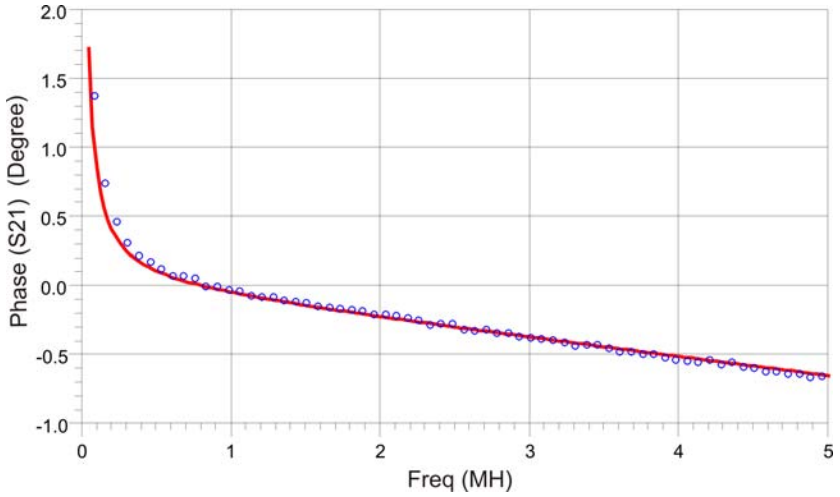
(b)

Figure 3.5 Simulation (solid lines) and measurement result (symbols) of a 22 pF chip capacitor used for DC blocking: (a) phase of S21 and (b) magnitude of the input impedance values.

As shown in Figure 3.5, the phase of S21 of the used chip capacitor based on in-fixture S-parameter measurement is given. It can be easily seen that the series resonance frequency is at the position, where S21 phase crosses zero. Correspondingly, minimum impedance is achieved around this frequency. Therefore, this DC block capacitor indeed has minimum influence on the RF signal around 2 GHz. In both Figures 3.5(a) and (b), good agreement between the measurement result and simulation prediction (model from vendor) is obtained.



(a)



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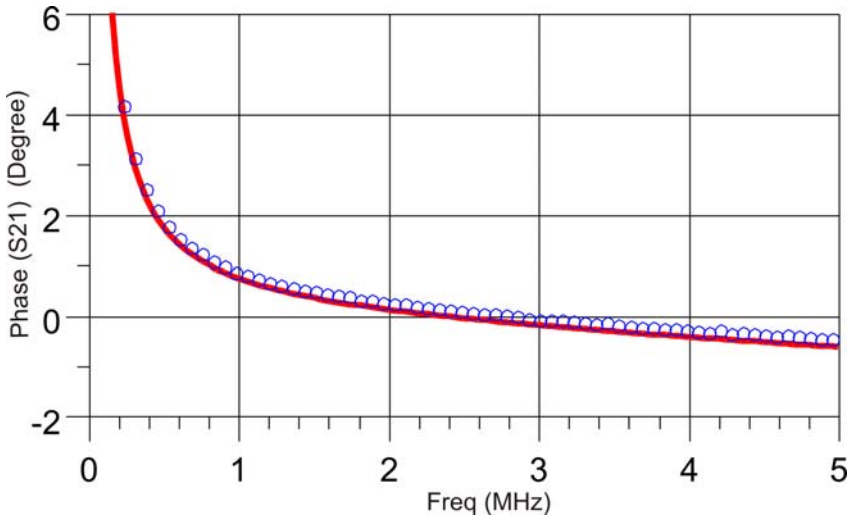


(c)

Figure 3.6 Comparison of simulation (solid lines) and measured (symbols) of S21 Phase of (a) 10 µF, (b) 1 µF and (c) 100 nF.

To improve the circuit level linearity, in particular for lowering the electrical memory effect, low baseband impedance is strongly desired [81]. This is in practice realized by making use of the series resonance of capacitors, whose series resonance frequencies are spread over the entire baseband frequency range (see Chapter 5, drain bias network design). Thus, two chip capacitors are chosen from Murata® with 10 µF (GRM32NF51E106ZA01) and 1µF (GRM32RR71H105KA01) and measured to verify models provided by the vendor. The major concern is to check the zero crossing point of the phase of S21, indicating the series resonance frequency. As the capacitance values decreases, the corresponding series resonance frequency increases (from 0.5

MHz to 5 MHz) as shown in Figures 3.6(a) and (b). 100 nF chip capacitor for designing stabilization network is also characterized. It is shown in Figure 3.6(c) that it has a series resonance frequency around 2.8 MHz. In all three cases, satisfying agreement between the model based simulation and measurement curves is obtained, which shows the successful verification of the vendor delivered model (including mounting effects) in its real circuit level. It is worth to mention that the used S-parameter measurement set up for vendor model verification is using a 50 ohm microstrip line at both ports (see Figure 3.1(a)), since the S-parameters are typically characterized in a 50 ohm environment. The soldering effects are included in the measurement results. This is also valid for chip inductor characterization in section 3.3.

It has to be pointed out that the measurement set up used for 10 µF, 1 µF, and 100 nF capacitor characterization is different from that of 22 pF, because of the different frequency band involved. Anritsu® VNA MS4640A (frequency range 70 kHz up to 70 GHz) series is used for the low frequency range measurement [82]. However, in this case the in-fixture calibration method is not needed because the operating frequency is at baseband (up to 5 MHz). Thus, the measurement is performed at the coaxial plane 1' and 2', shown in Figure 3.1(a). The length of the microstrip line in each fixture-half (25 mm) has to be included in the simulation to include the given physical connection lines.

3.3 SMD Inductor

Lumped inductor is used as RF choke inside the bias network. In this work, a 68 nH chip inductor (Coilcraft, 0603CS-68NXJLU) has been adopted for designing the gate bias network (see Chapter 5, gate bias network design). Figure 3.7 shows the equivalent circuit of the measured chip inductors [83]. L_0 is the desired inductance. L_s and R_s model the parasitic series inductance and resistance, respectively. C_p is the parasitic capacitance related to the self-resonance frequency [40]. The model topology will become more complicated with increasing operating frequency [83].

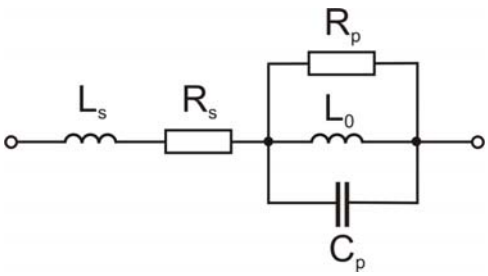
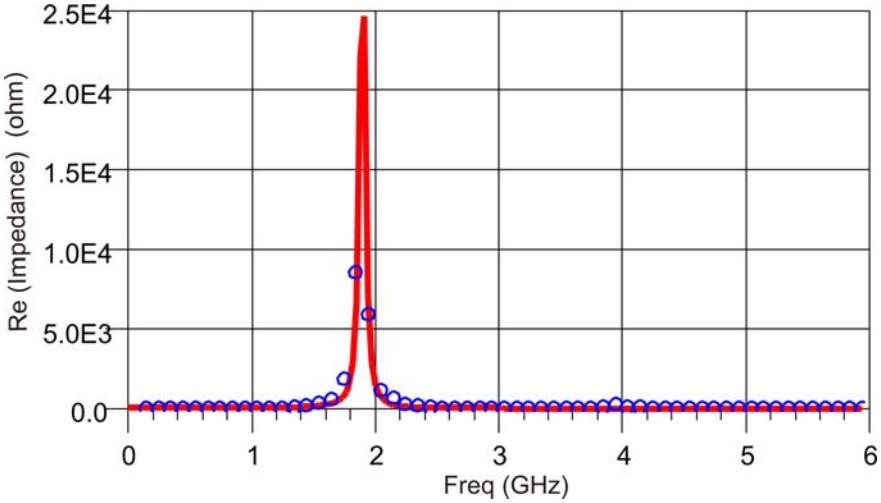
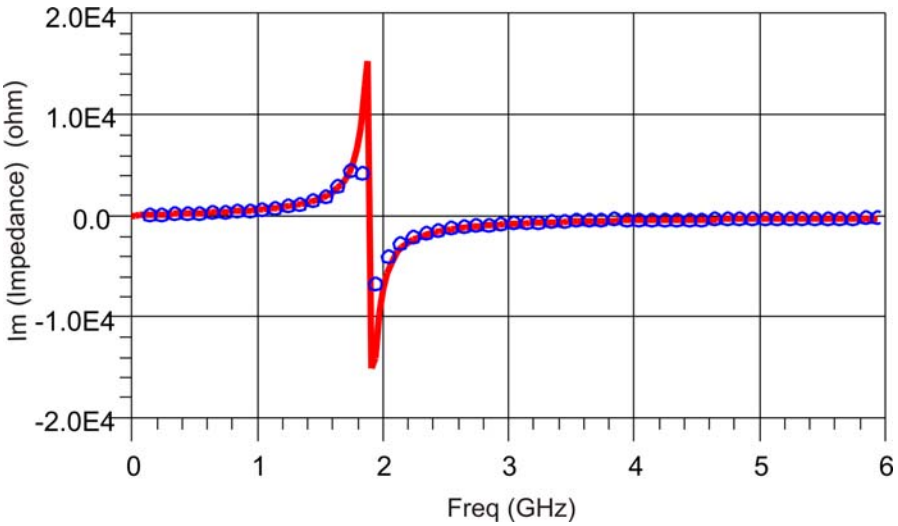


Figure 3.7 Equivalent circuit of a real chip inductor.



(a)



(b)

Figure 3.8 (a) real part of the impedance and (b) imaginary part of the impedance of the chip inductor based on the S-parameter measurement (symbols) and simulation (solid lines).

Similarly, the chip inductor with ceramic core is characterized using in-fixture measurement. Simulation and measurement are plotted in Figure 3.8(a)-(b) in terms of real and imaginary impedance part. Very good agreement is achieved within the full measured frequency range (up to 6 GHz). The self-resonance occurring around 1.9 GHz is clearly observed. Thus, this chip inductor can be used for the application at 2.1 GHz, where the inductor shows high impedance.

In this chapter, verification of the involved SMD models have been achieved successfully, on the basis of comparison with the corresponding measurement results. All the practical mounting effects are already taken into account. Thus, it has made a solid starting point for obtaining reliable circuit design, which will be thoroughly discussed in Chapter 5.

Chapter 4

Modeling of AlGaAs/GaAs HEMT Chip Device

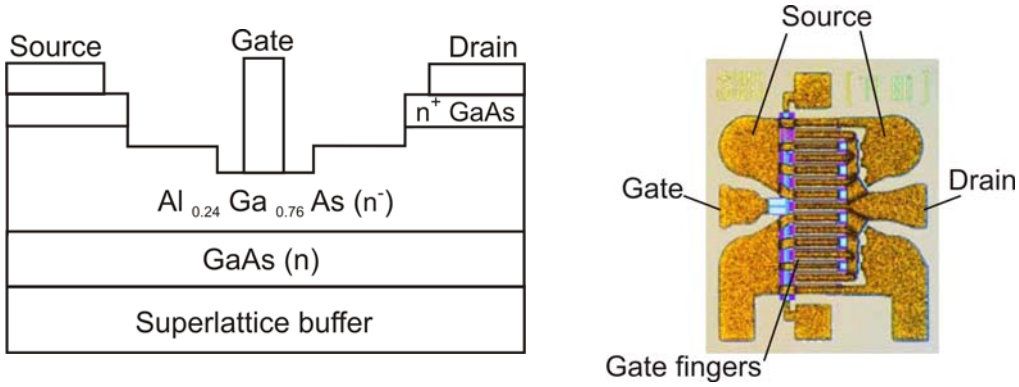
In this chapter, a large-signal model of the AlGaAs/GaAs HEMT chip device will be developed using the bottom-up modeling approach developed in the HFT Department (now renamed as Microwave Electronics Lab) [84]. GaAs HEMT device with mature technology can deliver good gain, excellent linearity and high efficiency, making it an outstanding technology for RF power amplifier applications above 2 GHz [85].

In section 4.1, device structure of the chosen 1.2 mm GaAs HEMT chip (TriQuint® TGF4230-SCC) will be given first [86]. Then, a brief summary of this chip device specification will be introduced. In section 4.2, an overview of the device modeling approach will be briefly summarized. After that, the detailed modeling procedures and the related model verification results are given in sections 4.3-4.4.

4.1 AlGaAs/GaAs HEMT Chip

As depicted in Figure 4.1, the material structure of the adopted AlGaAs/GaAs HEMT device includes a thin n-type GaAs layer (low to mid doped, 10^{17} cm^{-3}) sandwiched between a superlattice buffer layer and a low doped (10^{16} cm^{-3})

AlGaAs layer. An n^+ GaAs cap layer completes the structure. The device structure includes a 2.1 μm wide recess etched into both GaAs n^+ layer and the AlGaAs layer, and a conventional narrow gate recess. Gate length is 0.5 μm, and the total gate width is 1.2 mm [37, 86]. The source electrodes are grounded using via holes. The die thickness is 0.1 mm [86].



(a) (b)

Figure 4.1 AlGaAs/GaAs HEMT device: (a) cross section and (b) chip [37, 86].

The combination of the low doped AlGaAs layer under the gate and the highly doped channel together with the superlattice buffer layer results in a device with high gate-drain and gate-source breakdown voltage, typically 22 to 23V, and nearly constant transconductance 160 mS/mm. It has a moderately high maximum channel current (I_{MAX}) of 438 mA/mm. The high breakdown voltage allows the device to be operated with a relatively high drain voltage of up to 10V. The nearly constant transconductance gives the device high gain in class-AB and class-B [86]. It is designed to work up to 12 GHz for high efficiency power applications. Bond pads and backside metalization are gold-plated, and aluminium bond wire should therefore not be used [37].

4.2 Modeling Approach Overview

In general, there are mainly two approaches for modeling. One is physical modeling and the other is empirical modeling. Physical modeling is based on the semiconductor material, technology and the device physical-parameters. The main advantage is that it describes the device operation in terms of device physics. However, it has high computing expenditure [87]. Moreover, accurate

physical data is necessary for modeling purpose. Hence, it is more applicable for device designer. The empirical modeling (measurement based) is commonly used for amplifier design activity. It is based on several sets of measurement data such as S-parameter, waveform, and pulsed I(V) curves. This approach is able to provide high accuracy for large-signal operation since the elements are extracted based on the measurements, which emulate active device applications. The empirical model can be constructed either using analytical function or using table-based measurement data. There are several limitations for using analytical function based modeling [88-89]. It is hard to find functions that precisely describe the device operation over large voltage ranges. The fitting parameters inside may do not have any physical meaning.

Thus, table-based large-signal modeling approach is followed, for which the department has decades of experience [90-96]. It has been shown by previous research works that this approach can accurately predict the large-signal behaviour in terms of fundamental and harmonics power, and also intermodulation distortion.

As shown in Figure 4.2, the adopted table-based large-signal modeling approach is implemented in two steps.

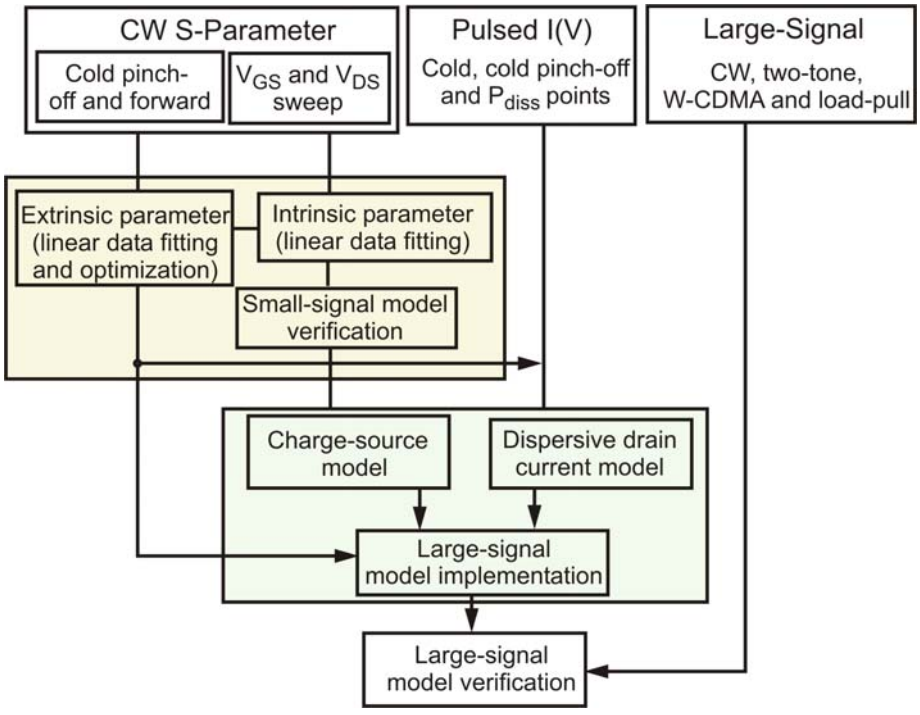


Figure 4.2 Large-signal table-based model derivation process (adopted from [97]).

The first step is developing a small-signal model (SSM), which can accurately describe the parasitic elements and the bias dependent intrinsic part of the device. The second step is to derive the large-signal model (LSM) from the developed SSM in a bottom-up constructive manner. Charge sources are obtained through surface integration and non-linear drain current is achieved through a set of pulsed I(V) measurements. The final large-signal model can account for both trapping and self-heating induced current dispersion and also linearity [96].

4.3 Small-Signal Modeling

For small-signal model extraction, the 22-element equivalent circuit model topology (shown in Fig 4.3) is adopted for the present 1.2 mm GaAs HEMT chip in use. The main advantages of this model are as follows [84]:

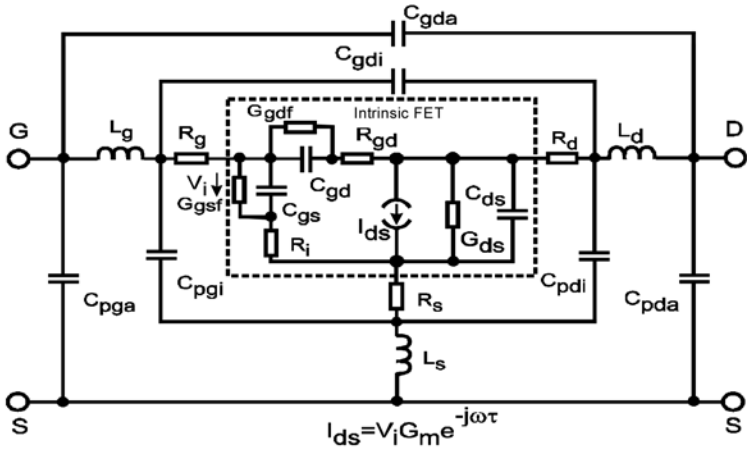


Figure 4.3 A 22-element distributed model for a GaN HEMT (adopted from [84]).

- It accounts for all the expected parasitic elements of the device.
- It reflects the physics of the device over a wide bias and frequency range.

It consists of 12 bias-independent extrinsic elements and 10 bias dependent intrinsic elements. In this model, C_{pgi}, C_{pdi}, and C_{gdi} account for the inter-electrode and crossover capacitances (due to air-bridge source connections) between gate, drain and source. While C_{pga}, C_{pda}, and C_{gda} account for parasitic elements due to the pad connections and probe tips-to-device contact

transitions. The parasitic resistances (R_g, R_d, and R_s) and inductances (L_g, L_d, and L_s) at the gate, drain, and source contacts have also been included.

4.3.1 Extrinsic Parameter Extraction

It is a very critical step to accurately extract the extrinsic parameters, since the intrinsic parameters will strongly depend on the extrinsic parameters extracted in this step. They are obtained based on a set of S-parameters, measured at cold FET operation. Optimization procedure is used to determine the final parameter values. Multi-plane data fitting and bi-directional search technique are adopted to exclude the local minimum problem during optimization [84]. In the following part, the generation of the starting values for optimization procedure will be explained in details.

The starting values of parasitic capacitance and inductance are deduced from cold pinch-off S-parameter measurement (V_{DS0} = 0V, $V_{GS0} < V_{pinch}$), while the series parasitic resistances are extracted from cold forward S-parameter measurement (V_{DS0} = 0V, V_{GS0} > 0V). The initial values evolution procedure of the adopted modeling approach is summarized as follows:

1. Under cold pinch-off state, the active equivalent circuit is reduced to a capacitive network at low frequency range (below 5 GHz for 1.2 mm device), as shown in Figure 4.4. Thus, the total branch capacitances of each branch can be easily estimated from the imaginary part of the Y-matrix, which is converted from the cold pinch-off S-parameter measurement.

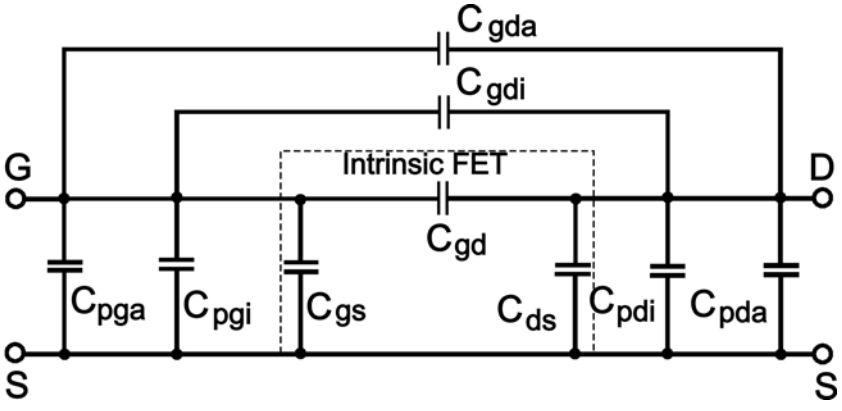


Figure 4.4 Cold pinch-off equivalent circuit at low frequency (adopted from [84]).

2. Next, the optimal distribution of the total branch capacitance is searched by scanning the C_{pga}, C_{gda}, and C_{pda} values within specified ranges (from 0 to the half of the total branch capacitance). During the iteration, C_{pga} and C_{pda} are assumed to be equal. $C_{pdi} \cong C_{pda}$ and $C_{gdi} \cong C_{gda}$ are also supposed, which differ from the ratio made for GaN HEMT device (for GaN the assumption is $C_{pdi} \cong 3C_{pda}$ and $C_{gdi} \cong 2C_{gda}$, because the permittivity is different for GaAs and GaN material) [84]. For each iteration:

   - De-embedding the extrinsic capacitances, converting Y-parameter to Z-parameter is made. The parasitic extrinsic inductances are determined from the imaginary part of this Z-parameter at high frequency range (above 5 GHz). The resistance can be de-embedded from the real part of the stripped Z-parameter.

   - At this point, all extrinsic elements are estimated and can be de-embedded from the measured S-parameters. This leads to the intrinsic transistor Y-parameters. Thus, the intrinsic elements of the model can be determined.

   - The resulting models are then used to simulate the cold pinch-off S-parameters, which are then compared with the measurement result to calculate the residual fitting error through the defined error function.

   - At the end, the best capacitance distribution is selected corresponding to the lowest error of all iterations. The related extrinsic capacitances and inductances are saved.

3. Determination of the starting value of extrinsic resistances is done with the cold forward measurement data, because the resistances become dominant under positive biased gate voltage (V_{GS0} = 1.61V, V_{DS0} = 0V), resulting in a more reliable starting value. Firstly, the determined extrinsic capacitances and inductances (step 2) are de-embedded from cold

forward measurement. Then, the resistances are determined from the stripped cold forward Z-parameters.

4. At this stage, all the starting values of the extrinsic elements are determined. Then, they are delivered to an optimization program (written in Matlab®) to generate the final extrinsic parameters.

Complete starting values of the 22-model parameters determined from cold measurements are listed in Table 4.1. The final extrinsic elements after optimisation are listed in Table 4.2. Regarding the extracted resistance values, they are not far from the starting values, which emphasize the reliability of the approach on cold forward measurement to get the parasitic resistance starting values.

Table 4.1 Starting values for the 22-element equivalent circuit model of a 1.2 mm GaAs HEMT derived from measurement (pinch-off and forward).

Extrinsic Parameters		**Intrinsic Parameters**	
C_{pga} = 112.5 fF C_{pda} = 112.5 fF C_{gda} = 0.0 fF C_{pgi} = 12. 484 fF C_{pdi} = 112.5 fF C_{gdi} = 0.0 fF	L_g= 37.09 pH L_d = 15. 87 pH L_s = 6.709 pH R_g = 1.498 Ω R_s = 0. 755 Ω R_d = 1.445 Ω	C_{gs} = 263. 998 pF C_{ds} = 85.920 pF C_{gd} = 271.008 pF R_i = 0.0 Ω R_{gd} = 0.0 Ω τ = 9.8586 ps	G_m = 0.0 mS G_{ds}= 0.0 mS G_{gsf} = 0.02 mS G_{gdf} = 0.0 mS

Table 4.2 Optimized device parameters of a 1.2 mm GaAs HEMT.

Extrinsic Parameters		**Intrinsic Parameters**	
C_{pga} = 134.90 fF C_{pda} = 100.93 fF C_{gda} = 0.0 fF C_{pgi} = 14.622 fF C_{pdi} = 143.608 fF C_{gdi} = 0.0 fF	L_g= 45.001 pH L_d = 20.467 pH L_s = 13.323 pH R_g = 1.3395 Ω R_s = 0.6896 Ω R_d = 1.3712 Ω	C_{gs} = 263. 998 pF C_{ds} = 85.920 pF C_{gd} = 271.008 pF Ri = 0.0 Ω Rgd = 0.0 Ω τ = 10.4302 ps	G_m = 0.0 mS G_{ds}= 0.0 mS G_{gsf} = 0.02 mS G_{gdf} = 0.0 mS

4.3.2 Intrinsic Parameter Extraction

After de-embedding the extrinsic parasitic elements, the bias dependent intrinsic elements can be extracted by a linear data fitting method [98]. Through the

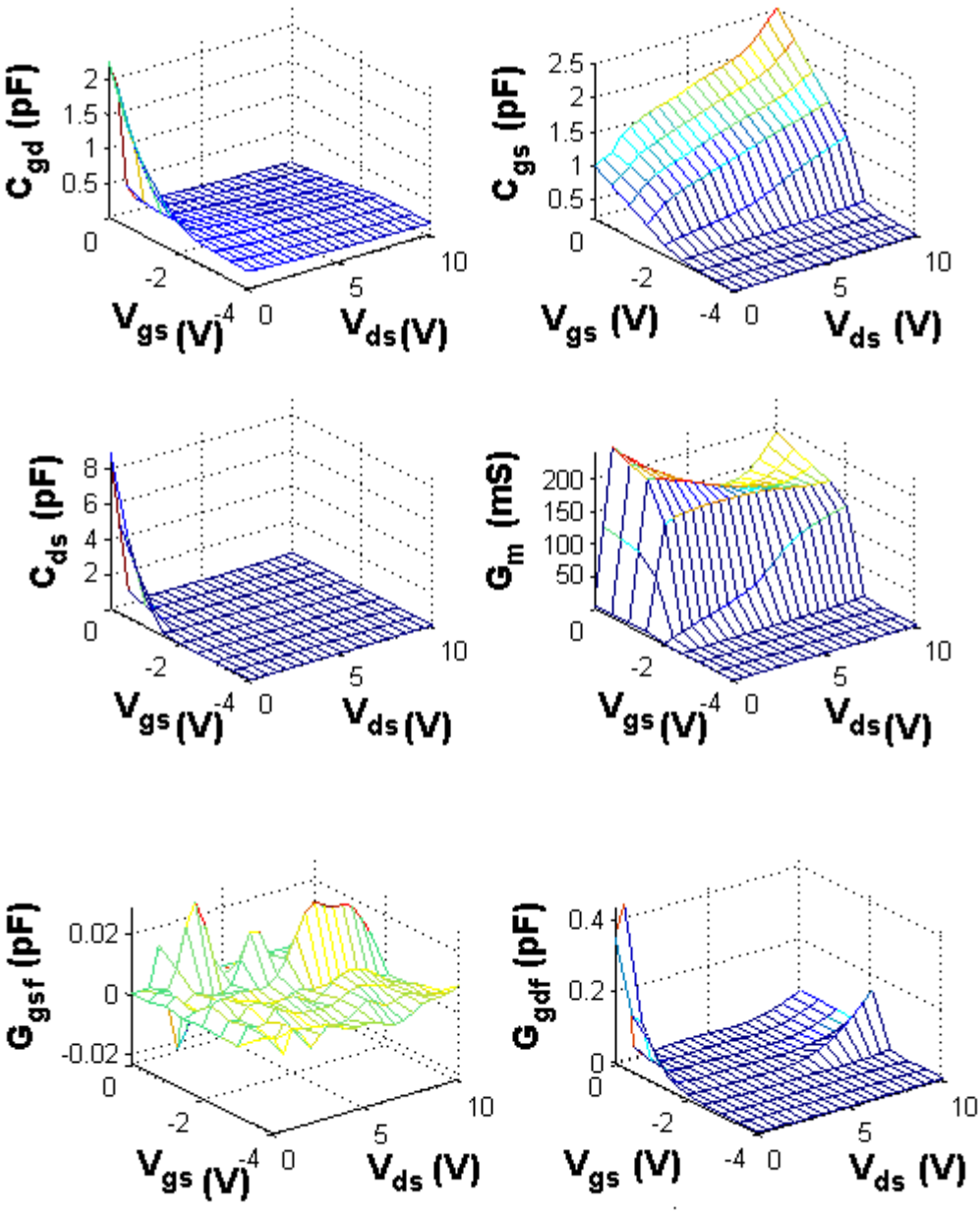
intrinsic Y-parameters, the admittances of the intrinsic HEMT can be expressed as follows:

$$Y_{gs} = Y_{i,11} + Y_{i,12} = \frac{G_{gsf} + j\omega C_{gs}}{1 + R_i G_{gsf} + j\omega R_i C_{gs}} \qquad (4.1a)$$

$$Y_{gd} = -Y_{i,12} = \frac{G_{gdf} + j\omega C_{gd}}{1 + R_{gd} G_{gdf} + j\omega R_{gd} C_{gd}} \qquad (4.1b)$$

$$Y_{gm} = Y_{i,21} - Y_{i,12} = \frac{G_m e^{-j\omega\tau}}{1 + R_i G_{gsf} + j\omega R_i C_{gs}} \qquad (4.1c)$$

$$Y_{ds} = Y_{i,22} + Y_{i,12} = G_{ds} + j\omega C_{ds} \qquad (4.1d)$$



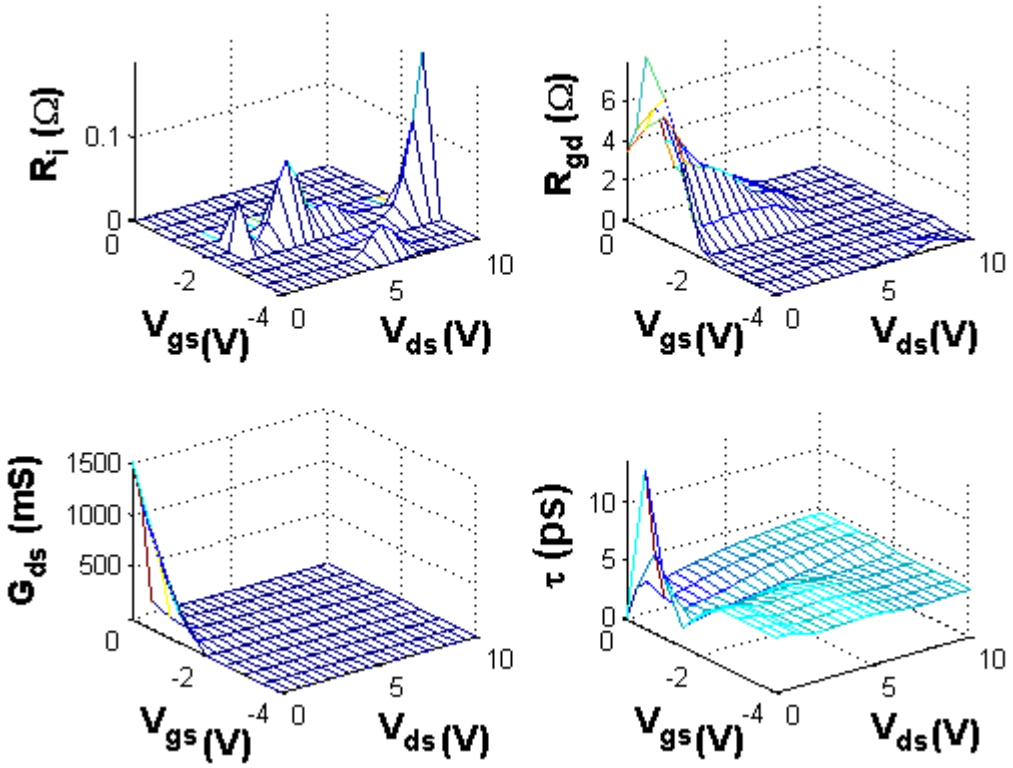
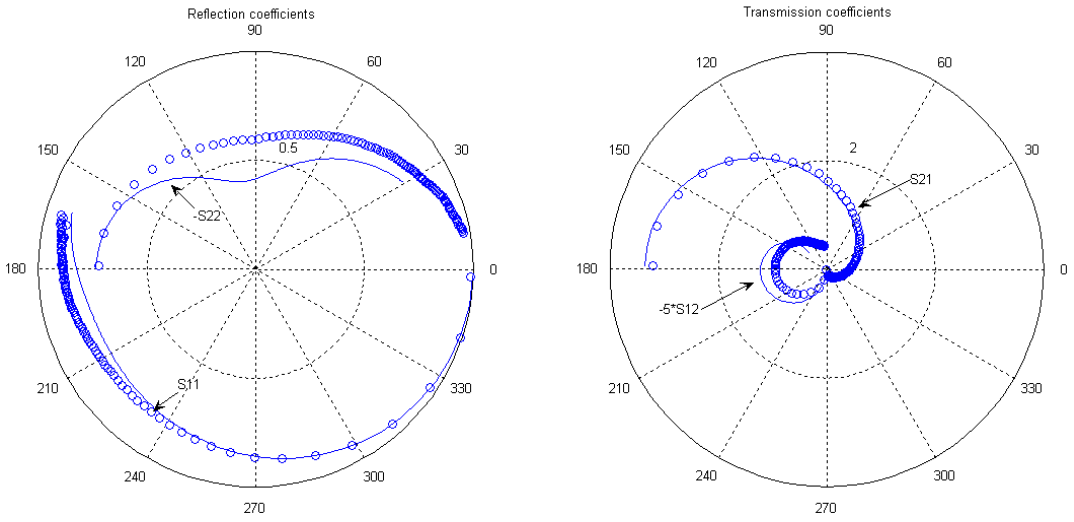


Figure 4.5 Extracted intrinsic elements as a function of intrinsic bias voltages (V_{gs} and V_{ds}) for a 1.2 mm GaAs HEMT.

The extracted bias dependent intrinsic elements as a function of intrinsic gate-source (V_{gs}) and drain-source voltage (V_{ds}) are shown in Figure 4.5. Physical proper values are obtained, according to the theoretical bias dependency. Similar shapes are obtained with the ones reported in [90]. C_{gd} is formed due to the extension of the depletion region into the gate-drain space. Smaller C_{gd} values are shown with increasing drain voltage since the extension of depletion increases with increasing drain voltage. C_{gs} is formed by the gate metal and the 2-DEG channel charge. At the gate voltage V_{gs} = 0V, C_{gs} decreases in the pinch-off region (V_{gs} < 2V) and gradually increases with drain voltage. This is due to the lateral electric field established by the drain voltage, which accelerates charge carriers in the channel to scatter into the barrier layer. The physical origin of C_{ds} is from the high-field part of the depletion layer, which separates the source and drain electrodes into an electrostatic sense. Hence, higher values for C_{ds} are obtained in the ohmic region owing to the reduction of the high-field part. G_m surface shows also physical behaviour, as it increases with increased gate voltage and also increases linearly with the drain voltage in

the ohmic region. The other bias dependent intrinsic parameters have shown also physical behaviour. The detailed explanations from a physics point of view can be found in [84].

The validity of the extracted element values are confirmed by comparison of measured and simulated S-parameters. Figure 4.6 shows comparison of the S-parameters at a class-AB bias point. The good agreement indicates the capability of the equivalent circuit topology to model the device small-signal performance.



Radius: 1 Radius: 4

(Frequency from 45 MHz to 40 GHz)

Figure 4.6 S-parameter comparison between measurement (symbols) and simulation (solid lines) of the 1.2 mm GaAs HEMT biased at class-AB point (V_{GS0} = -2.08V, V_{DS0} = 6V).

4.4 Large-Signal Modeling

In this section, the large-signal modeling of AlGaAs/GaAs HEMT device will be presented. The equivalent circuit of large-signal model is shown in Figure 4.7. It is derived from the distributed small-signal model [96].

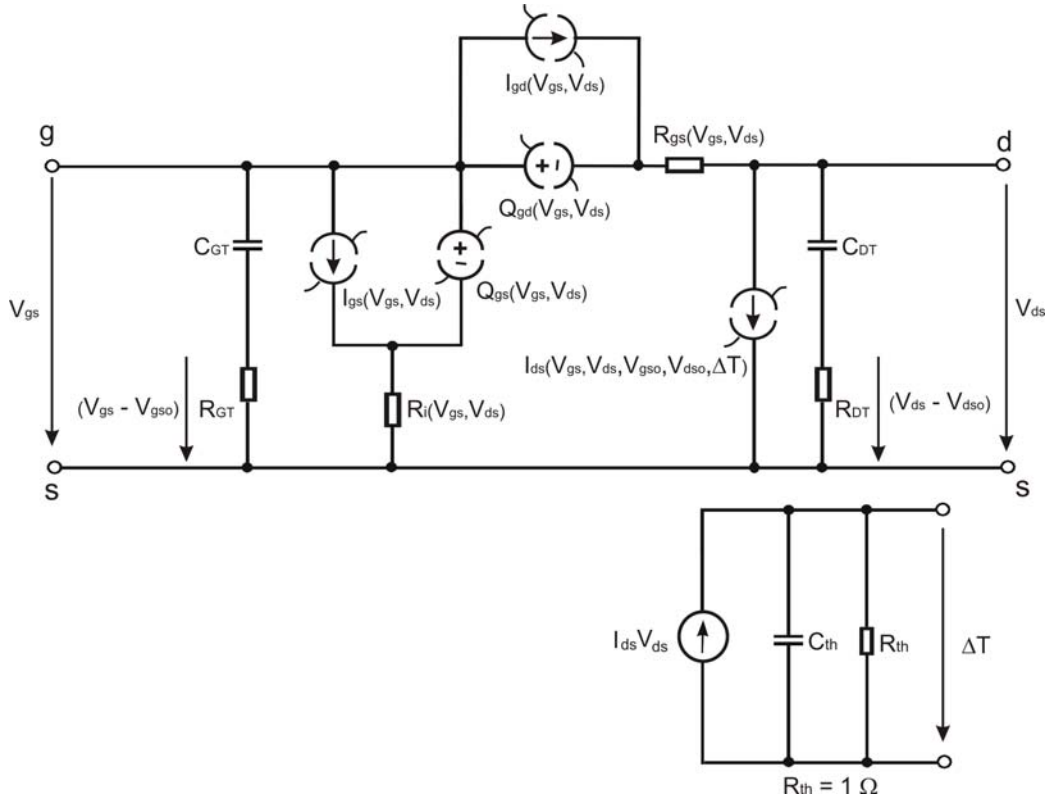


Figure 4.7 Large-signal model including self-heating and trapping effects (adopted from [96]).

The quasi-static gate current sources and gate charge sources are obtained through path-independent integration of corresponding gate conductance and capacitance, respectively. They are used to describe the conduction current and displacement current. Non-quasi-static effect of the charge sources is approximately modelled by using two bias dependent series resistances (R_i and R_{gd}) in the gate-source and gate-drain branches. By taking into account the essential charging time for the depletion region capacitances, it improves the model prediction at millimetre wave frequency.

Moreover, the improved drain current model accounts for the current dispersion phenomenon caused by trapping effects and self-heating effects, giving a more accurate performance prediction [84]. As shown in Figure 4.7, a series capacitor and resistor are added at both gate and drain branches. These RC high-pass circuits are intended to model gate and drain trapping effects. C_{GT} and C_{DT} are selected in the order of 1 pF to model the stored charges in the surface and buffer layer. The R_{GT} and R_{DT} are chosen in the order of 1 MΩ to model the small leakage current. Implicitly, the RC products give the proper trapping

constant (10^{-5} – 10^{-4} s) [96]. This implementation makes the equivalent circuit physically more meaningful.

Self-heating deduced current dispersion is controlled with normalized channel temperature rise ΔT. The thermal capacitance C_{th} is chosen to define a transit time constant in the order of 1 ms [84]. The value of thermal resistance R_{th} is normalized to 1Ω, since its value is incorporated in thermal fitting parameter in the current model expression [84].

4.4.1 Gate Current and Charge Models

As mentioned above, gate current can be obtained by the integral of G_{gsf} and G_{gdf} using the following equations (4.2a-b), under the assumption that G_{gsf} is only dependent on the gate-source voltage [84]:

$$I_{gs}(V_{gs},V_{ds}) = I_{gs}(V_{gs0},V_{ds0}) + \int_{V_{gs0}}^{V_{gs}} G_{gsf}(V,V_{ds0})dV \qquad (4.2a)$$

$$I_{gd}(V_{gs},V_{ds}) = I_{gd}(V_{gs0},V_{ds0}) + \int_{V_{gs0}}^{V_{gs}} G_{gdf}(V,V_{ds0})dV - \int_{V_{ds0}}^{V_{ds}} G_{gdf}(V_{gs},V)dV \qquad (4.2b)$$

This modeling approach is simpler than obtaining the gate currents from DC measurement [96]. Also, gate conductance could be more accurate for describing the gate current than the DC measurements. The resulted I_{gs} and I_{gd} as a function of the intrinsic voltage are shown in Figure 4.8.

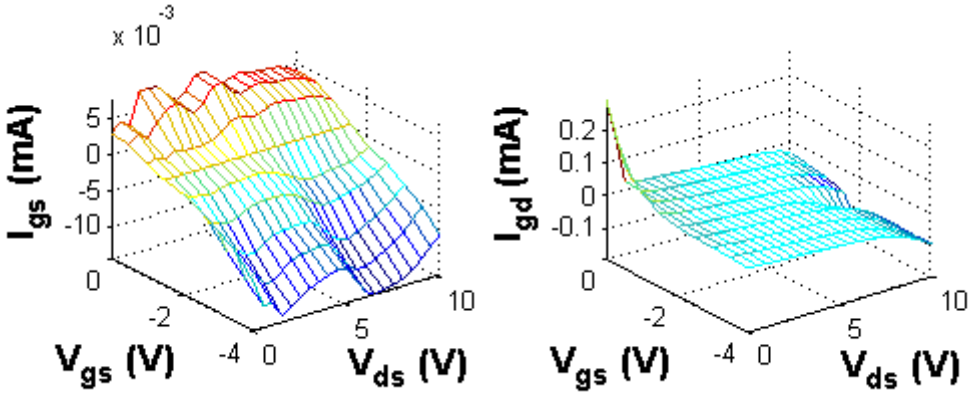


Figure 4.8 Extracted gate current sources I_{gs} and I_{gd} versus intrinsic voltages (V_{gs} and V_{ds}) for a 1.2 mm GaAs HEMT.

To include the effect of C_{gs}, C_{gd}, and C_{ds} while maintaining the consistency of the large-signal model, the charge sources Q_{gs} and Q_{gd} have been formulated by integrating C_{gs}, C_{gd}, and C_{ds} as given in the equations:

$$Q_{gs}(V_{gs},V_{ds}) = \int_{V_{gs0}}^{V_{gs}} C_{gs}(V,V_{ds0})dV + \int_{V_{ds0}}^{V_{ds}} C_{ds}(V_{gs},V)dV \tag{4.3a}$$

$$Q_{gd}(V_{gs},V_{ds}) = \int_{V_{gs0}}^{V_{gs}} C_{gd}(V,V_{ds0})dV - \int_{V_{ds0}}^{V_{ds}} [C_{ds}(V_{gs},V) + C_{gd}(V_{gs},V)]dV \tag{4.3b}$$

The obtained surfaces of Q_{gs} and Q_{gd} versus intrinsic gate and drain voltage are shown in Figure 4.9.

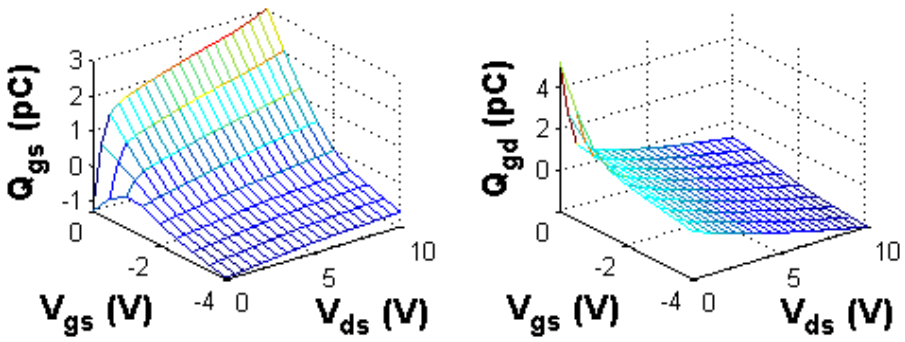


Figure 4.9 Calculated gate charge sources Q_{gs} and Q_{gd} versus intrinsic voltage (V_{gs} and V_{ds}) for a 1.2 mm GaAs HEMT.

4.4.2 Drain Current Model

The non-linear drain current model is formulated as in equation [84]:

$$\begin{aligned} I_{ds}(V_{ds},V_{gs},V_{ds0},V_{gs0},P_{diss}) = I_{ds,iso}^{DC}(V_{gs},V_{ds}) + \alpha_G(V_{gs},V_{ds})(V_{gs}-V_{gs0}) \\ + \alpha_D(V_{gs},V_{ds})(V_{ds}-V_{ds0}) + \alpha_T(V_{gs},V_{ds})P_{diss} \end{aligned} \tag{4.4}$$

where $I_{ds,iso}^{DC}$ is the isothermal drain current after de-embedding the self-heating effect. α_G and α_D model the deviation in the drain current due to the surface trapping and buffer trapping, respectively. α_T models the deviation in the drain current due to the self-heating effect. Hence, the drain current is considered as a summation of dispersionless DC current and other dispersion contributions

due to RF current components. The amount of trapping induced current dispersion depends on the rate of dynamic change of the applied intrinsic V_{gs} and V_{ds} with respect to those average values V_{gs0} and V_{ds0}. In other words, this current dispersion is mainly stimulated with the RF or the AC component of the gate-source and drain-source voltages, which is described by (V_{gs}-V_{gs0}) and (V_{ds}-V_{ds0}) in (4.4). The self-heating induced dispersion is caused mainly by the low frequency components of the drain signals. Thus, P_{diss} in (4.4) accounts for the static and quasi-static intrinsic power dissipation.

The four parameters $I_{ds,iso}^{DC}$, α_G, α_D, and α_T can be extracted from at least four sets of pulsed I(V) measurement, which are set at proper quiescent bias points. First of all, trapping effects can be characterized by pulsed I(V) measurements at negligible device self-heating. To determine the surface trapping effect, the device is biased at two quiescent bias points:

$V_{GSO} < V_P$, $V_{DSO} = 0V$ ($P_{diss} \approx 0$)
$V_{GSO} = 0V$, $V_{DSO} = 0V$ ($P_{diss} \approx 0$).

In this case, the current variation is assumed to be caused only by the surface trapping. A set of pulsed I(V) measurements taken at these two quiescent bias point are shown in Figure 4.10.

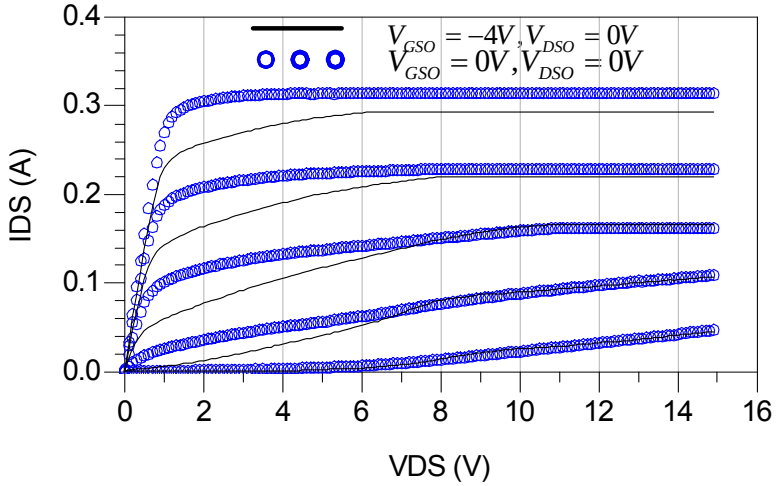


Figure 4.10 Pulsed I(V) characteristic of the 1.2 mm GaAs HEMT at zero quiescent drain voltage to characterize the surface trapping.

The buffer trapping effects can be characterized using the following two quiescent bias points:

$$V_{GSO} < V_P,\ V_{DSO} = 0V\ (P_{diss} \approx 0)$$
$$V_{GSO} < V_P,\ V_{DSO} >> 0V\ (P_{diss} \approx 0).$$

A set of pulsed I(V) measurements taken at these two bias points is shown in Figure 4.11. Thus, the $I_{ds,iso}^{DC}$, α_G, and α_D surfaces can be extracted from the performed measurement data. The resulting surfaces are shown in Figure 4.12.

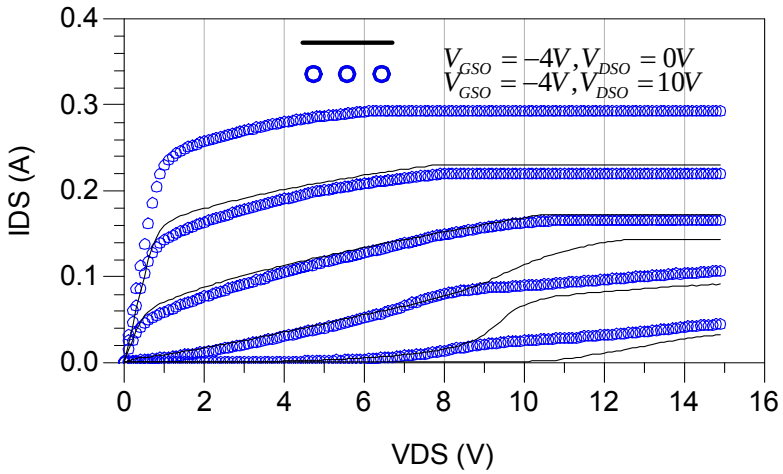
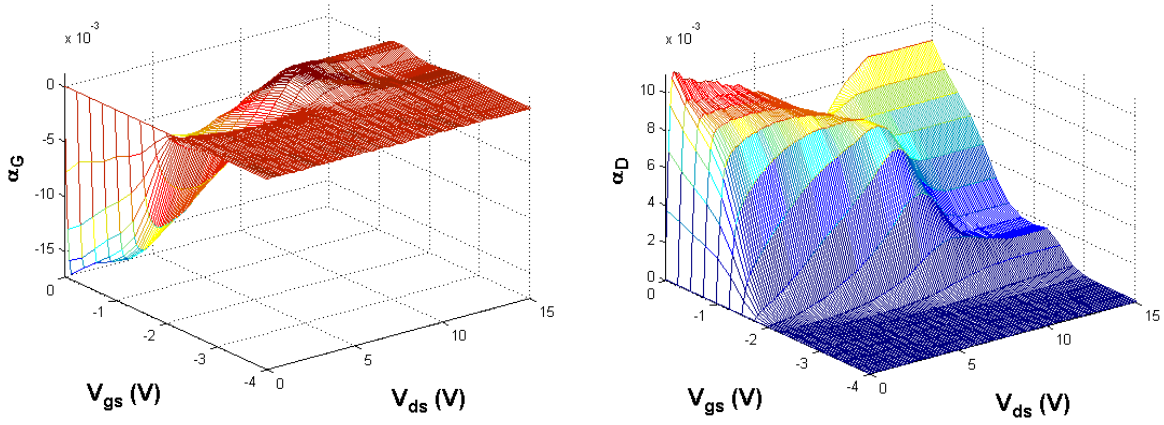


Figure 4.11 Pulsed I(V) characteristic of the 1.2 mm GaAs HEMT at quiescent gate voltage (below the pinch-off) to characterize the buffer trapping.



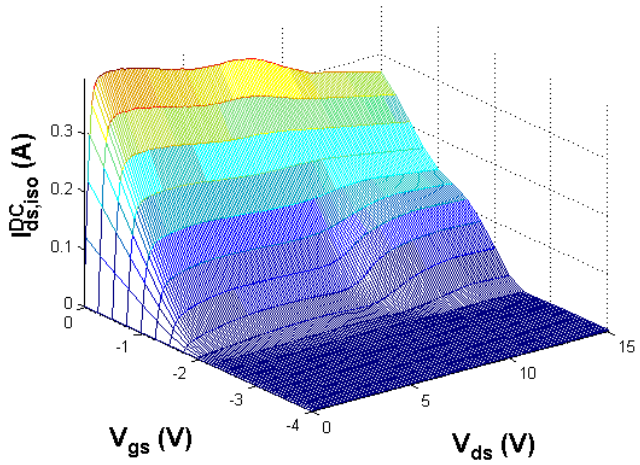


Figure 4.12 Bias-dependent drain current model fitting parameters α_G , α_D , and the extracted isothermal drain current of the 1.2 mm GaAs HEMT.

The self-heating induced current dispersion can be characterized at one or more active bias points ($P_{diss} \neq 0$). In this case, active pulsed I(V) measurements are taken at two quiescent bias points (V_{GS0} = -2.1V, V_{DS0}= 9V) and (V_{GS0} = -1.8V, V_{DS0} = 8V). From these performed measurements, the fitting parameter α_T surface can be extracted. It is shown in Figure 4.13.

Now, all the needed gate charge sources (Q_{gs}, Q_{gd}), currents (I_{gs}, I_{gd}), and the drain current model parameters are determined. These coefficients can be written in CITI-file format to be implemented in ADS as a table-based model. The large-signal model is implemented in a symbolically defined device (SDD) in ADS.

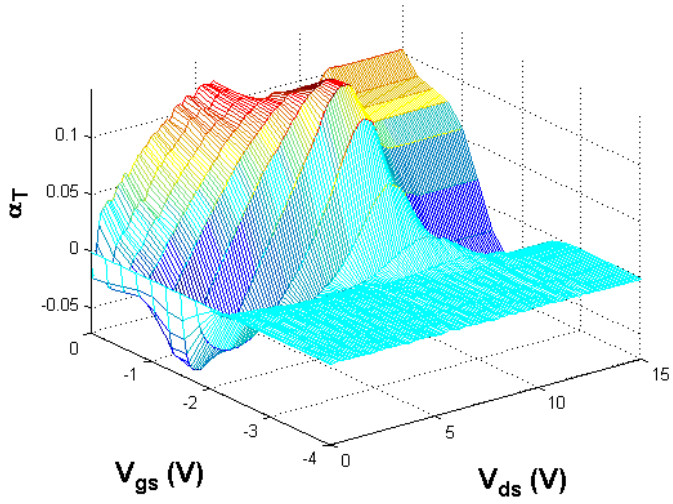
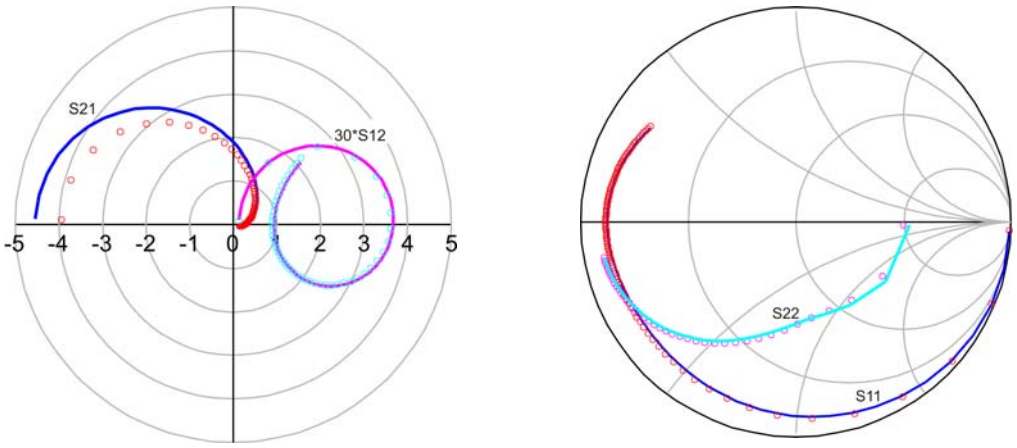


Figure 4.13 Bias-dependent drain current model fitting parameter α_T of a 1.2 mm GaAs HEMT.

4.4.3 Model Verification

Now, the obtained large-signal model will be thoroughly verified by various measurements. First, it will be verified by S-parameter measurements regarding the model consistency. In general, the model shows good S-parameter prediction at large bandwidth, as shown in Figure 4.14. As explained in the last section, the non-linear gate elements of the model, which strongly influence S11 and S12, are extracted from S-parameter measurement data. Therefore, the model gives better simulation for S11 and S12, because of using the same measurement system to extract and validate the model. However, the drain current in the model, which contributes to the simulation of S22 and S21, is extracted from pulsed I(V) measurements. Nevertheless, the agreement of measured and simulated output reflection coefficient S22 is excellent, whereas the transmission coefficient S21 shows some small discrepancy (measured |S21| = 4, simulated |S21| = 4.5).



Radius: 5 Radius: 1

(Frequency from 45 MHz to 40 GHz)

Figure 4.14 Comparison of measured (symbols) and simulated (solid lines) S-parameter for a 1.2 mm GaAs HEMT at V_{GS0} = -2.08V, V_{DS0} = 9V.

4.4.3.1 Pulsed I(V) Characteristic

Pulsed I(V) simulation has been performed at quiescent bias conditions different than the used ones for model fitting parameter extraction. Figure 4.15 shows pulsed I(V) simulations under two different quiescent bias conditions at constant ambient temperature. The very good agreement shows the ability of the model

for predicting the bias dependence of the trapping and self-heating effects. Also, the simulations verify the convergence behaviour of the model response under pulsed stimulation, which is very important for digital applications.

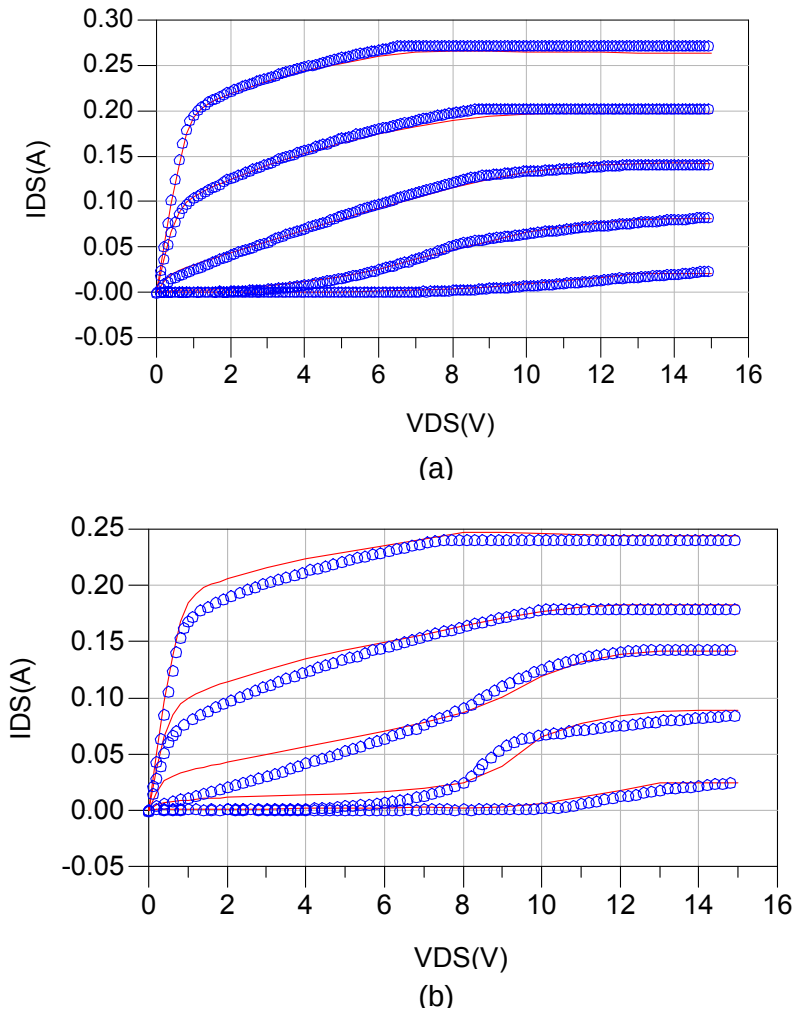
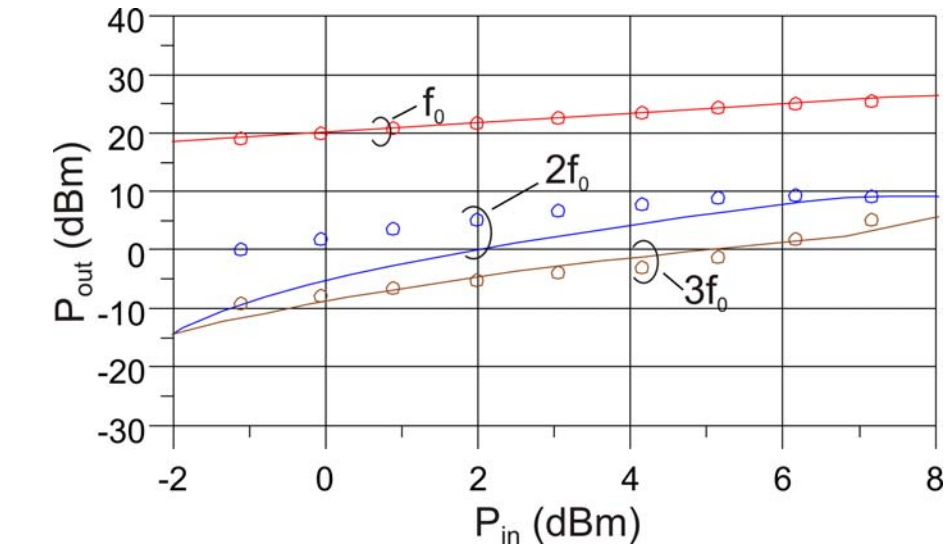


Figure 4.15 Pulsed I(V) simulation (solid lines) and measurement (symbols) for a 1.2 mm GaAs HEMT at different quiescent bias points for V_{GS} = -2.25V to –0.25V in step of 0.5V: (a) V_{GS0}= -2V, V_{DS0} = 9V and (b) V_{GS0}= -2.6V, V_{DS0} = 9V.

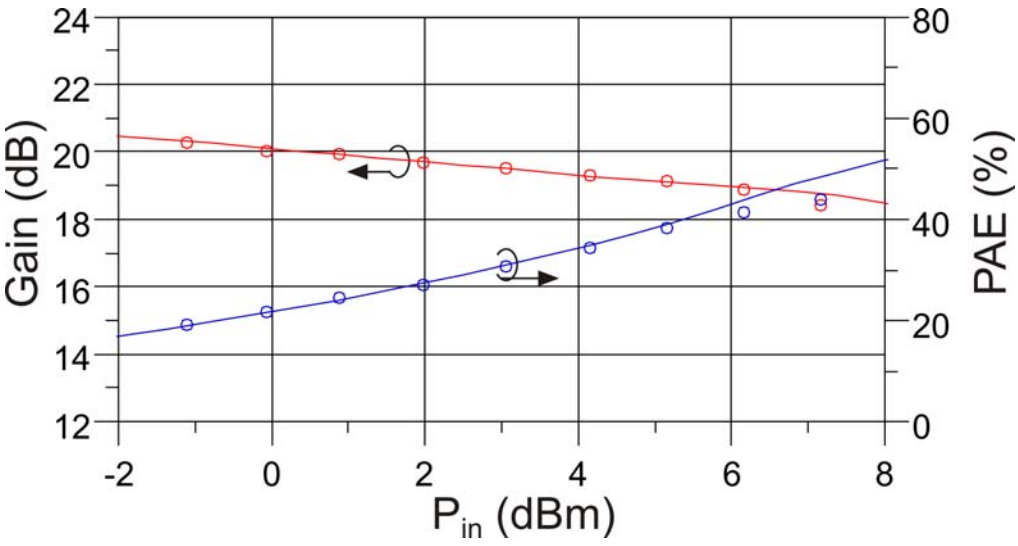
4.4.3.2 Output Power and Efficiency

The prediction capability of the large-signal model concerning the output power and power efficiency is a vital figure of merit judging the quality of the developed model.

A single-tone power sweep measurement is performed for this purpose. It has been performed using the measurement set-up reported in [99]. The results depicted in Figure 4.16 show a very good agreement for the fundamental output power, gain, and efficiency for output power level up to 1 dB compression point. The model also shows good prediction for the higher harmonic output power.



(a)

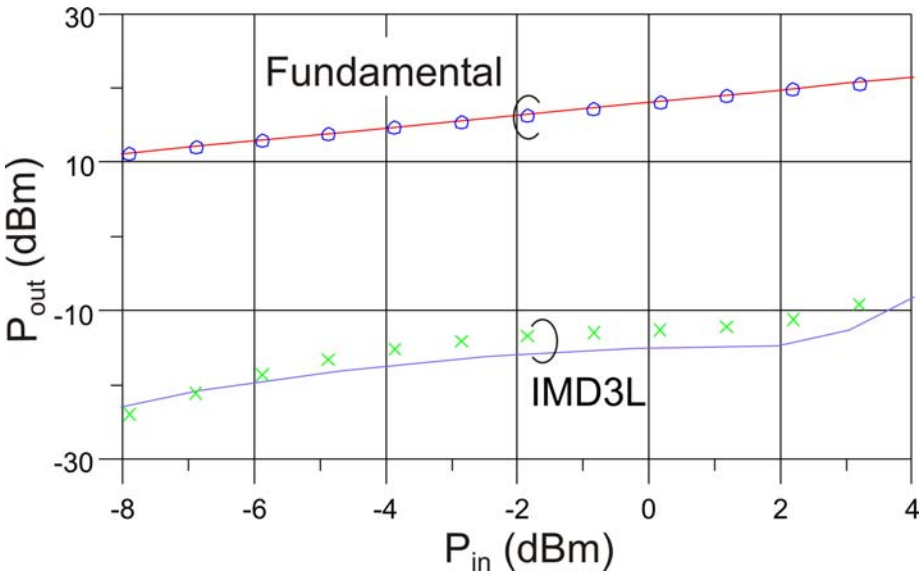


(b)

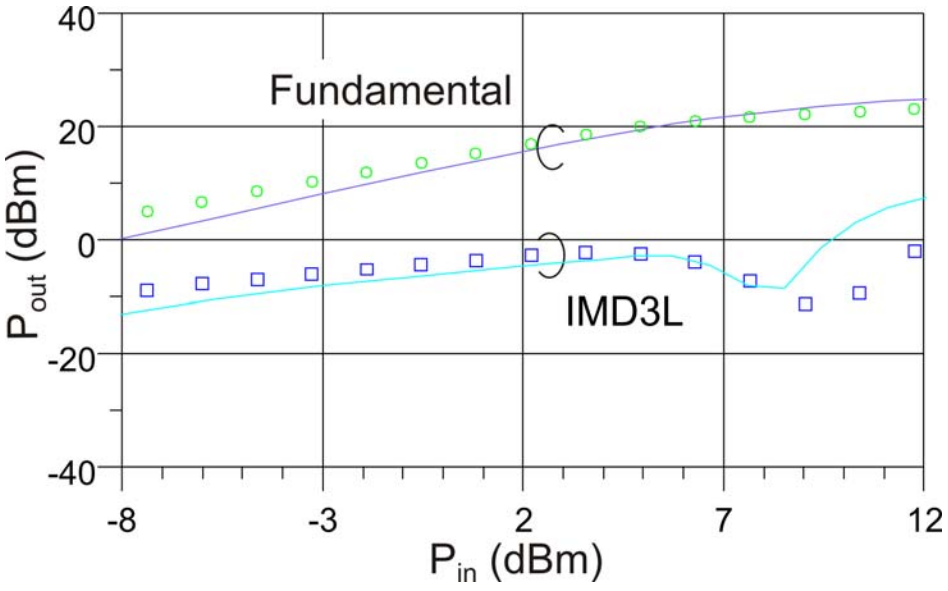
Figure 4.16 Single-tone power sweep simulations (solid lines) and measurement (symbols) for class AB bias point (V_{GS0} = -1.85V, V_{DS0} = 8V) at 2.14 GHz in a 50Ω environment.

4.4.3.3 Intermodulation Distortion

The conventional two-tone test is adopted to test the linearity prediction capability of the model. The used two-tone test set up is reported in [81]. A 200 kHz tone spacing at 2.14 GHz is used as stimulus. At class AB bias point, the comparison is done and the results are shown in Figure 4.17.



(a)



(b)

Figure 4.17 Two-tone excitation (f_0 = 2.14 GHz, Δf = 200 kHz) power sweep simulations (lines) and in-house measurement (symbols) for: (a) class AB biased point (V_{GS0} = -1.85V, V_{DS0} = 8V) and (b) class C biased point (V_{GS0} = -2.6V, V_{DS0} = 9V) in a 50Ω environment.

It can be clearly seen that the IMD products can be predicted accurately from low power to high power range. What is more interesting is that the model can even accurately predict the sophisticated sweet-spot occurrence, as shown in Figure 4.17 (b). The excellent non-linearity prediction, which is a critical point for power amplifier design, will greatly assist the RF designer to achieve the reliable circuit design in an efficient way.

Chapter 5

Demonstrator Design of a Class-AB Power Amplifier Following the Partitioning Approach

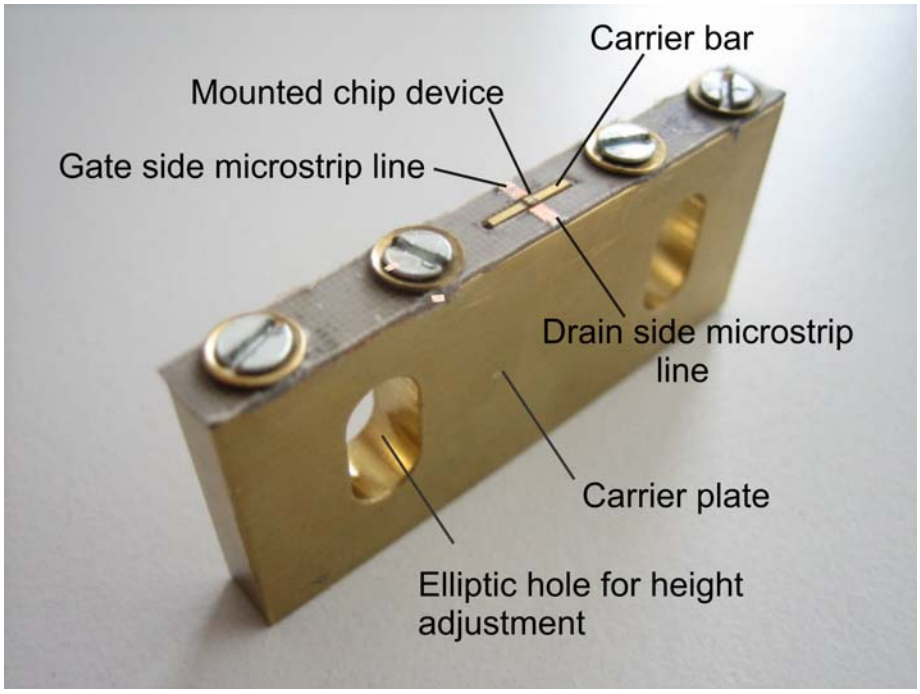
In this chapter, the demonstrator of a single ended class-AB power amplifier operating at 2.14 GHz center frequency employing AlGaAs/GaAs HEMT technology will be designed and characterized. As depicted in Figure 1.2, single ended power amplifier usually consists of active device, gate bias network, drain bias network, input impedance matching network, and output impedance matching network. Consequently, the entire power amplifier will thus be built up by tackling the individual parts in the sequence from inner to exterior.

Based on the research results obtained in the previous chapters, the complete design procedure of the amplifier circuit following the proposed partitioning design approach will be shown step by step. Each intermediate design should be verified by its corresponding measurement, as explained previously. Following design step will be conducted based on the successful design verification of the achieved parts. Hence, discrepancy can be localized easily and fixed more efficiently. The specific superiority of the proposed partitioning design approach will become obvious, with the comparison of the power amplifier designed using the conventional design approach at the end.

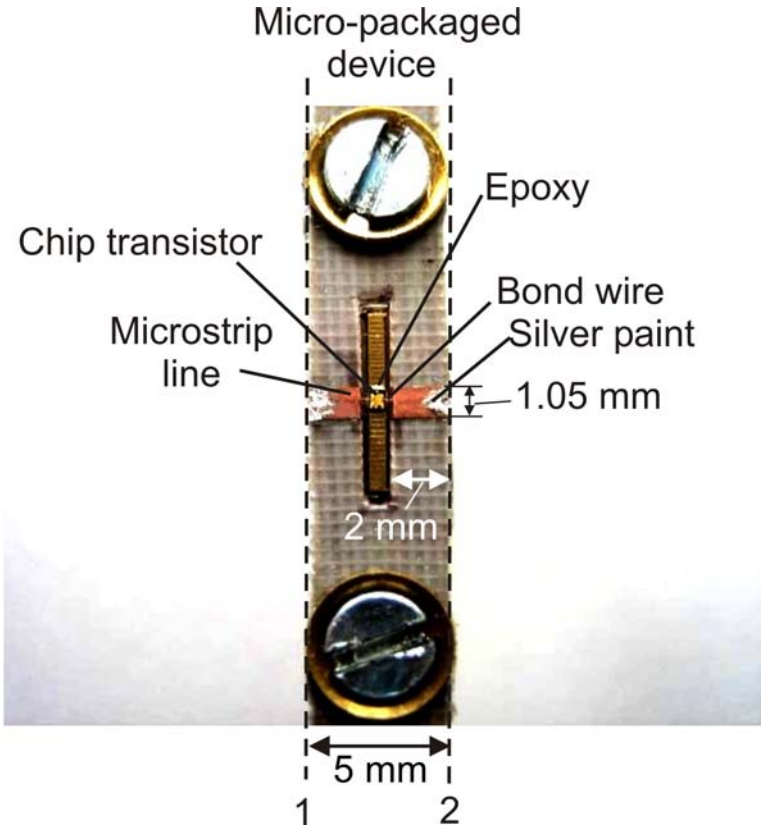
In sections 5.1-5.3, design of the micro-packaged device, bias networks and matching networks will be carried out separately. Finally, the assembled complete power amplifier performance will be characterized in section 5.4.

5.1 Micro-Packaged Device Characterization

To use transistor die in the power amplifier circuit, the active device firstly has to be mounted on a carrier plate for mechanical support and heat sinking. In industry, there are versatile commercial forms available for transistor packaging made up of ceramic, metal, and plastic [24-25]. Obviously, package adds parasitic reactance, losses, and thermal limitations as well. Thus, it becomes much more challenging to deal with packed power transistor other than with the bare die chip, especially when there is pre-matching circuits contained inside the package. Multi-bonding wires and MOS (metal over semiconductor) capacitors are usually adopted to construct the internal matching circuits for commercial packages. Package parasitic effects associated with the specific mounting environment have to be deeply analyzed and accurately modelled for the success and efficient power amplifier circuit design [100-102].



(a)



(b)

Figure 5.1 (a) Mounted transistor on the brass made carrier-plate, and (b) top view of the micro-package mounted device.

As shown in Figure 5.1, GaAs HEMT chip transistor is mounted on the brass made carrier using electrical conductive silver epoxy. It has already been pointed out in section 2.1, that the die attach plays a key role in terms of the operation reliability [103]. Persistent adhesivity and good grounding must be guaranteed; otherwise, long-term operation reliability will become doubtful, and even significant performance degradation can appear. One single gold bond wire with 25 μm diameter is used to connect the chip gate pad and drain pad with the microstrip line for input signal and output signal, respectively (see Chapter 2). The source pad of the HEMT transistor is already connected with the backside metallization layer internally. Brass carrier behaves directly as ground plate and no extra bond wire is needed for source connection. However, the performance degradation resulted from the parasitics of conductive epoxy should be taken into account in the circuit design procedure [104].

The brass plate is designed with the shape depicted in Figure 5.2, with central part manufactured with protruding shape. Therefore, the chip is nearly on the same height as the substrate and can be easily bonded. The substrate used is Teflon (the dielectric constant has been precisely determined in Appendix B) and it can be cut using sharp scalpel together with a straight ruler carefully. The slot should be cut as exact as possible to fit the chip width (approximately 0.8 mm) to minimize the length of bond wire needed. The end of the microstrip line should be flat. Otherwise, it would be difficult to perform wire bonding on non-flat surface. This would force the bonding wire to be made longer, and it also would make the precise modeling of bonding parasitic effects more difficult.

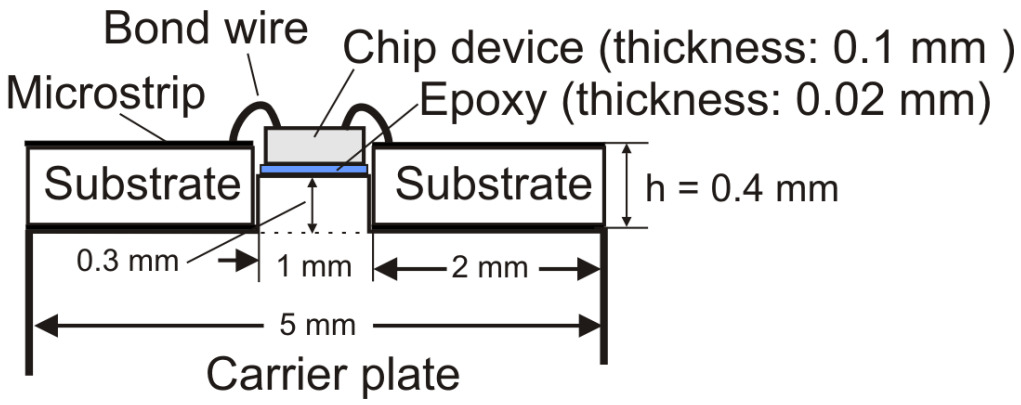
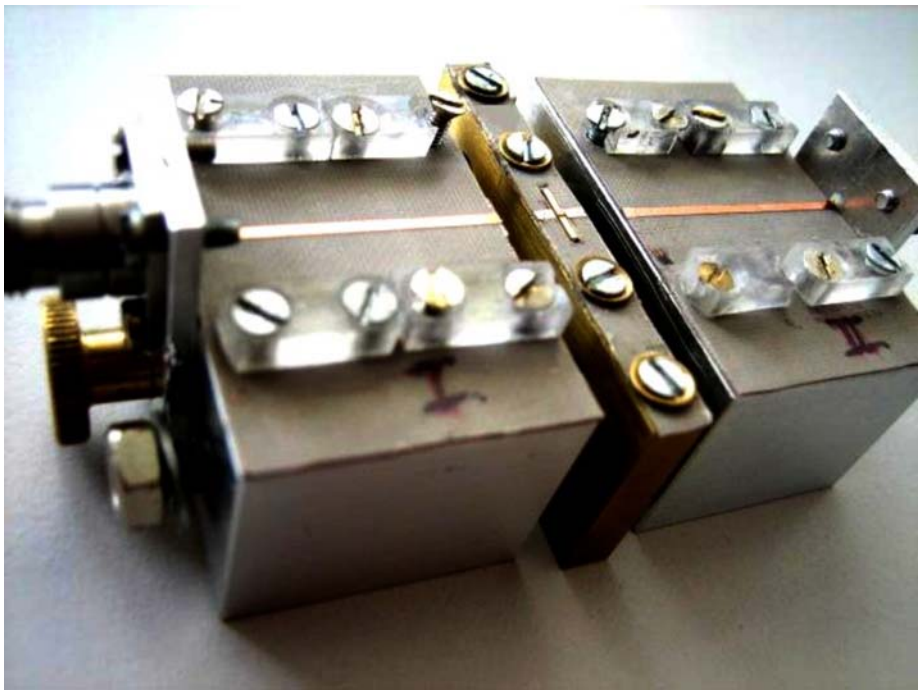


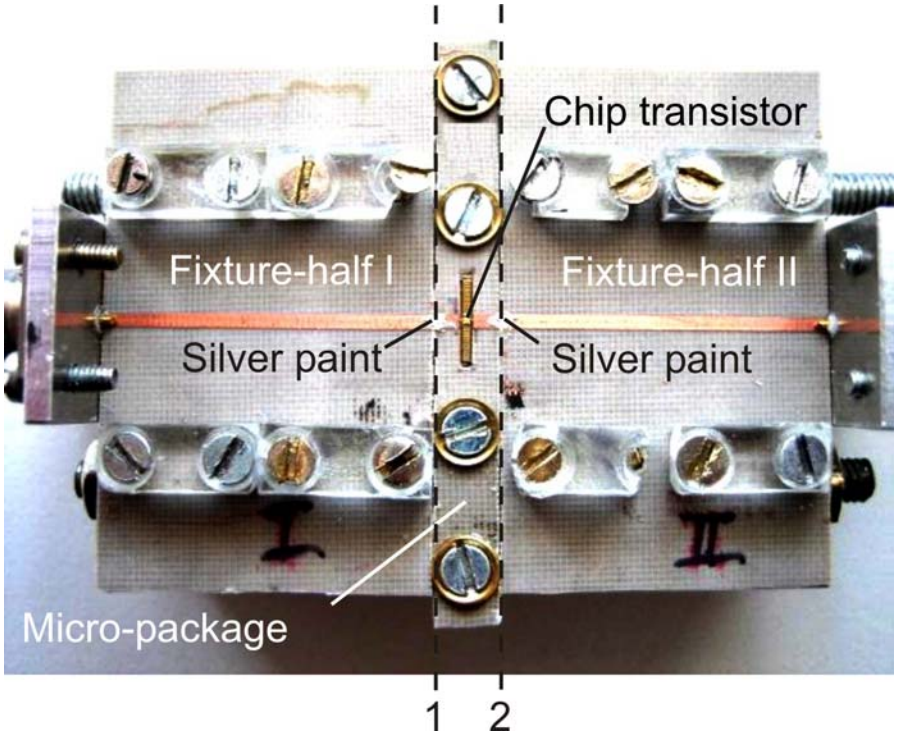
Figure 5.2 Illustration of the mounted transistor on the brass carrier-plate.

Another point to be emphasized is concerning the attachment of the substrate onto the brass carrier. It has been observed in practice that there will be strong gain decrement (around 3-5 dB) if the substrate has a loose contact with the brass plate causing poor ground [105]. Hence, the substrate is attached firstly using the silver painting and then fastened by four screws ensuring perfect grounding for the microstrip lines (length of 2 mm on each side) as can be seen in Figure 5.1. Two large elliptic holes are drilled through the carrier plate for adjusting the height of the carrier (see Figure 5.1), to make it on the same level as the two fixture-halves.

In Figure 5.3(a), two metal bolts are made through the holes for mechanical support. After careful height fine adjustment, a mechanically stable test environment is achieved by tightening the nuts.



(a)



(b)

Figure 5.3 Measurement fixture configuration for micro-packaged device characterization: (a) before connection, (b) after connection using silver paint.

After that, the interconnection of the micro-package and the test-fixture is done using sliver painting. Attention must be addressed for painting the silver (as discussed in section 2.2.4) on the microstrip line with 1.05 mm width to achieve interconnection. The painting procedure is recommended under the microscope observation. The mount and the concentration of the silver paint are key factors to be controlled to avoid any short circuit. Also, the silver-painted area should not flow outside the copper trace of the microstrip line (see Figure 2.12). After the whole procedure being done, it should be kept at least 30 minutes at the room temperature for drying. Incompletely dried silver interconnection will lead to unstable performance during the measurement, which has been observed by own experiments.

5.1.1 Small-Signal Performance

Now, small-signal S-parameter characterization will be performed for the micro-packaged device using the two fixture-halves shown in Figure 5.3 (with measurement reference planes 1 and 2). The fixture will be calibrated following the THLR in-fixture calibration method (see Appendix A) over the frequency range 0.1- 6.0 GHz.

As illustrated in Figure 5.1(b), the constructed micro-package is composed of chip device, epoxy mounting, microstrip line, and silver paint. Each sub-part has been investigated in detail in the previous chapters. Thus, the topology of the complete micro-package is built up by incorporating these sub-part model delivered before, as shown in Figure 5.4.

Concerning the bonding wires, the length can be roughly estimated from microscope observation. Based on this, the initial parasitic inductance value has been assumed to be 0.4 nH for each wire. Also the parasitic capacitance caused by wire bonding is assumed to be 40 fF [49]. The model parameters of bonding wire and epoxy mounting will be optimized to obtain minimum disagreement between measured and simulated S-parameter over the entire frequency range. Experience has shown that the parasitic effects from the epoxy mounting have a dominant influence. Thus, its parasitic inductance and resistance need to be carefully set first. Bonding wire parasitic effects can, then, become a fine tuning candidate [106-107]. The final equivalent circuit of the

micro-package is given in Figure 5.5. The simulation and measurement comparison is displayed in Figure 5.6. At bias point V_{GS0} = -2.1V, and V_{DS0} = 9V, good agreement is achieved for all S-parameters, confirming the model validity for predicting the small-signal performance. Since the in-fixture calibration has less accuracy approaching 6 GHz, due to the change of load type (from chip resistor to sliding load, refer to Appendix A, Figure A.3), less agreement can, thus, be seen for S11 and S22 at frequencies approaching 6 GHz.

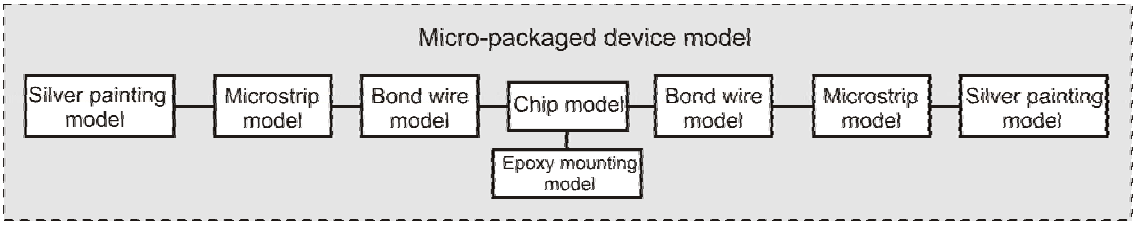


Figure 5.4 Topology of the equivalent circuit of the micro-packaged device model.

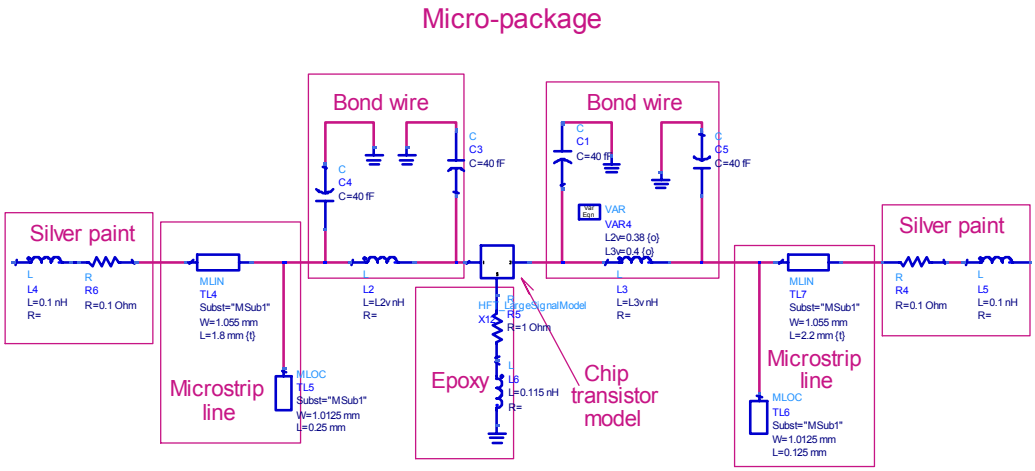
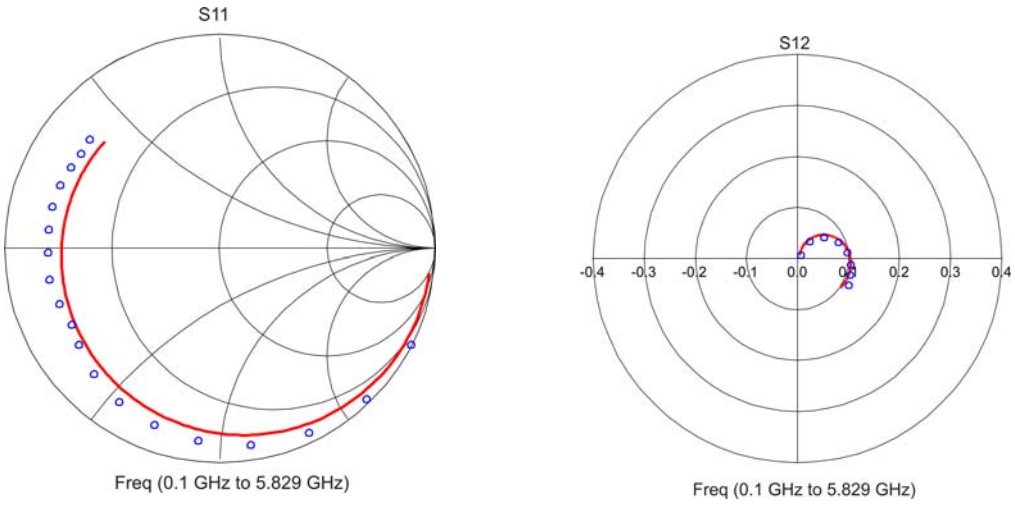
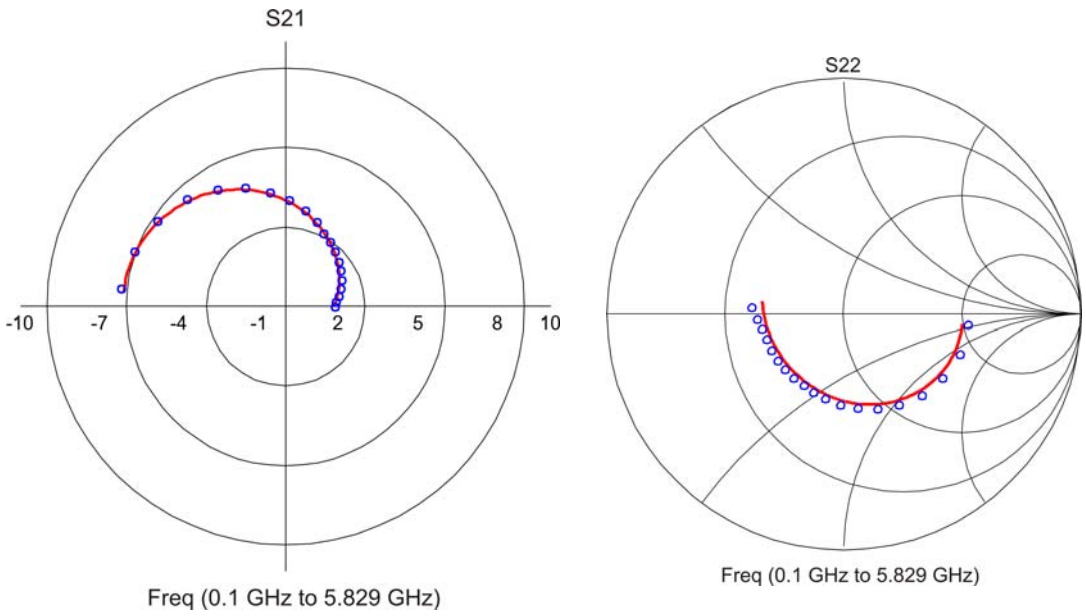


Figure 5.5 Equivalent circuit of the micro-package including the active device.



Radius: 1 Radius: 0.4



Radius: 10 Radius: 1

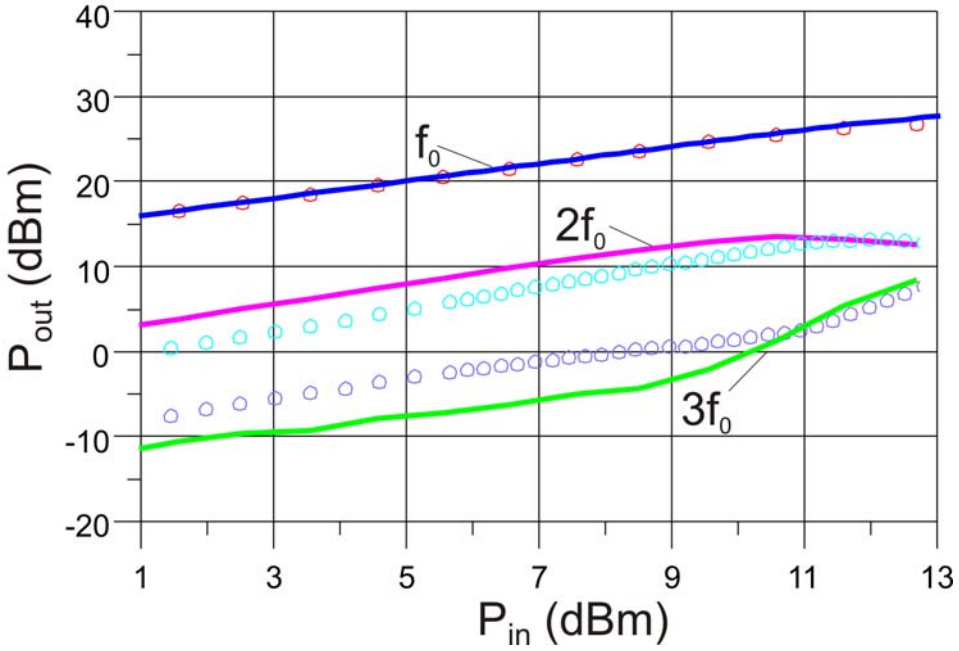
Figure 5.6 Comparison of S-parameter measurement (symbols) and simulation (line) (at V_{GS0} = -2.1V, V_{DS0} = 9V)

5.1.2 Large-Signal Performance

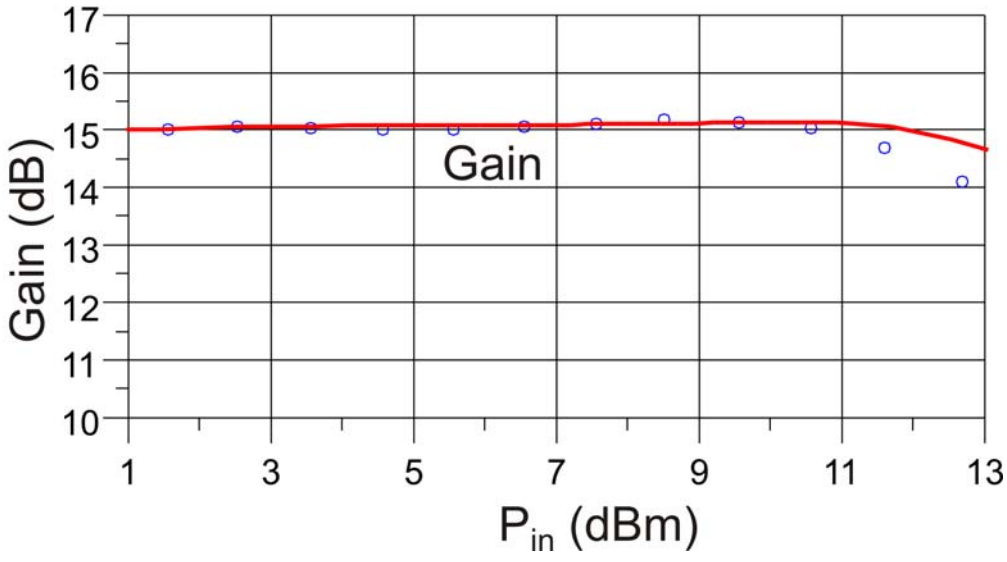
In order to evaluate and confirm the large-signal performance (in terms of output power, efficiency and gain) of the micro-packaged device, single-tone stimulus will be used. The adopted time domain measurement set-up is reported in [99]. Using this set up, one is able to perform the in-fixture calibration (see Figure 5.3(b), reference plane 1 and 2), by using the S-parameters of the two fixture-halves obtained. Both input and output power at the fundamental and higher order harmonic frequencies can be obtained accurately using the signal waveform measurement.

Simulated and measured results of the single-tone power sweep have been compared in Figure 5.7. It can be seen that good agreement between simulated and measured RF large-signal performance of the micro-packaged device has been obtained. Figure 5.7(a) shows very good match for fundamental output power. Good fitting for both second and third harmonics is achieved at higher power range (input above 9 dBm), although less agreement is obtained at lower power range. The simulation can well predict the trend of the harmonic output power. Figure 5.7(b) also shows the good prediction of the gain compression

phenomena, at 13 dBm of input power. In Figure 5.7(c), the difference of PAE between simulation and measurement at the high power range is due to the limitation of the large-signal model of the chip transistor for predicting the DC current. Nevertheless, a very reliable unit to start designing the periphery sub-part circuits such as bias networks is confirmed.



(a)



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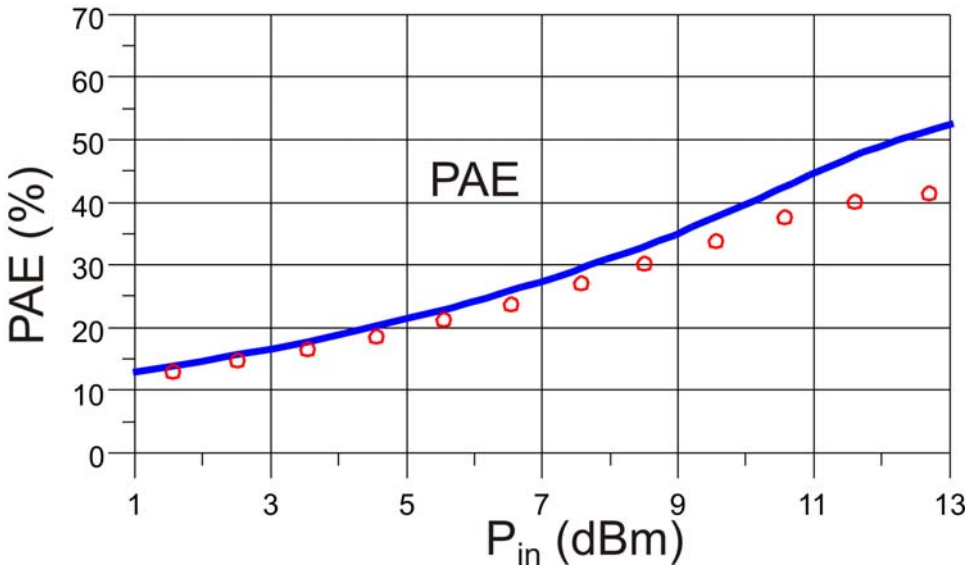


(c)

Figure 5.7 Single-tone power sweep measurement and simulation of the micro-packaged device (at V_{DS0} = 9V, V_{GS0} = -2.1V). (a) Simulated (lines) and measured (symbols) output power at the fundamental, second and third harmonics, and (b) simulated (lines) and measured (symbols) gain, (c) simulated (lines) and measured (symbols) PAE.

5.2 Bias Network Design

5.2.1 Drain Bias Network

Drain bias network should have frequently two functions. The main role is to provide proper DC bias to the active device with minimum disturbing the RF signal path. However, there is another function, which becomes more and more important for broadband wireless communication. The bias network should provide low impedance for baseband signal (video frequency) with wider bandwidth (for instance, UMTS with 5 MHz and LTE with 20 MHz). It has been reported in several publications that ideal short termination at base band is a key factor for improving linearity performance at the circuit level [108-111]. Also, the electrical memory effect can be greatly reduced, which thus enables the digital predistortion technique effectively enhancing the power amplifier linearity,

and finally the linearity performance demanded by advanced wireless communication schemes can be satisfied on system level [110].

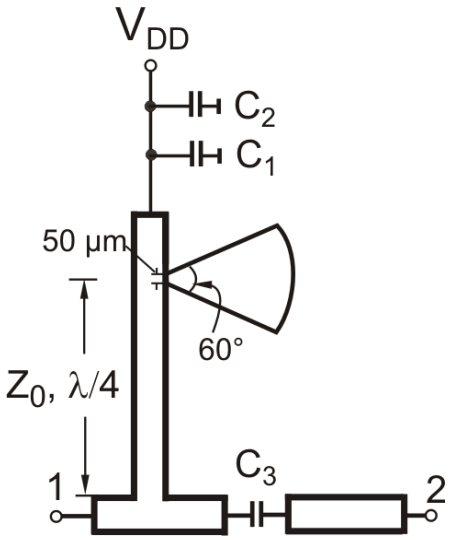


Figure 5.8 Schematic of the proposed drain radial stub bias network.

In this design, a quarter wave line has been adopted due to its simplicity. In addition, an open radial stub is used to provide a short circuit at the exactly desired position, which corresponds to the RF operating center frequency (2.14 GHz). This is difficult to achieve by using chip-type RF bypass capacitor, since it is hard to exactly place and solder it at the desired position in practice owing to the handling limitation. By incorporating the radial stub, the RF operating frequency shift can be overcome significantly. The radial stub design formula is given in [112] and designed using the model provided by ADS®. As shown in Figure 5.8, the C_1 and C_2 chip capacitors (10 µF and 1 µF) are selected to provide extremely low impedance in the frequency range from DC to 5 MHz. Their models have been verified in Chapter 3 against measurement results. By resonating at its series resonant frequency, the impedance in the order of several mΩ is obtained by each capacitor. Although the total topology is not as complicated as reported in [111], it has shown a promising function to achieve the desired goal [113]. The positioning of these DC decoupling capacitors is not as critical as for RF decoupling. So, this eases the fabrication procedures. It has to be pointed out that these two capacitors also have the function of removing the parasitic effects from the DC power supply along with the feeding cables (inductance) [113].

In Figure 5.8, C3 is the DC blocking capacitor. Its value is 22 pF and it has a series resonant frequency approximately at 2 GHz (refer to section 3.2). Its model has also been validated in Chapter 3. To include DC blocking within the bias network is to facilitate the active package part characterization using the designed bias network. Otherwise, additional DC blocking capacitor or commercial bias tee has to be used to characterize the micro-packaged device.

The final fabricated drain bias network is shown in Figure 5.9. It is connected with the in-fixture measurement set up by using the silver painting as before.

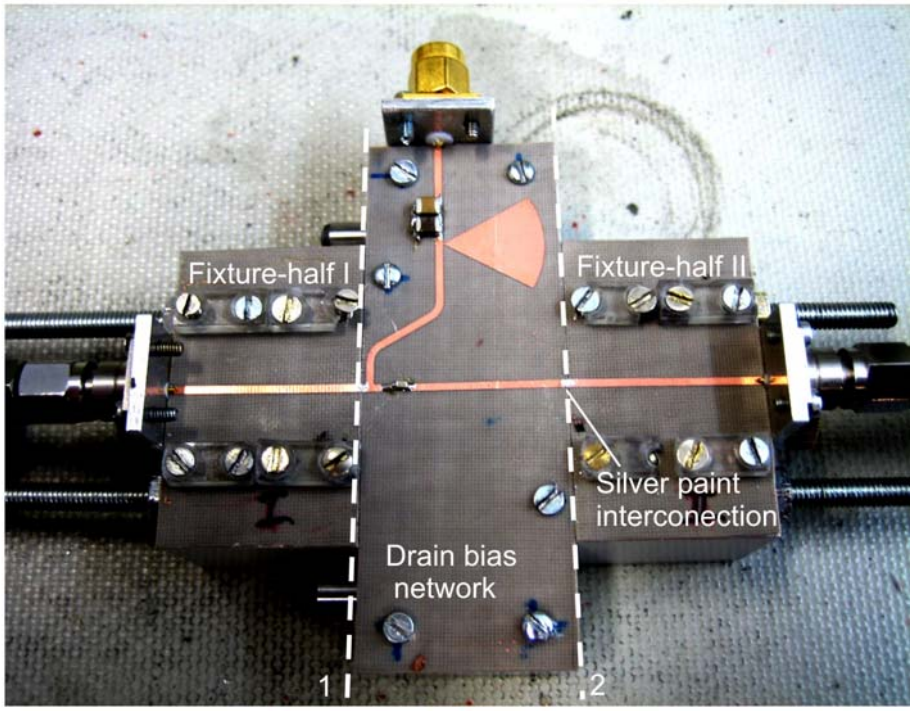


Figure 5.9 In-fixture measurement set up of the fabricated drain bias network.

Comparison of the measured and simulated S-parameters of the drain bias network is given in Figure 5.10. It can be seen that good fitting is achieved over the entire frequency range including the fundamental and second harmonic frequency.

Next, the performance of the fabricated drain bias network at the baseband is analysed using Anritsu® Vector Star VNA (70 kHz to 70 GHz). Measurement is compared with simulation in Figure 5.11 [82]. It can be seen, excellent agreement is obtained within the measurement frequency up to 100 MHz. The resistance part is very low (approximately 0.5Ω) during the whole frequency

range. More important, the reactive part is well suppressed below 1Ω up to 20 MHz due to the adoption of the baseband capacitors.

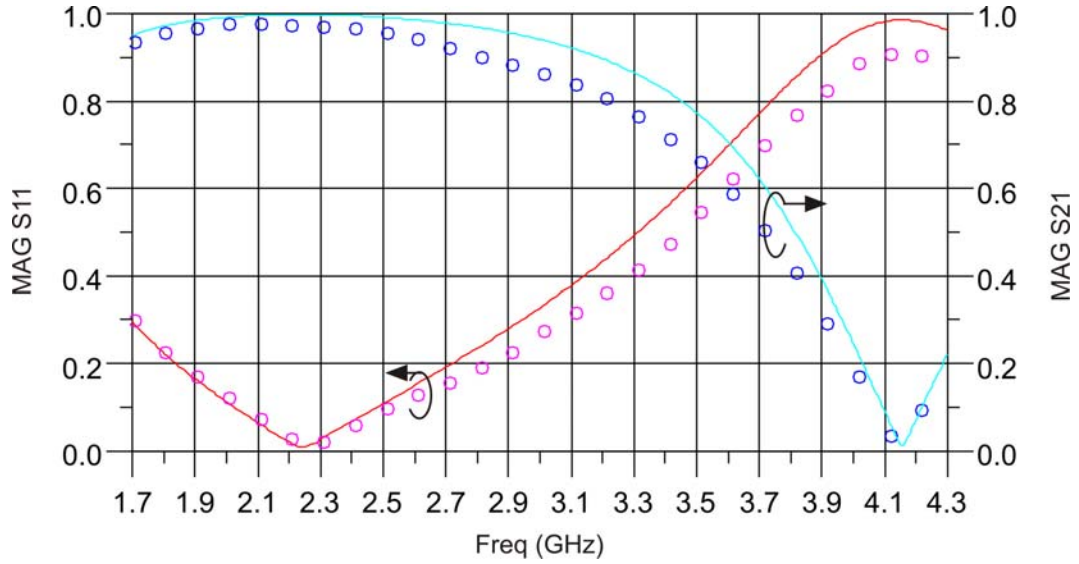
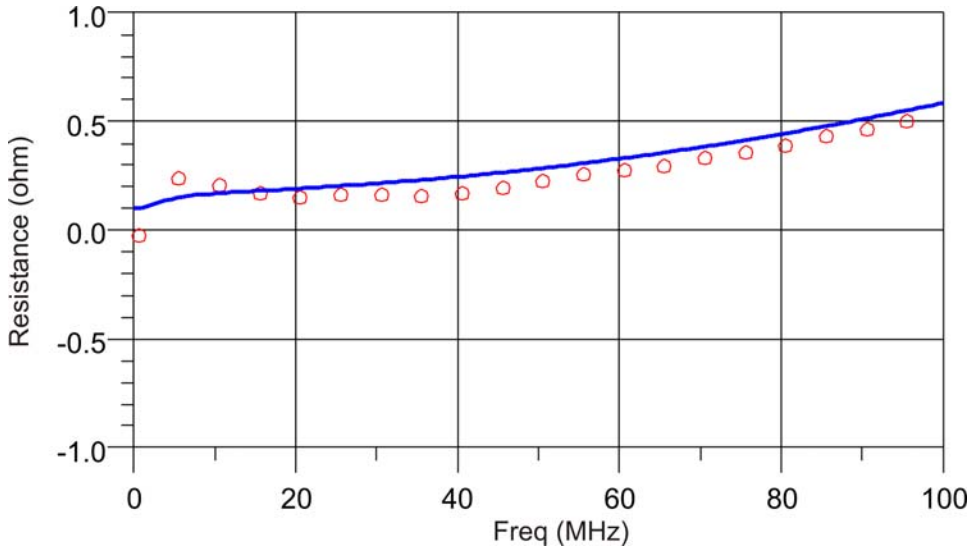
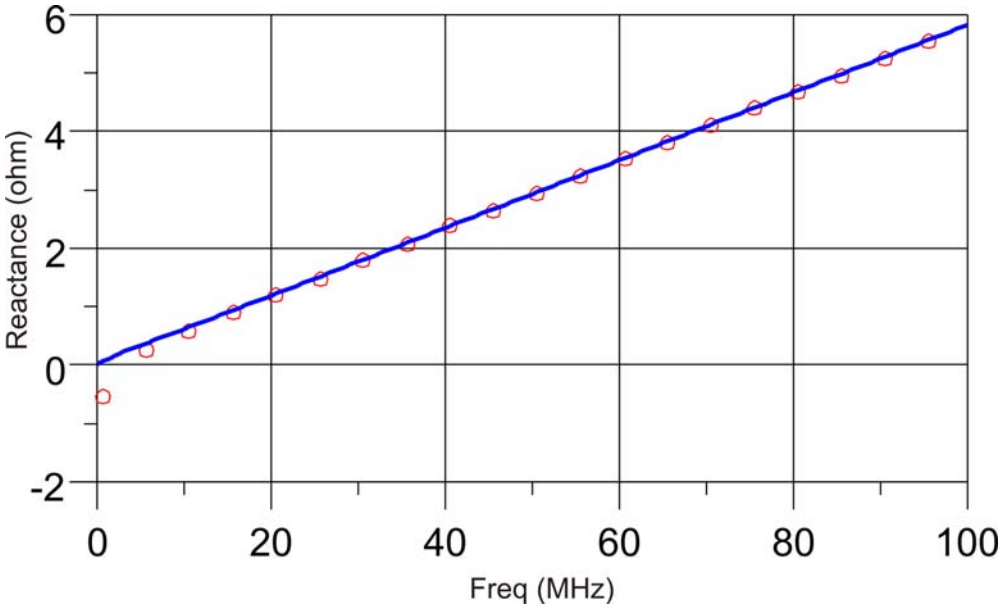


Figure 5.10 Measured (symbols) and simulated (solid lines) S-parameter of the designed drain bias network.

This confirms the designed drain bias network sub-part works very well at the desired fundamental frequency, second harmonic frequency, and also baseband frequency. In all these frequency zones, very good agreement between simulation and measurement results has been achieved.



(a)



(b)

Figure 5.11 Comparison of the drain bias network base band impedance from simulation (solid lines) and measurement (symbols): (a) resistance and (b) reactance.

5.2.2 Gate Bias Network

The design of gate bias network is normally complicated compared to the drain bias network design, since it usually has to contain the stabilization circuit as well. For power amplifier operation, it is highly desirable to make it unconditionally stable. However, the active device manufactured by the semiconductor foundry frequently does not fulfil the unconditionally stable operating conditions. Thus, it becomes very often to consider the stabilization network design while designing gate bias network, since output side will put a strict limitation of the power requirement, which significantly increases the stabilization network design difficulty [114-115].

In Figure 5.12, investigation of the stability factor (K factor) of the micro-packaged device (see Figure 5.4) is done both in simulation and measurement (on the basis of the THLR S-parameter measurement data). Good agreement between simulation and measurement is shown, which again verifies the model capability for predicting S-parameter from this important application point of view. As can be seen, K factor of the micro-packaged device is below unit in the

frequency range 0.1 GHz to 6 GHz. It shows the mandates to include the stabilization part in this specific case.

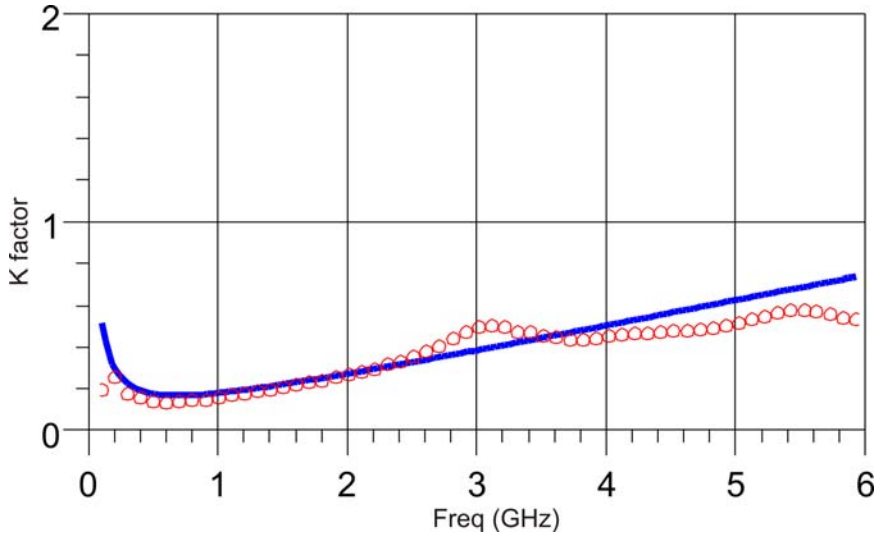


Figure 5.12 Comparison of K factor of the micro-packaged device between simulation (solid lines) and measurement (symbols).

There are various schemes to realize the stabilization part, as explained in [114-115]. The main design concern is to increase the K factor over the whole frequency band (from several MHz up to 3rd harmonic), at the same time not to lose much power gain at the RF operating frequency.

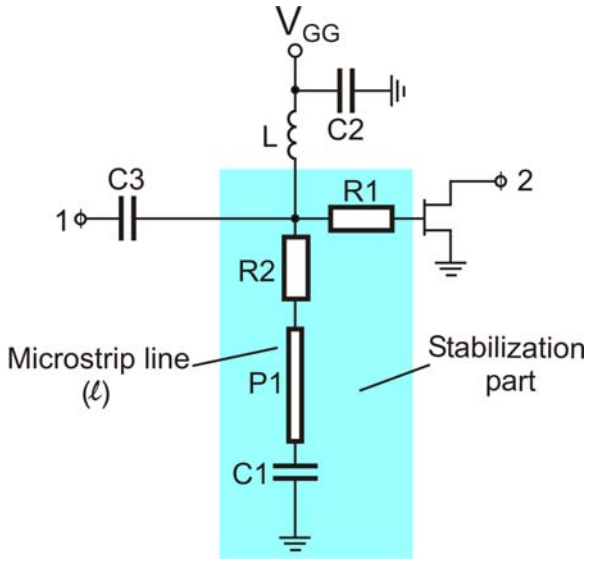


Figure 5.13 Gate bias network topology including the stabilization network.

The stabilization network topology proposed in [126] is adopted, as shown by the shadowed area in Figure 5.13. The distinctive advantages of this stabilization network is that it can make the transistor stable in the frequency range higher than the RF operating center frequency (in this case, 2.14 GHz) using resistor R1 and also stable at the frequency range lower than the RF operating center frequency using R2 and micostrip line P1. Thus, it is possible to stabilize the amplification circuit within a very wide frequency band covering both above and below RF operating center frequency bands. Furthermore, the degree of gain reduction in the RF operating frequency can be made much lower than using the conventional stabilization circuit [116]. L1 is a lumped surface mounted chip inductor, providing high impedance for RF signals compared to the input impedance of the active device. C1 is used to separate the DC bias voltage. C2 is mainly for decoupling the baseband signal and the noise from the power supply. C3 is the DC blocking capacitor as explained before. The next design step is to choose the parameters of the elements in the stabilization network such that the K factor of the stabilized micro-packaged device is just above unit over the entire frequency range and close to unit at the RF operating center frequency. After optimizing the parameter values, the final element values are given in Table 5.1.

Table 5.1 Element values of the gate bias network.

C1 (pF)	C2 (μF)	C3 (pF)	R1 (Ω)	R2 (Ω)	L (nH)	ℓ (mm)
100	10	22	10.3	8.25	68	20.85

The final stability factor of the micro-packaged device after including the designed stabilization network is given in Figure 5.14. It can be seen that K is larger than one up to 6 GHz. It is very close to unit at the operating frequency around 2 GHz, implying minimum gain reduction caused by adding the stabilization network.

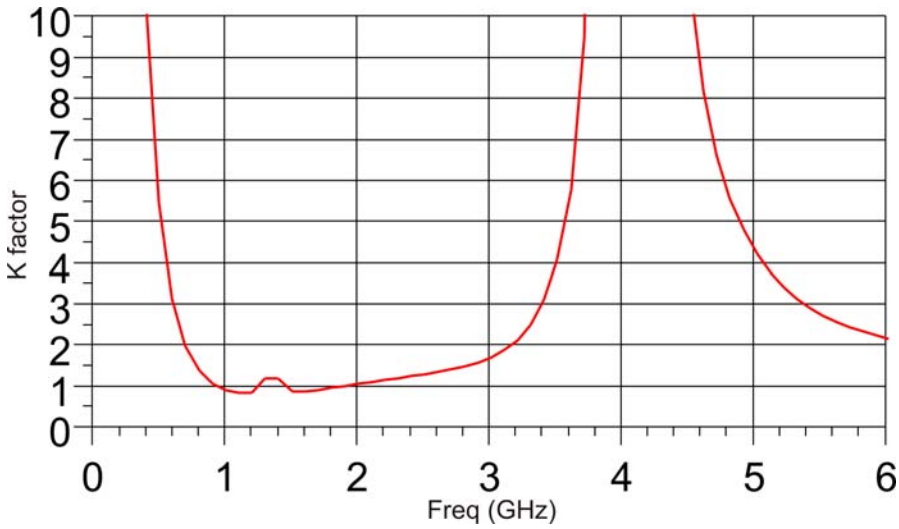


Figure 5.14 Simulation of K factor of the micro-packaged device after including the stabilization network.

The fabricated gate bias network is shown in Figure 5.15. It is characterized using the in-fixture calibrated measurement set up (with measurement plane 1 and 2), as for drain bias network.

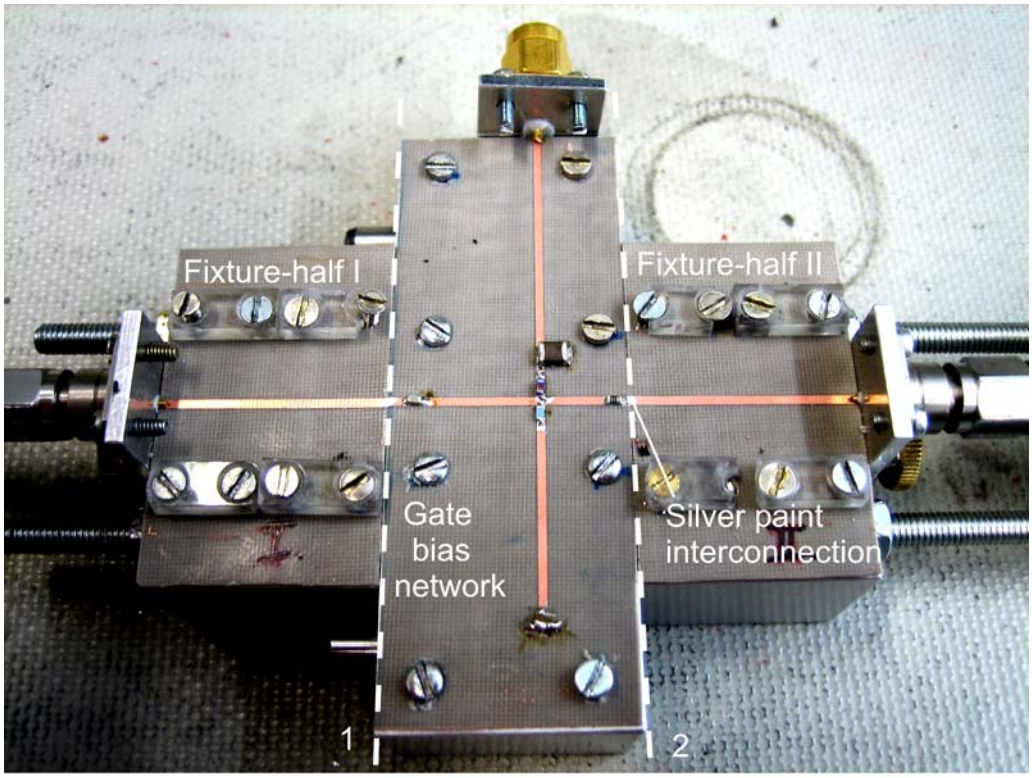


Figure 5.15 In-fixture measurement set up of the fabricated gate bias network.

Figure 5.16 shows the S-parameter results of both simulation and measurement of the designed gate bias network in the frequency range from 1.5 GHz up to 2.7 GHz. Very good agreement is achieved between them over the entire measured frequency range. It can also be seen that gate bias network using lumped inductor has a broader bandwidth compared with the drain bias network, in which quarter wave transmission line is utilized. Also, the fabricated gate bias network has a higher loss due to the resistive elements included.

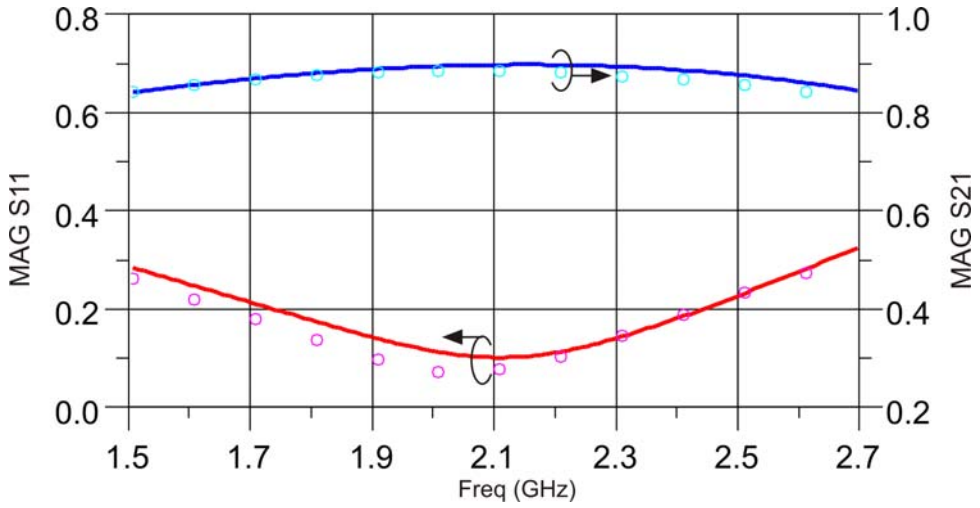


Figure 5.16 Measured (symbols) and simulated (solid lines) S-parameter of the designed gate bias network.

Next, the performance of the micro-packaged device together with the fabricated drain and gate bias network will be characterized and compared with simulation prediction. As shown in the Figure 5.17, these individual parts are interconnected together using silver paint as done before. One should pay attention to the height alignment while assembling them together. Finally, all these parts including the measurement fixtures should be on the same height for achieving good continuity.

First, the S-parameters will be measured using VNA with the in-fixture measurement set up (with reference plane 1 and 2 in Figure 5.17) at the designed bias points (V_{DS0} = 9V and V_{GS0} = -2.1V). The results are reported in Figure 5.18.

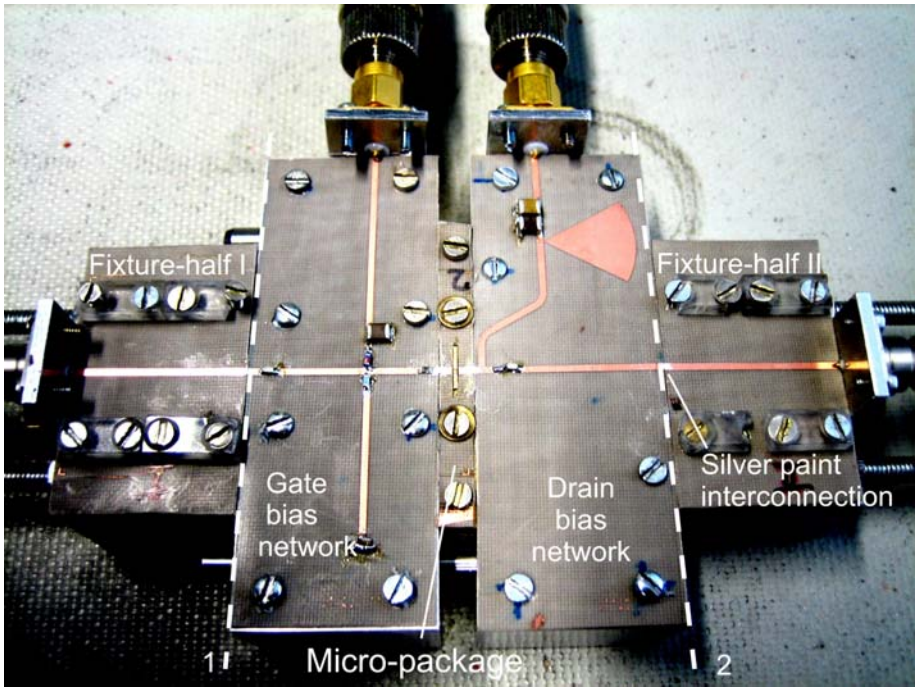
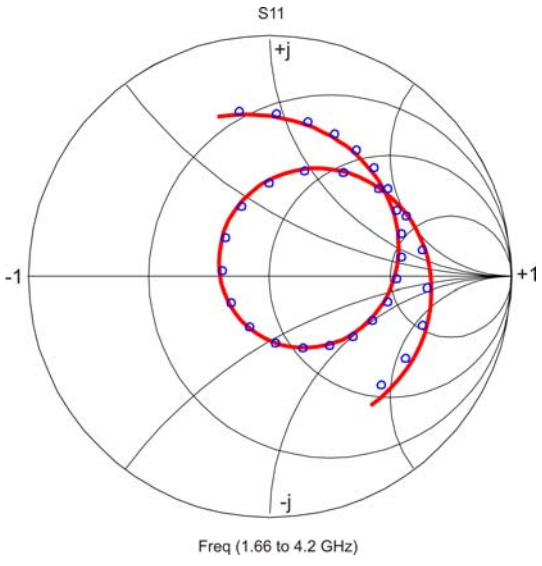
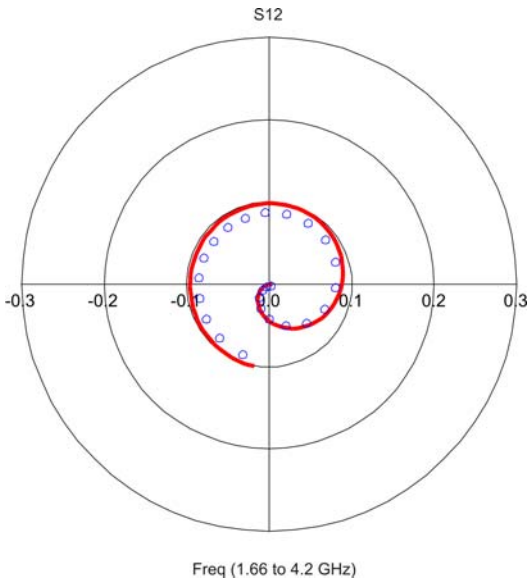


Figure 5.17 Characterization of the micro-packaged device with connected bias networks.

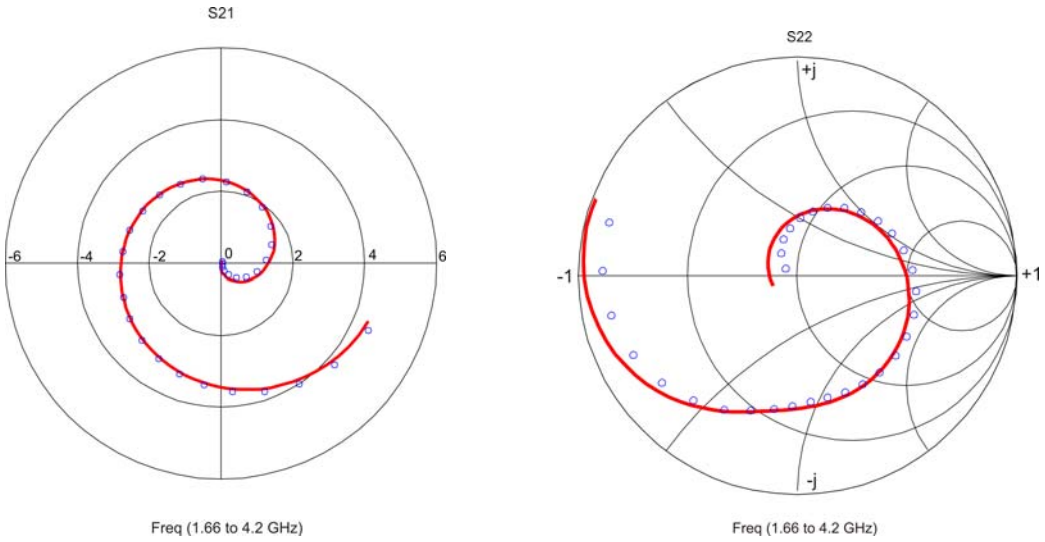
- Small-signal characterization



Radius: 1



Radius: 0.3



Radius: 6 Radius: 1

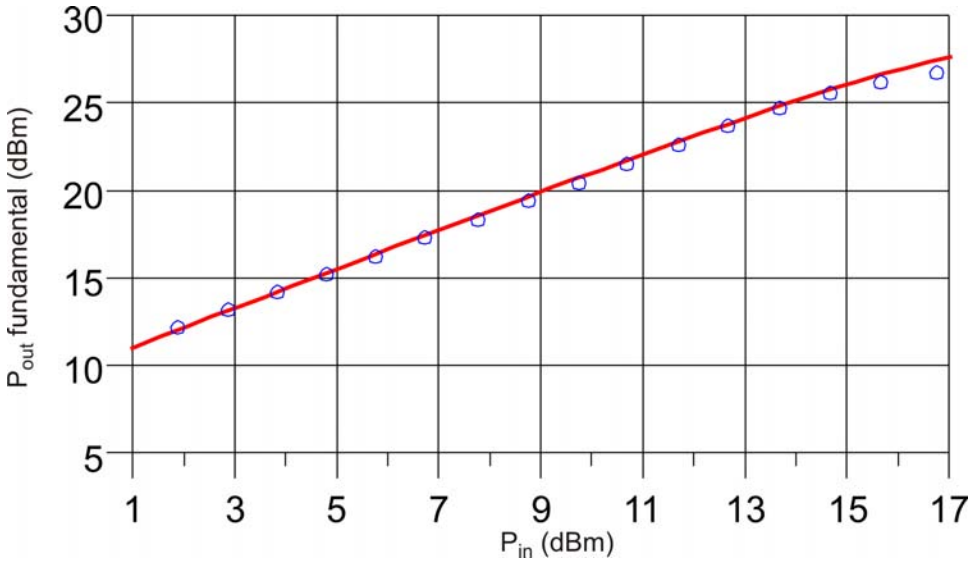
Figure 5.18 S-parameter comparison of the micro-packaged device part biased using fabricated bias networks between simulation (solid lines) and in-fixture measurement symbols) at V_{GS0} = -2.1V and V_{DS0} = 9V.

As can be seen, excellent agreement between simulation and real measurement is obtained over the frequency range 1.66 GHz to 4.2 GHz, including the second harmonics. It validates the small-signal performance of the design till this stage.

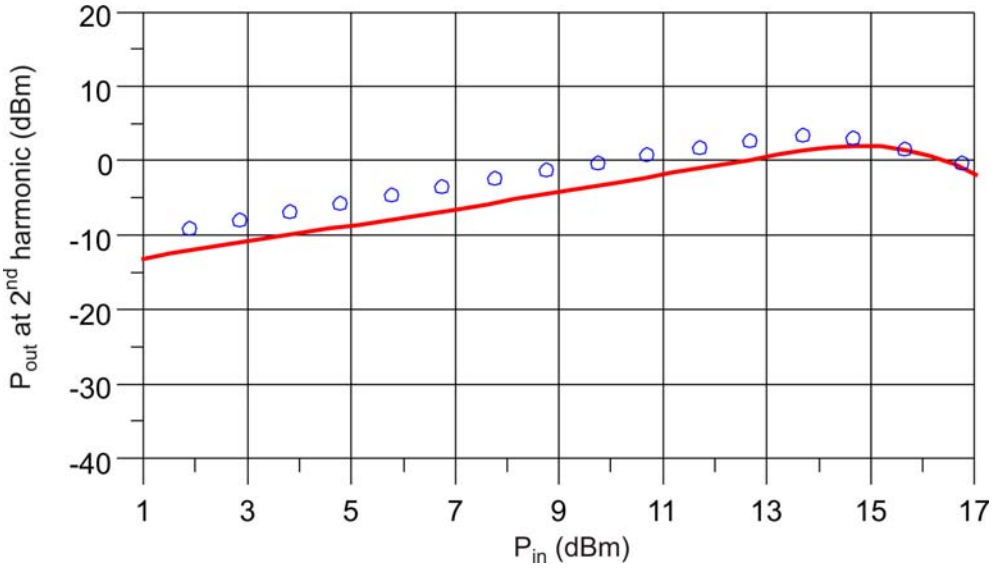
- Large-signal characterization

The single tone power sweep characterization is also performed in order to verify the large-signal performance. As given in Figure 5.19, both output power at fundamental and higher order harmonics are well predicted by simulation. Also, the power added efficiency shows well match with simulation, especially at the average power region, which is critical for power amplifier operating with dynamic power range signal.

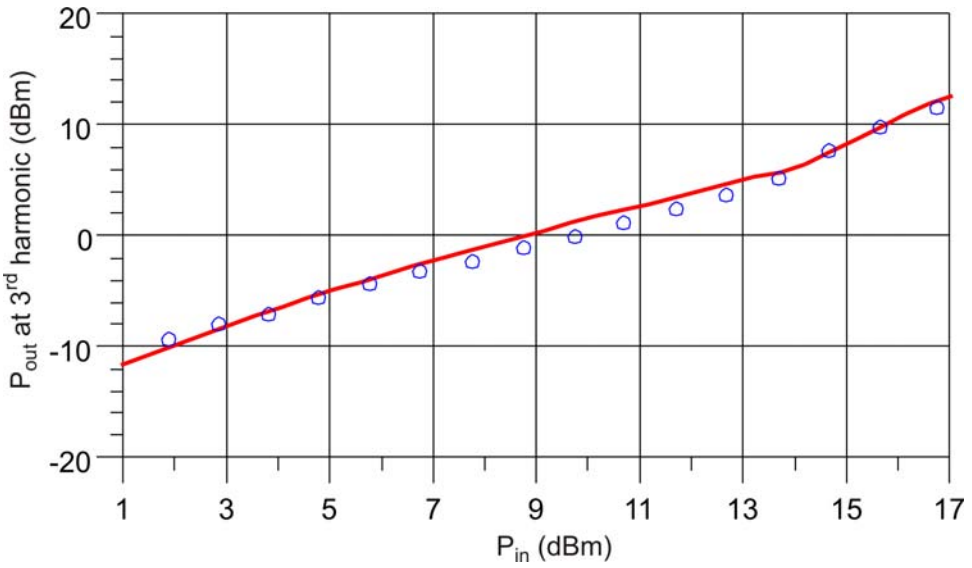
Therefore, the micro-packaged device with the connected drain and gate bias networks has been successfully verified in terms of both small-signal and large-signal operation. It sets solid starting points for continuing design assignment with matching networks.


30
25
20
15
10
5
1
3
5
7
9
11
13
15
17
P_{out} fundamental (dBm)
P_{in} (dBm)

(a)


20
10
0
-10
-20
-30
-40
1
3
5
7
9
11
13
15
17
P_{out} at 2nd harmonic (dBm)
P_{in} (dBm)

(b)


20
10
0
-10
-20
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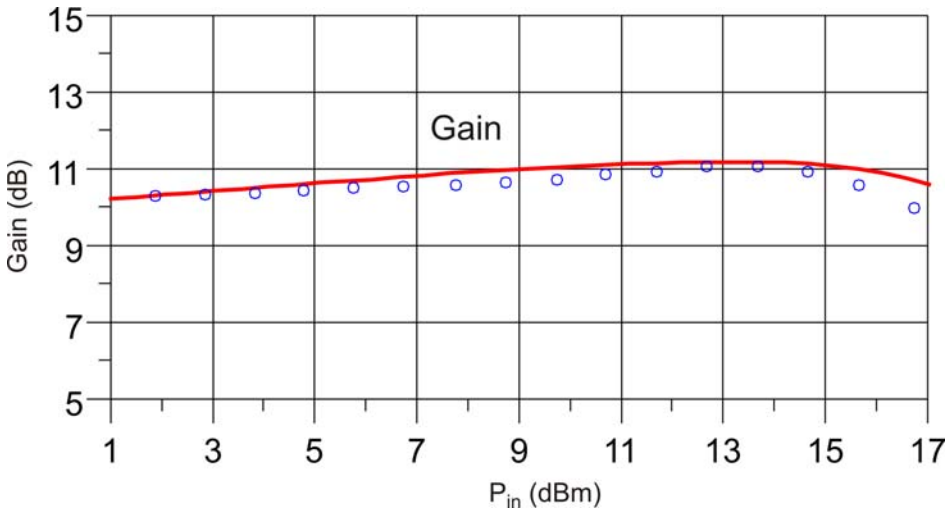
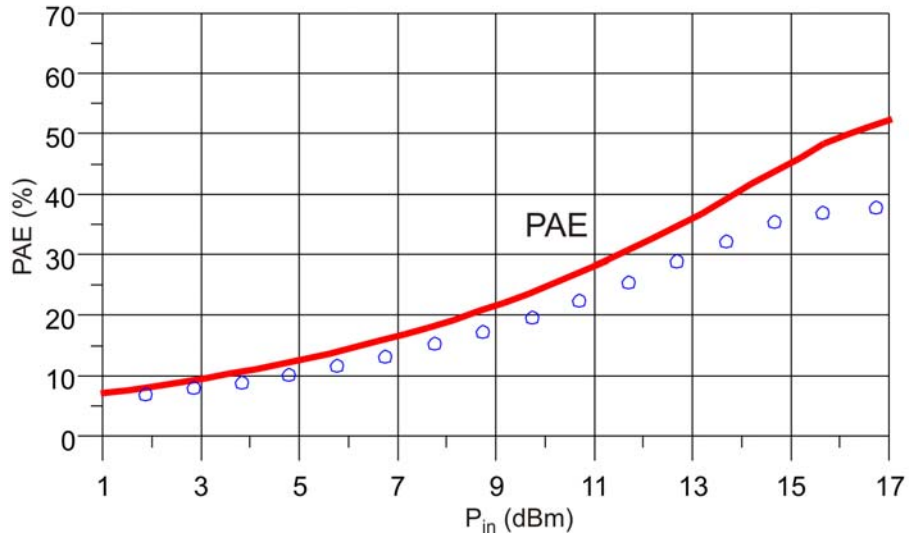
15
17
P_{out} at 3rd harmonic (dBm)
P_{in} (dBm)

(c)



(d)



(e)

Figure 5.19 Single-tone power sweep measurement (symbols) and simulation (solid lines) of the micro-packaged device with fabricated bias networks (biased at V_{GS0}= -2.1V and V_{DS0} = 9V). (a) Output power at fundamental, (b) output power at second harmonic, (c) output power at third harmonic, (d) gain, and (e) power added efficiency.

5.3 Matching Network Design

The function of matching network is to transfer the desired termination values at both input and output side to the normal environmental impedance (usually 50Ω). For power amplifier input matching, the design target is to achieve complex conjugate match with the input impedance [115]. Then, the minimum

power reflection is obtained at the input side. For the output matching, the active device is expected to be loaded with various terminations according to the different specific design goals, in terms of output power, efficiency, and linearity. For power amplifier design, the optimum output impedance is normally chosen as a compromise between these specifications. Load-pull is normally performed to select the final proper termination either by simulation or by experiment.

Following parts will explain the input and output matching network design procedures. Finally, the designed matching networks will be fabricated and measured. Comparison will be done with simulation and followed by circuit tuning work, if necessary.

5.3.1 Matching Impedance Determination

Based on the S-parameter measurement results (Γ_{in} and Γ_{out}) performed at the microstrip calibration plane 1 and 2, the input and output impedances of the micro-packaged device (with the bias networks) can be calculated directly, in a 50Ω environment (see Figure 5.20) [115]. For instance, the calculated input impedance from measurement is compared with the one predicted from simulation, as shown in Figure 5.21. Very good agreement is achieved for both real and imaginary part, over the frequency range 1.6 GHz up to 4.4 GHz, which again validates the successful prediction concerning the small-signal performance by simulation.

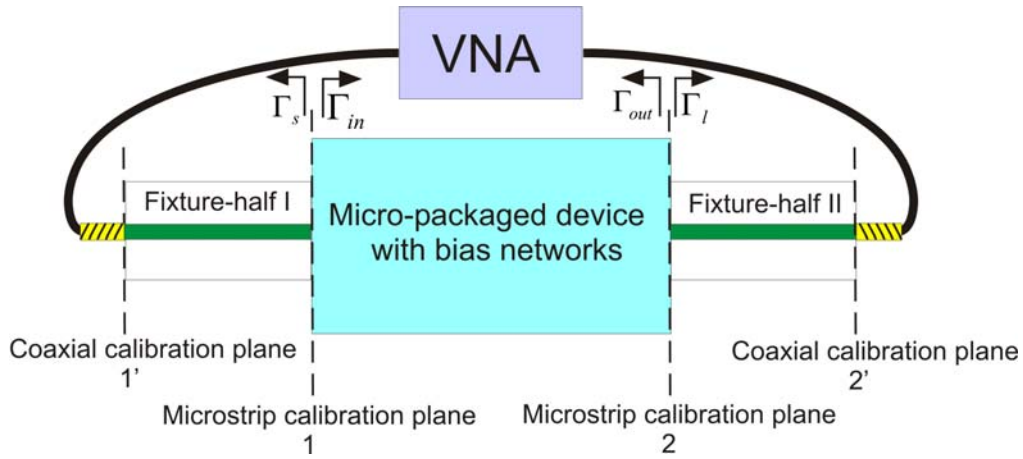


Figure 5.20 Schematic of the in-fixture measurement of the micro-packaged device with the designed bias networks.

Then, the optimum output load (Z_{load}) at the reference plane 2 is determined by load-pull simulation in this work. Figure 5.22 shows the load contours for output power and power added efficiency, when the signal source is terminated with the complex conjugate input impedance determined (see Figure 5.21, $Z_s = Z_{in}^* = (75.94 - j87.77)\Omega$ at 2.14 GHz). Based on the compromise made between output power and efficiency, the output load is determined to be $Z_{load} = (28.47 – j19.70)\Omega$, at the input power of 16 dBm.

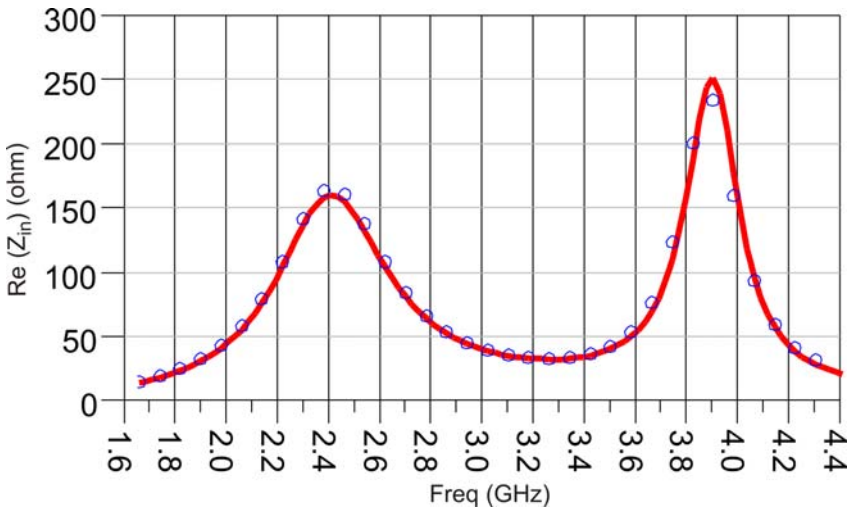
However, one should notice that the transistor is not really unilateral in practice, which means that the input impedance will be affected with the load condition at the output, and vice versa. Hence, the final input impedance and the optimum load termination should be determined in an iterative manner.

After several iterations, the final input impedance and optimum load termination determined are:

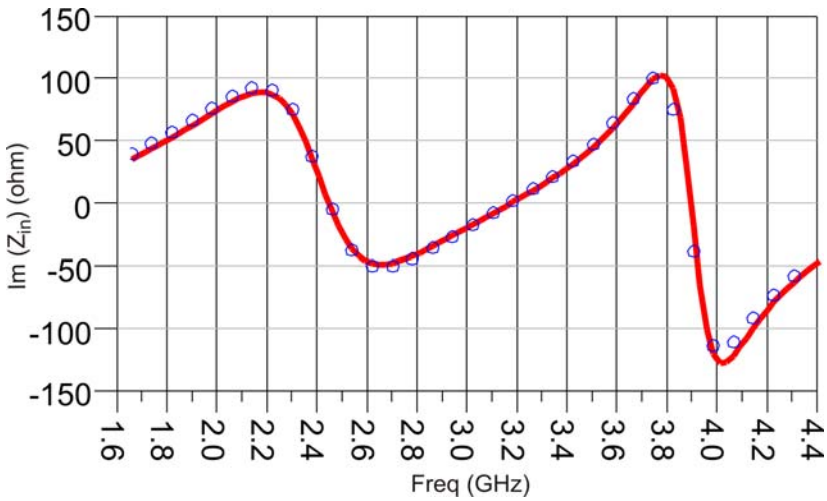
$$Z_{in} = (119.228 + j105.1)\Omega \text{ and}$$

$$Z_{load} = (27.549 – j28.054)\Omega.$$

With the normalization impedance of 50Ω, one can get $z_{in} = Z_{in}/50\Omega = 2.38 + j2.10$, $z_{load} = Z_{load}/50\Omega = 0.55 + j0.56$.



(a)



(b)

Figure 5.21 Comparison of input impedance in 50Ω environment between simulation (solid lines) and measurement (symbols): (a) real part, and (b) imaginary part.

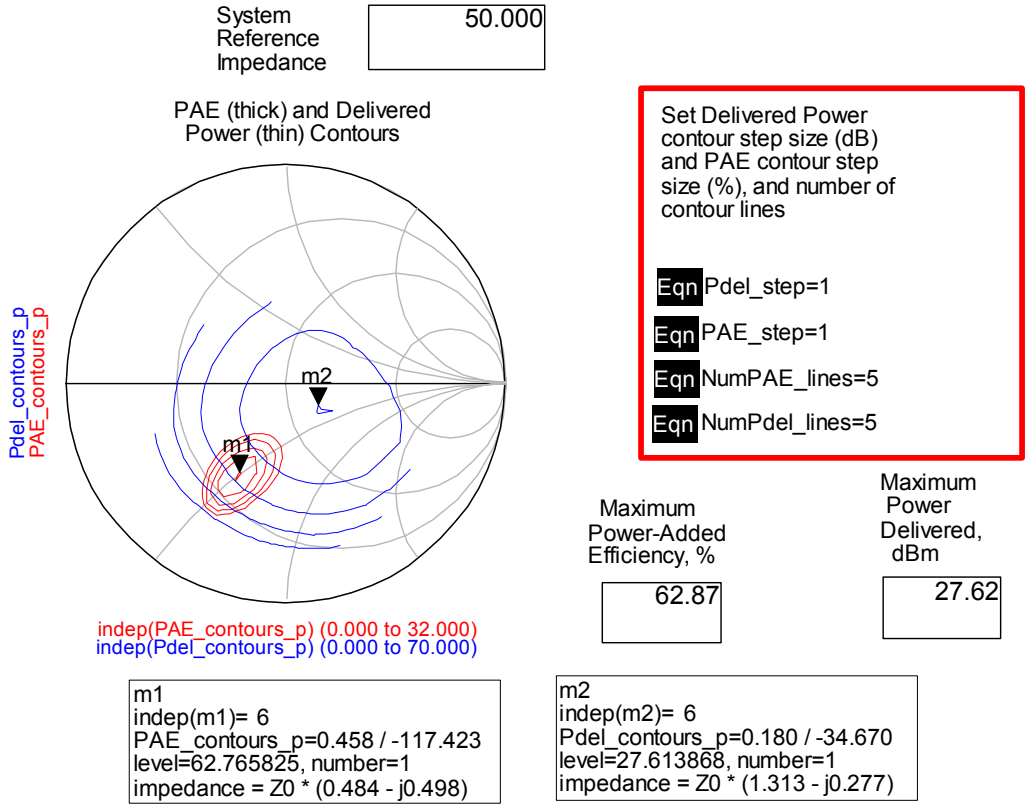


Figure 5.22 Load-pull simulation of the micro-packaged device together with designed bias networks (at bias point V_{GS0} = -2.1V and V_{DS0} = 9V), with input power of 16 dBm.

5.3.2 Matching Network Design

1. Input matching network

The task is to match the Z_{in} to the standard source impedance Z_s (50Ω). The chosen topology is to use distributed form, namely microstrip line, because above 2 GHz lumped elements are better to be avoided in designing matching networks owing to their parasitic effects. Normal L-shape is adopted to construct the matching circuit, as shown in Figure 5.23(a). In this case, the characteristic impedance of the line is 50Ω. The dimension of the transmission lines can be either calculated analytical or graphically. Smith chart is found to be a powerful tool for such kind of design [112]. One can read directly from the Smith chart of the electrical length needed to transform one impedance to another impedance along certain path, either in series or shunt configuration. Detailed design procedure can be found in [117].

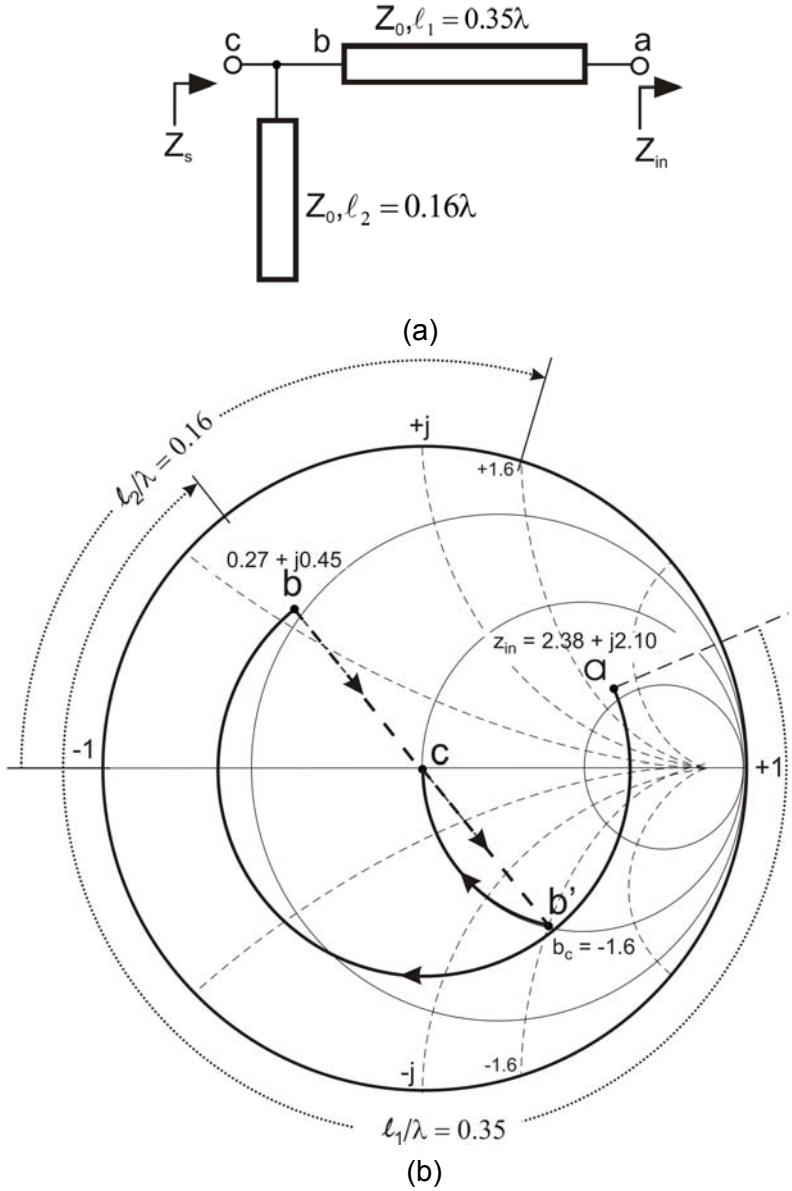


Figure 5.23 Input matching: (a) topology, and (b) design procedure using Smith chart.

Using the CAD software (LLSmith), the electrical length ℓ_1 of the series transmission line L1 (transform impedance at point *a* to point *b*) can be read as 0.35λ. In order to transform point b to the center point c of the Smith chart using a shunt stub, point *b* has to be projected to point *b'* (y=1/z, change from impedance to admittance plane) first. The normalized shunt capacitance (susceptance part) b_c at point *b'* is -1.6. Then the open stub L2 (equivalent to a lumped capacitor of normalized capacitance 1.6) can rotate point *b'* to *c* along the admittance circle. From the rotation the length of ℓ_2 can be determined to be 0.16λ (moving from open toward generator till the expected reactance position). λ is approximately 96.8 mm at the 2.14 GHz operating center frequency. The physical length and the width can then be synthesized using graphical or analytical tools given in [112]. Alternatively, this can be performed using CAD tools available in simulation software (for instance ADS® LinCal tool).

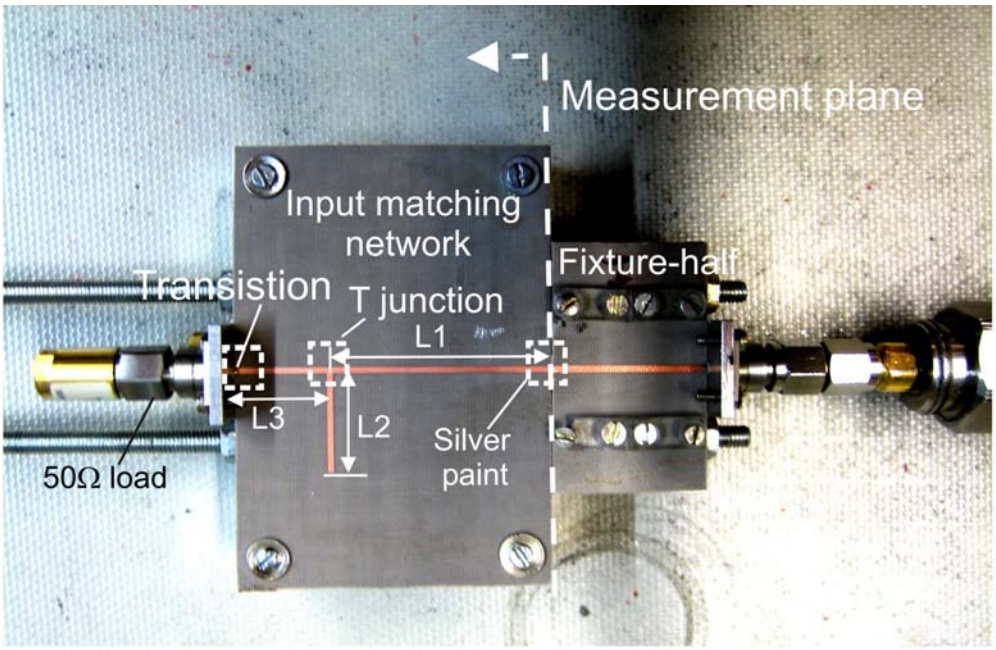


Figure 5.24 Characterization of the fabricated input matching network using the in-fixture measurement set up.

After the design is finished in ADS, the layout can be generated and fabricated using chemical wet-etching technology. As shown in Figure 5.24, the fabricated input matching network is then connected with a half fixture using silver paint to perform the in-fixture characterization. Another port is terminated with a 50Ω standard load mounted on a coaxial launcher. In the design procedure, the

silver painted interconnection parasitic effect is taken into account based on its equivalent mode developed. A T-junction model using Hammerstad model in ADS® is adopted for connecting the three microstrip lines (L1, L2 and L3) [118]. The transition from coaxial-to-microstrip is also analysed separately in this work, to remove any uncertainty. Figure 5.25 shows the measurement set up, in which the measurement plane is denoted, at the end of the fixture-half (actually, only one of the calibrated two fixture-halves using THLR in-fixture calibration method is taken).

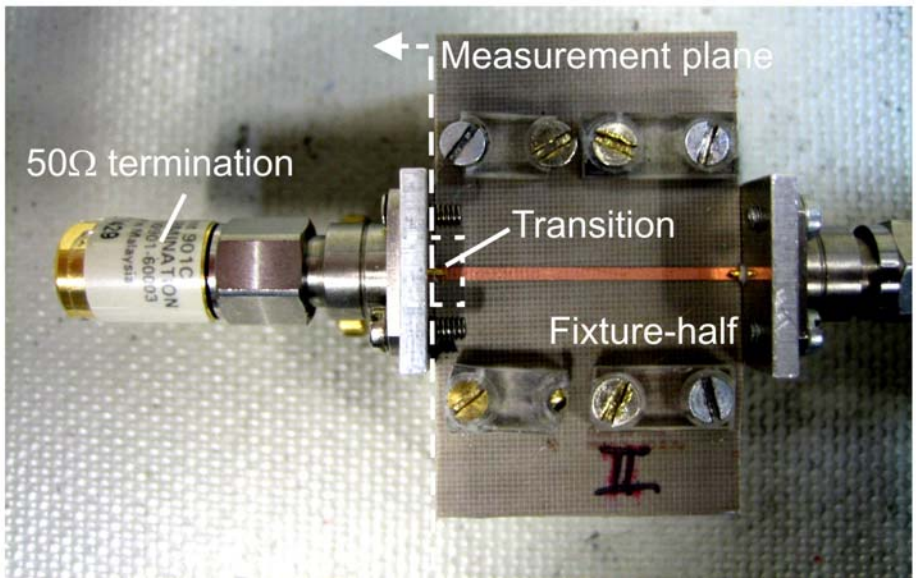
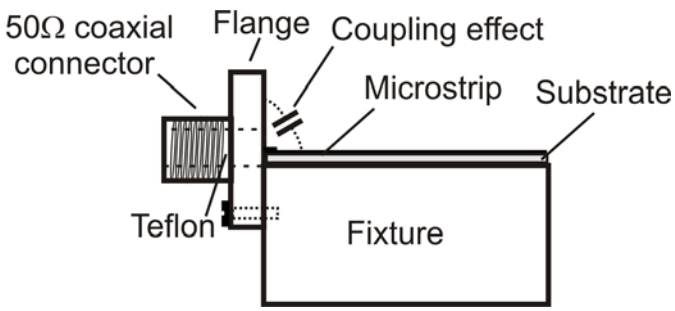
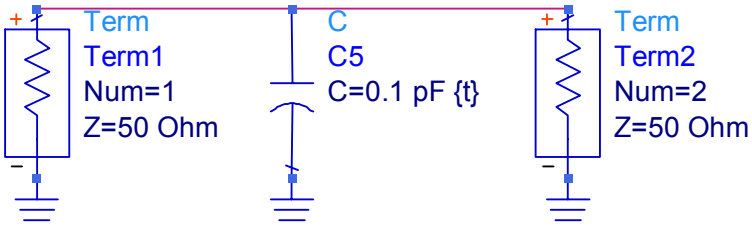


Figure 5.25 Characterization of the coaxial-to-microstrip transition**.**

A shunted capacitor is used to model the coupling effects between the microstrip line and the flange (as ground) [112]. The coaxial-to-microstrip transition effect can be modelled using a shunted capacitor, to a first-order approximation, as shown in Figure 5.26 [119].



(a)



(b)

Figure 5.26 Coaxial-to-microstrip transition effect: (a) illustration, and (b) modeling.

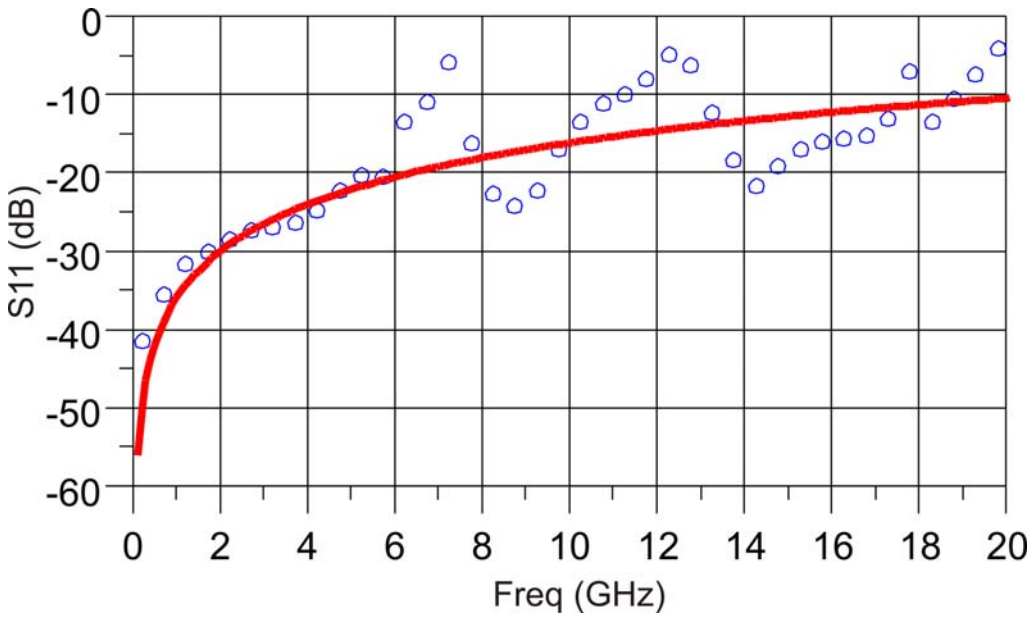


Figure 5.27 Simulation (solid line) and measurement (symbols) of the return loss of the microstrip-to-coaxial transition.

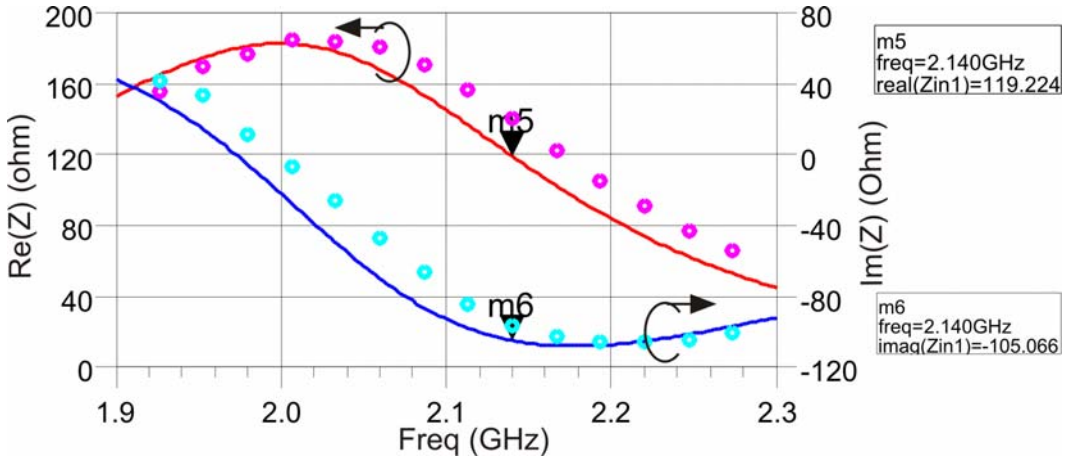


Figure 5.28 Simulated (solid lines) and measured (symbols) of the transformed impedance using the designed input matching network.

The capacitor for modeling the coupling effect has been taken with 0.1 pF [119], and the fitting with measurement (see Figure 5.25) is shown in Figure 5.27. Very good match is obtained up to 6 GHz. It shows that the transition effect at 2 GHz is negligible (return loss approximately –30 dB).

The simulated and measured transformed impedances using the designed input matching network are compared in Figure 5.28. The simulation results show that designed network can successfully transform the 50Ω impedance to the target one. At 2.14 GHz, the simulated value of Z_s is (119.2 – j 105.0)Ω (marker 5 and 6), which is very close to the targeted impedance Z_s = (119.228 – j105.1)Ω. However, the measured true transformed impedance shows some discrepancy. It shows approximately 20Ω and 8Ω difference with respect to simulation results for both the real and imaginary part.

It is assumed that the main reason causing the discrepancy is due to the limited model accuracy of the open-end effect and T-junction used in the ADS® software (models referred to [118]). The reason for larger discrepancy for the real part is that the real part of the impedances near point *a* (see Figure 5.24, this region has a high resistance above 100Ω) is more sensitively affected than that of the reactive part by even a small change (in the order of 1 mm) of the lengths of the microstrip lines (strongly influenced by L1 and partly by L2).

Thus, one has to tune the design parameters in the simulation first to fit the measurement results, in order to find the dominating design factors. What has been found is that with the modification of the lengths L1 ($\Delta\ell_1$ = - 0.49 mm) and L2 ($\Delta\ell_2$ = - 0.2 mm), perfect fitting with the initial measured results can be obtained, as seen in Figure 5.29.

Because it is very difficult to perform the post-fabrication tuning on the circuit to change the dimensions in this case, modified circuit is realized considering the length changes. It means in the layout generation, one has to purposely enlarge dimension according to the length difference given above.

Taking into account the modification of the length of the microstrip line concluded above, a second design of the input matching network is performed. With this new design, good result has been achieved, as shown in Figure 5.30.

It can be seen that the desired impedance can be provided by the fabricated input matching network at the design frequency. Also, good agreement between simulation and measurement has been obtained over the frequency range from 1.9 GHz up to 2.3 GHz.

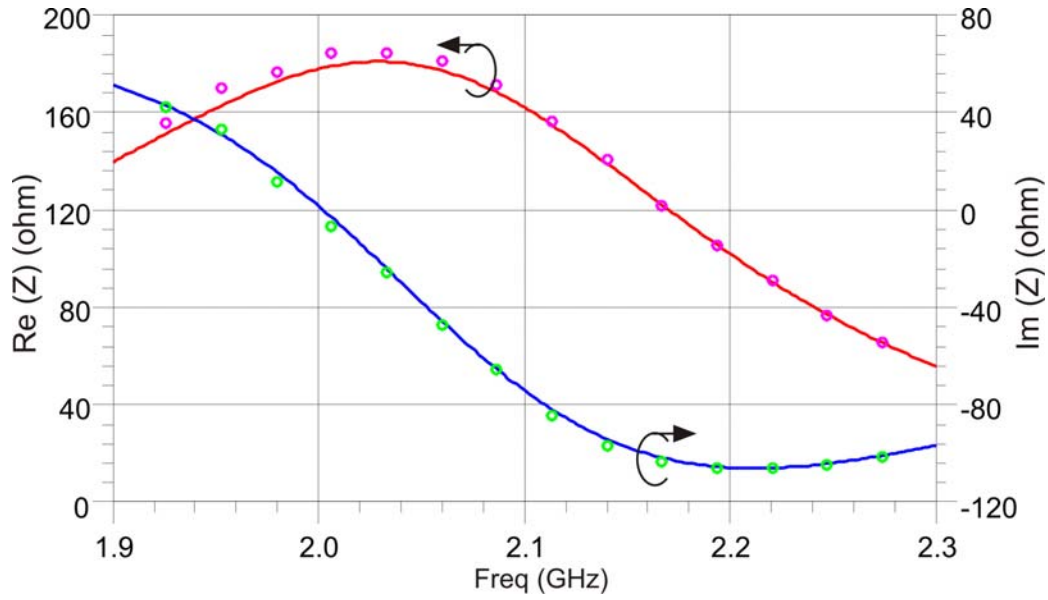


Figure 5.29 Impedance transformation based on the re-simulation (solid lines) of the input matching network with the tuned lengths of L1 and L2. (Measures results are in symbols.)

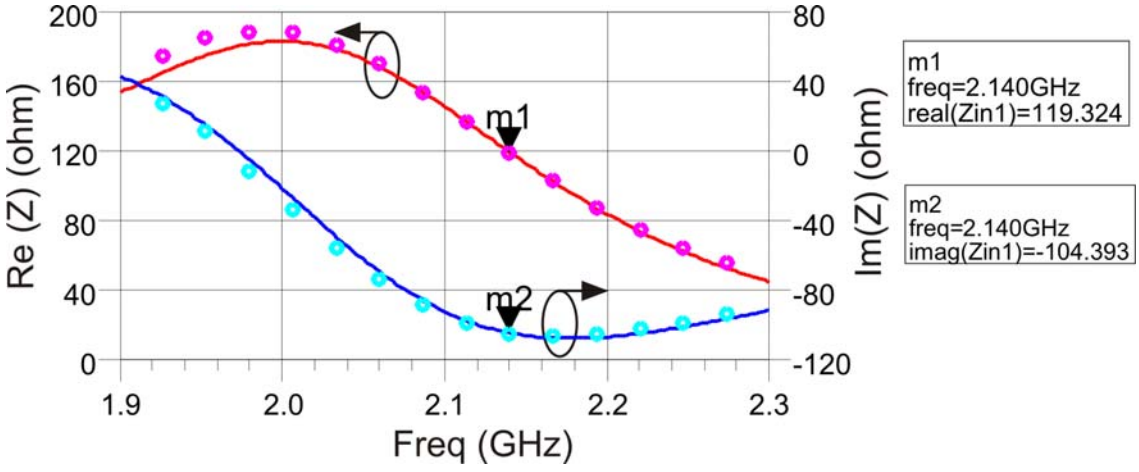


Figure 5.30 Simulated (solid lines) and measured (symbols) transformed impedance from the redesigned input matching network.

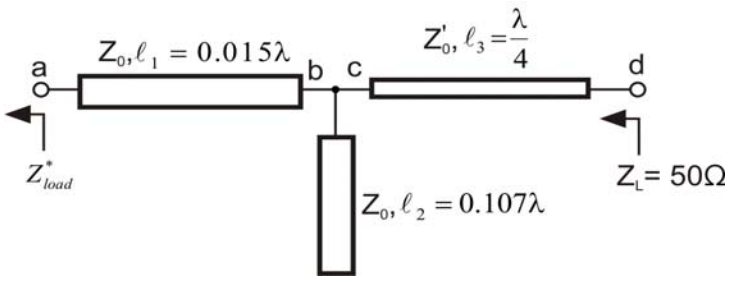
2. Output matching network

In comparison with the input matching network, the output matching network is intended to provide the desired load impedance by transforming the standard 50Ω load termination. As has been pointed out, the desired load impedance

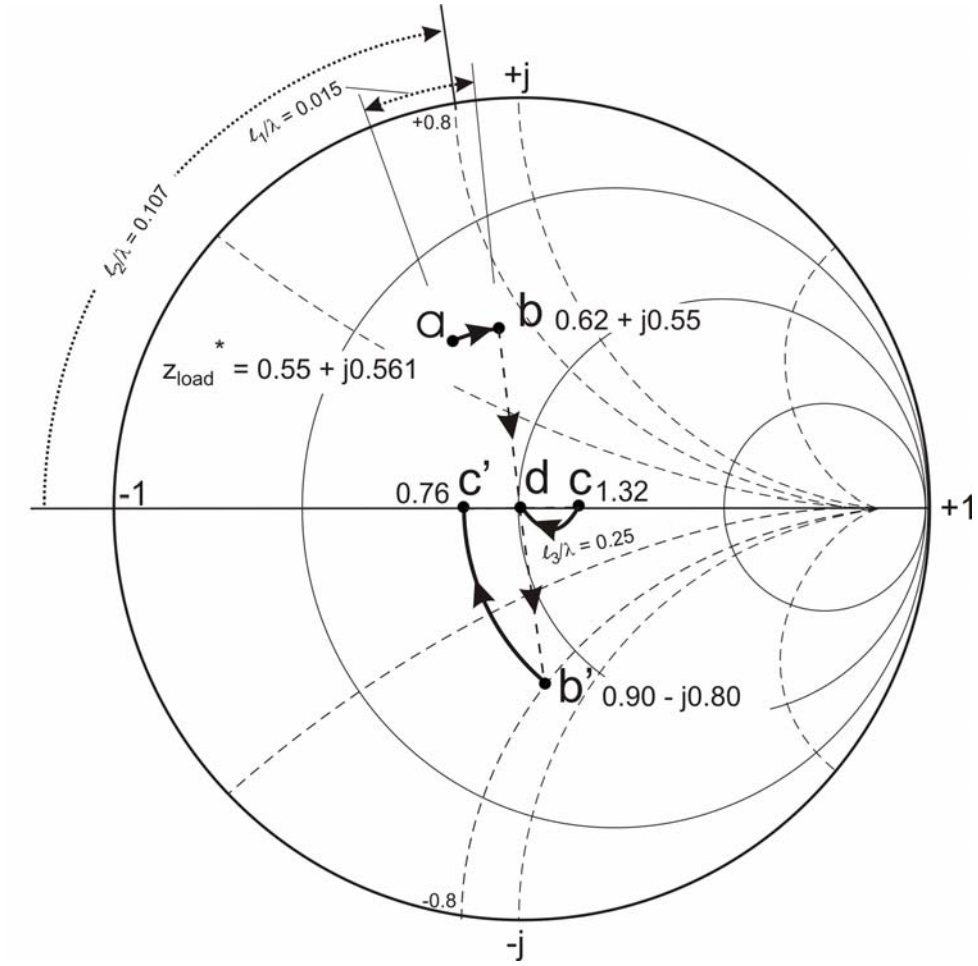
Z_{load} = (27.549 – j28.054)Ω in this design is determined by load-pull simulation. The normalized z_{load}^* = Z_{load}^*/50Ω = 0.55 + j0.561.

The Smith chart is utilized to design the output matching circuit. As shown in Figure 5.31, starting point *a* (0.55 + j0.561) is transformed by a series transmission line L1 (ℓ_1 = 0.015λ) to point *b* (0.62 + j0.55). Then, point *b* is projected to point *b'* (0.90 – j0.80), in order to use the open shunt transmission line L2 (ℓ_2 = 0.107λ) following a constant admittance circle. The length ℓ_2 is determined from the rotation of point *b'* to *c'* (0.76). The determination procedure has been explained in the input matching network design part. To come back the impedance Smith chart, point *c'* is projected to point *c* (1.32). After that, a quarterwave transformer is adopted to transform point *c* to the center point *d* of the Smith chart. The characteristic impedance of the transformer can be calculated as $Z_0^{'}$ = $\sqrt{50 \cdot 66.19}\,\Omega$ = 57.52Ω. For the other transmission lines L1 and L2, the characteristic impedances are 50Ω. A T-junction with different width is used to connect these three microstrip lines in the ADS simulation [118]. The symmetrical impedance step model is used to connect the L3 with the normal 50Ω microstrip line, at the right side [118].

Similar to the input matching network, the implementation of the output matching network is done in ADS using microstrip technology. The characterization of the fabricated output matching network is aimed to measure the transformed impedance value at the reference plane given in Figure 5.32. Thus, the real function in terms of impedance transformation can then be evaluated directly.



(a)



(b)

Figure 5.31 Output matching network: (a) topology and (b) design using Smith chart.

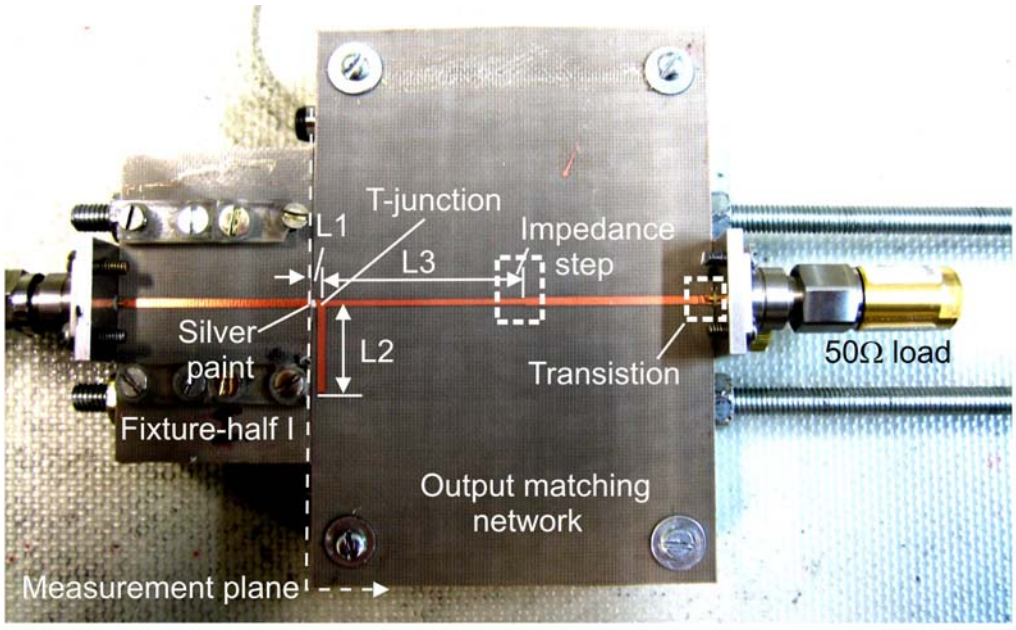


Figure 5.32 Characterization of the fabricated output matching network using the in-fixture measurement set-up.

The comparison of the measured and simulated transformed impedances of the output matching networks is given in Figure 5.33. The simulation shows that the designed output matching network can well transfer the 50Ω into the desired load condition, i.e. Z_{Load} = (27.549 – j28.044)Ω (as shown by marker 3 and 4). However, the measurement shows approximately 5Ω difference for both the real and the imaginary part.

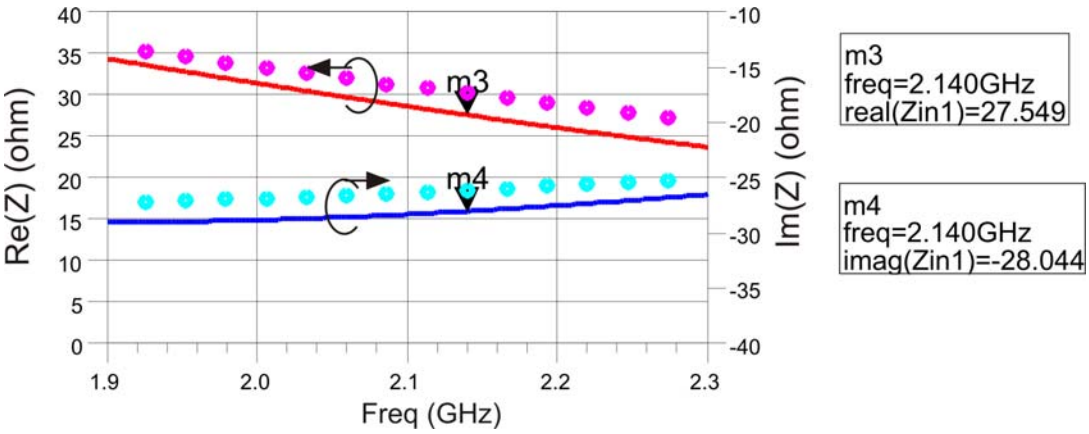


Figure 5.33 Simulated (solid lines) and measured (symbols) impedances of the designed output matching network.

In this case, the coaxial-to-microstrip transition, silver painting effects are included in the design procedure as before. The discrepancy for the output matching network is smaller compared to that of input matching network. And, this can be explained by comparing the Smith charts in both cases (Figure 5.23 and Figure 5.31). It can be seen that the transforming region for the output impedance is much more near to the center of the Smith chart, which means the change of the impedance is less sensitive to the change of the transmission line length used in the input matching circuits.

Consequently, tuning work has been initialized in the simulation to alter the design parameters to fit to the measured curves. Very good fitting result is achieved by tuning the lengths (ℓ_1 enlarged from 0.8 mm to 1.2 mm, ℓ_2 shortened from 10.43 mm to 9.71 mm, and ℓ_3 shortened from 21.8 mm to 20.6 mm), as given in Figure 5.34. In comparison with the tuning made for the input matching network, in both cases the open end stubs have been shortened in the order of 0.5 mm. However, the situation becomes obviously complicated for the output matching, since the junction widths for connecting ℓ_1 and ℓ_3 are different,

and also the length of ℓ_1 is very short (approximately 1 mm). Moreover, both lengths of L1 and L3 are affecting the final transformed impedance. The total effective length adjustment of the junction is a decrease of 0.8 mm, which is similar to the change made in the input matching circuit.

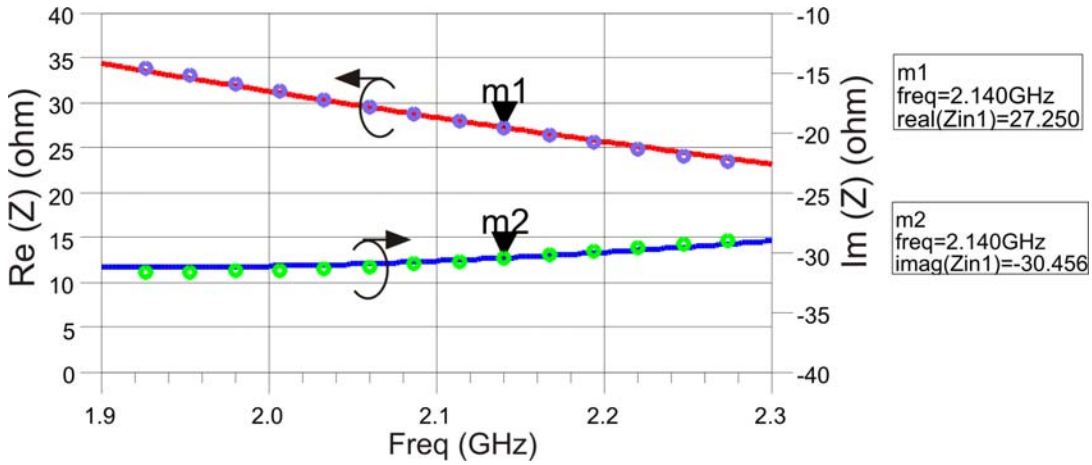


Figure 5.34 Transformed impedance based on the re-simulation (solid line) of the output matching network with tuned lengths of L1, L2 and L3 (symbols are measured results).

Since it is difficult to perform the post-fabrication modification on the fabricated circuit, the output matching circuit has been re-designed. The layout is generated under the consideration of the length differences observed above, which means the length of the microstrip lines is oppositely altered in the final layout implementation. This time, good agreement has been achieved directly as shown in Figure 5.35. As can been shown, in the measurement Z_{Load} = (27.25 + j30.456)Ω is tested (see marker 1 and 2), which is very close to the target impedance.

Thus, it has been shown that both input and output matching network have been successfully realized and verified. During the realization procedure, the importance and advantages of the partitioning design approach has been greatly demonstrated. The enabled access, to measure the transformed impedance from the fabricated matching networks, has highly assisted the designer to evaluate its design. This is rather difficult in the conventional single-step design method. And, it would have caused obvious discrepancy regarding the final power amplifier circuit, if the verification of the matching networks

would have been neglected. This verification task again makes the designer full of confidence about the realized sub-parts.

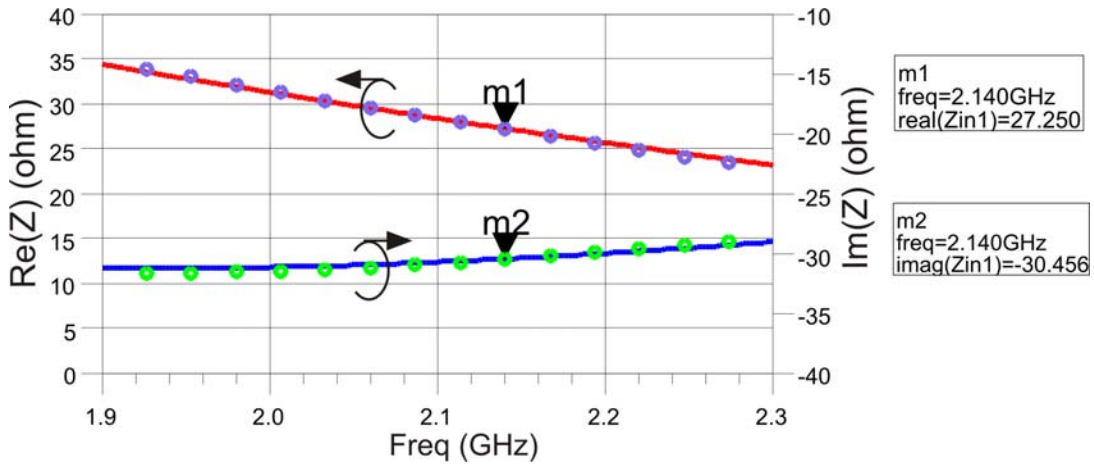
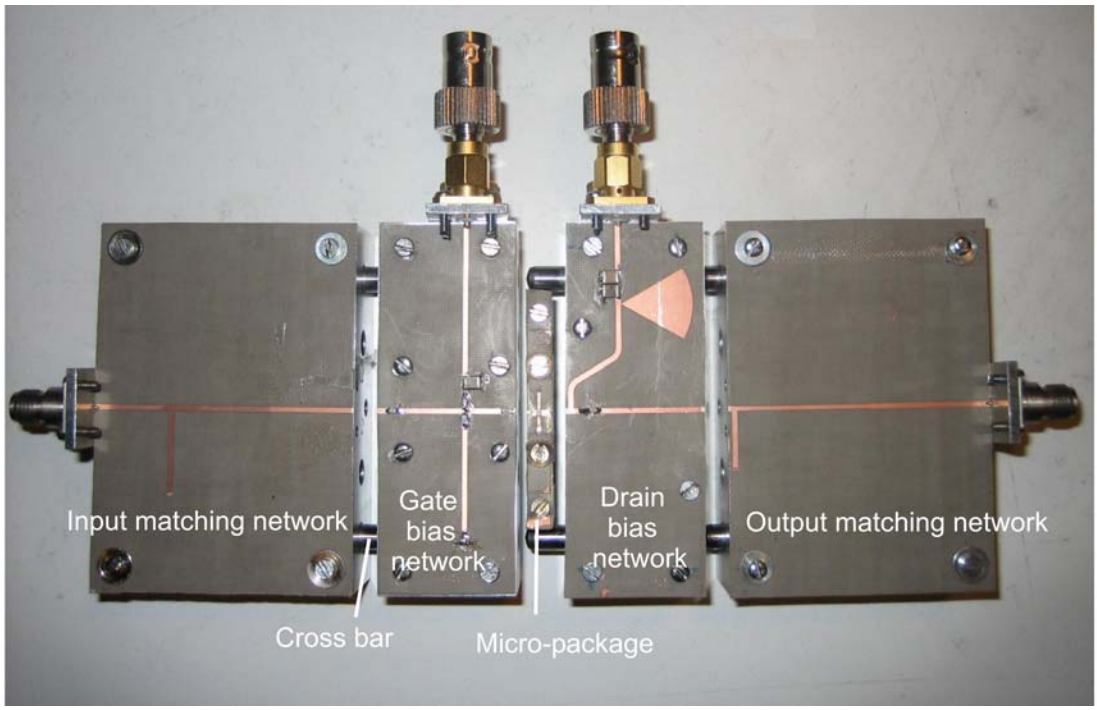


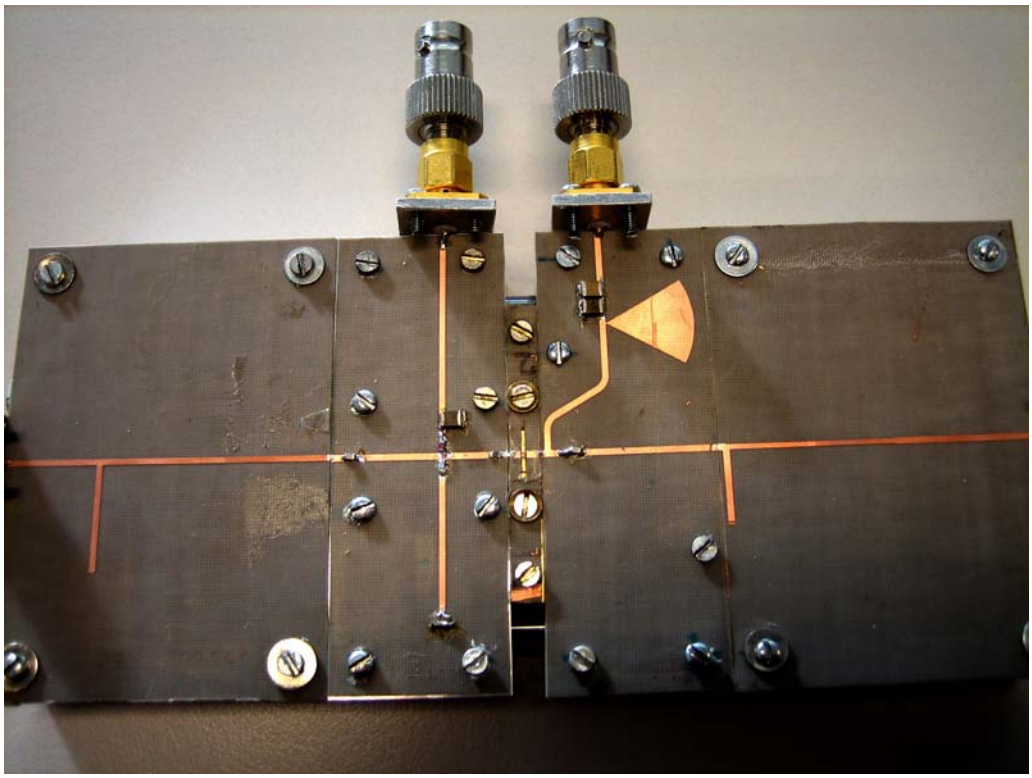
Figure 5.35 Simulated (solid line) and measured (symbols) transformed impedance of the re-designed output matching.

5.4 Power Amplifier Performance Evaluation

Finally, the complete power amplifier circuit will be assembled through interconnecting the successfully verified sub-parts together, which have been tackled in the previous sections with great care (Appendix C provides the design schematic of each sub-part). As shown in Figure 5.36(a), metal-made cross bars can make sure that the surfaces of each sub-part are on the same level. After that, silver painting is carefully adopted to make the connection between the microstrip lines after all the sub-parts having been compressed together, as given in Figure 5.36(b). At the end, the performance evaluation of the constructed power amplifier will be done in next sections for both small-signal and large-signal operation.



(a)



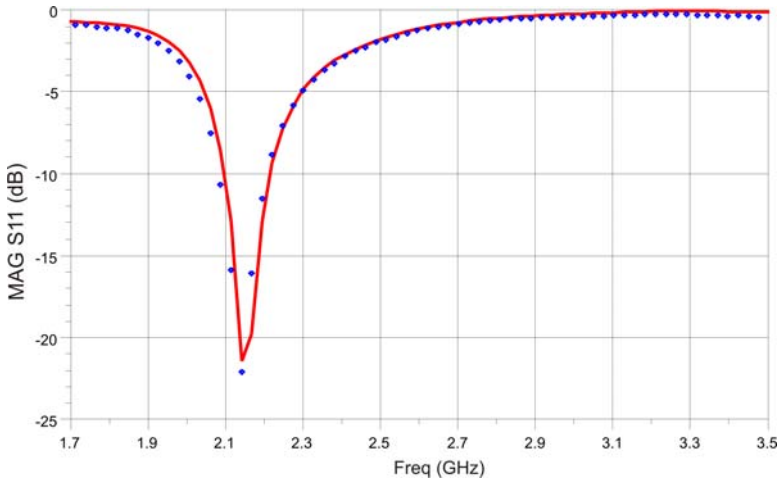
(b)

Figure 5.36 Final power amplifier circuit: (a) partitioning view, (b) complete assembly.

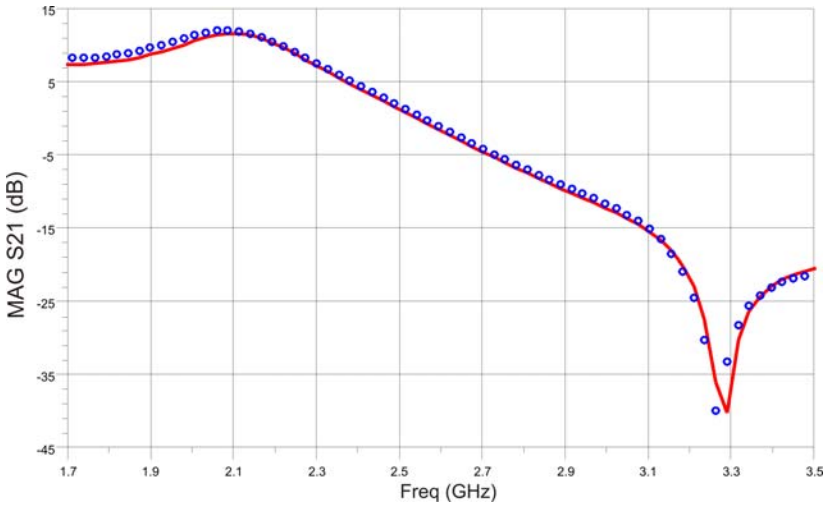
5.4.1 Small-Signal Performance

The small-signal S-parameters of the completely designed power amplifier has been measured at the operation bias point to evaluate the input and output return losses, small-signal gain and bandwidth.

As can be seen from the comparison, excellent match for all the four S-parameters between simulation and measurement in the frequency range from 1.7 GHz up to 3.5 GHz is given in Figure 5.37. At the operating center frequency (2.14 GHz), the return loss S11 shows less than -20 dB. The power amplifier has a small-signal gain S21 of 11. 5 dB. It has a gain variation of 1 dB within the frequency range from 2 GHz to 2.2 GHz. The output reflection coefficient S22 is approximately –5 dB, which is acceptable for RF power amplifier design.



(a)



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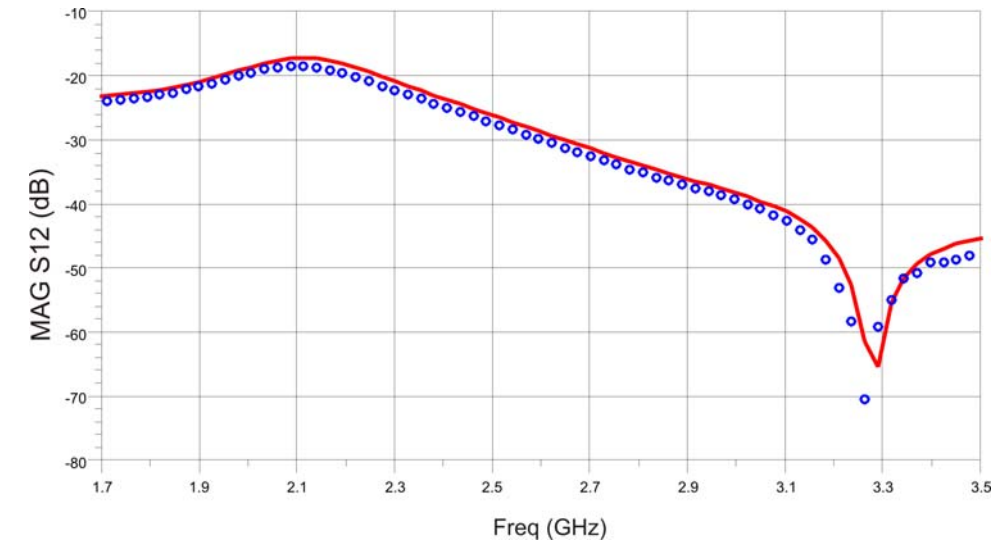
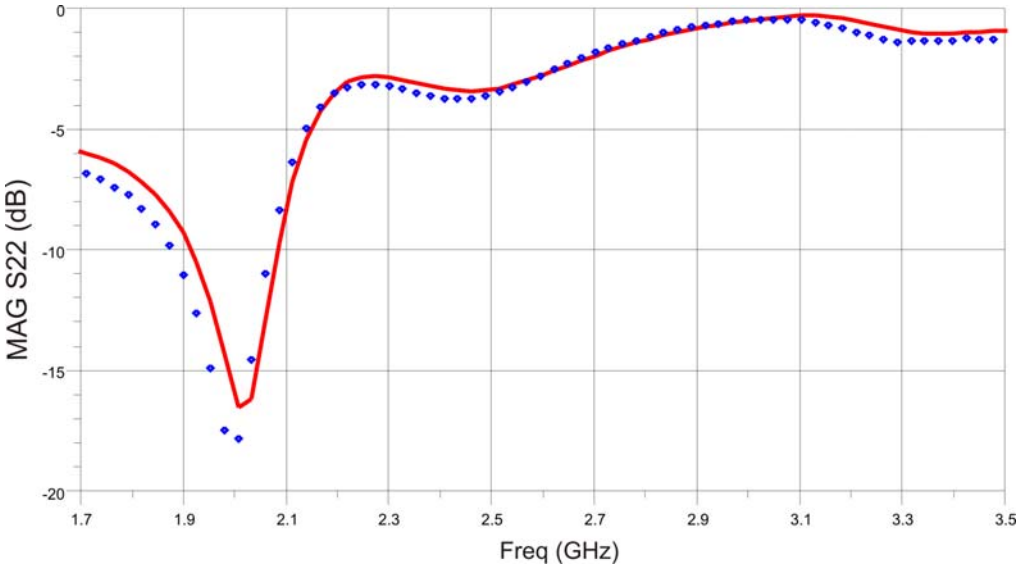


(c)



(d)

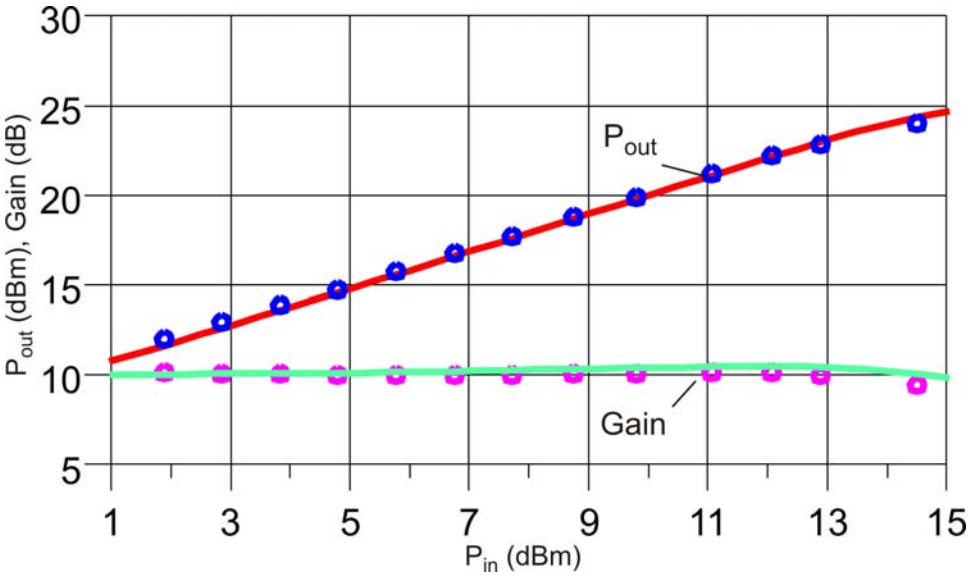
Figure 5.37 Measured (symbols) and simulated (solid lines) S-parameters of the complete power amplifier circuit biased at V_{GS0} = -2.1V and V_{DS0} = 9V.

It has to be emphasized that the comparison given above is done without any post-fabrication tuning on the final circuit after assembling them together nor with any adjustment on the previous delivered design result from simulation. Thus, it shows the first-pass success circuit design can become a reality using this proposed design strategy.

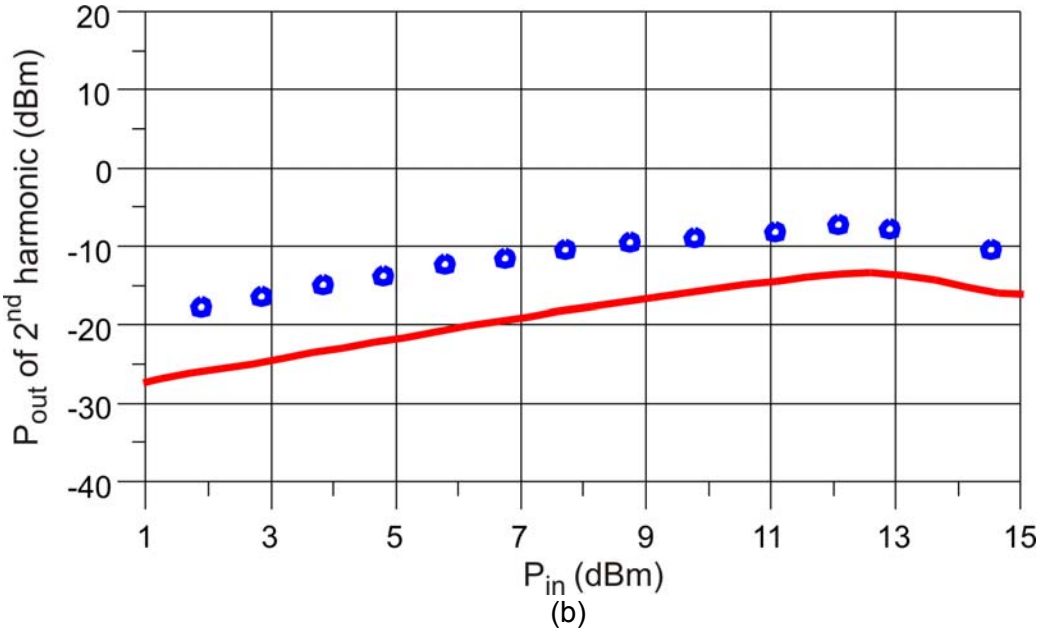
5.4.2 Large-Signal Performance

1. Single-tone power sweep measurement

The completely composed power amplifier is characterized under single tone stimulus to evaluate its large-signal performance.



(a)



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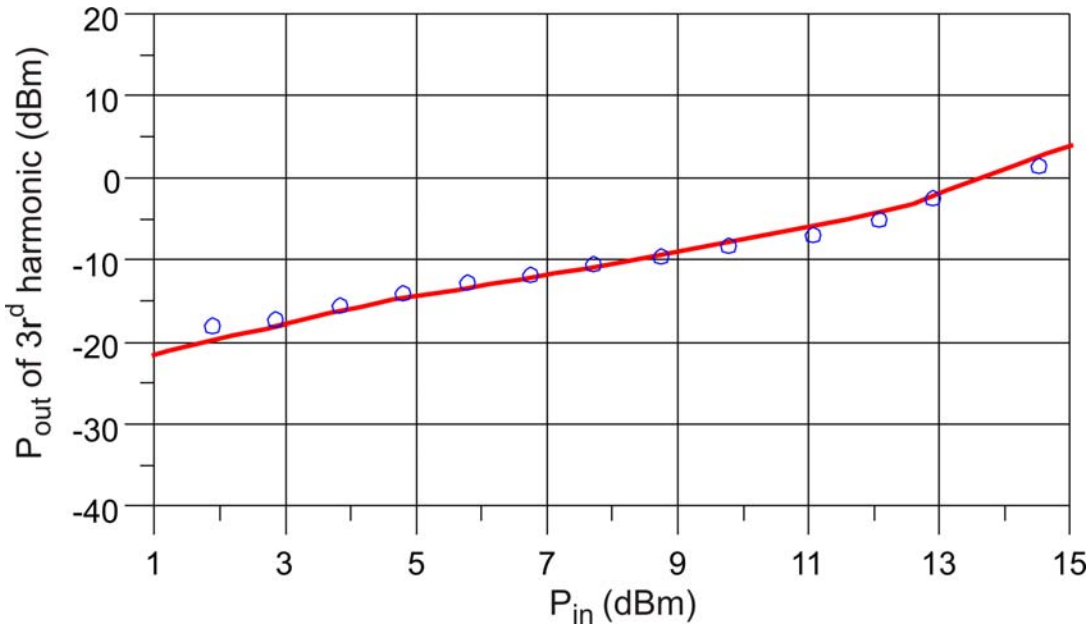

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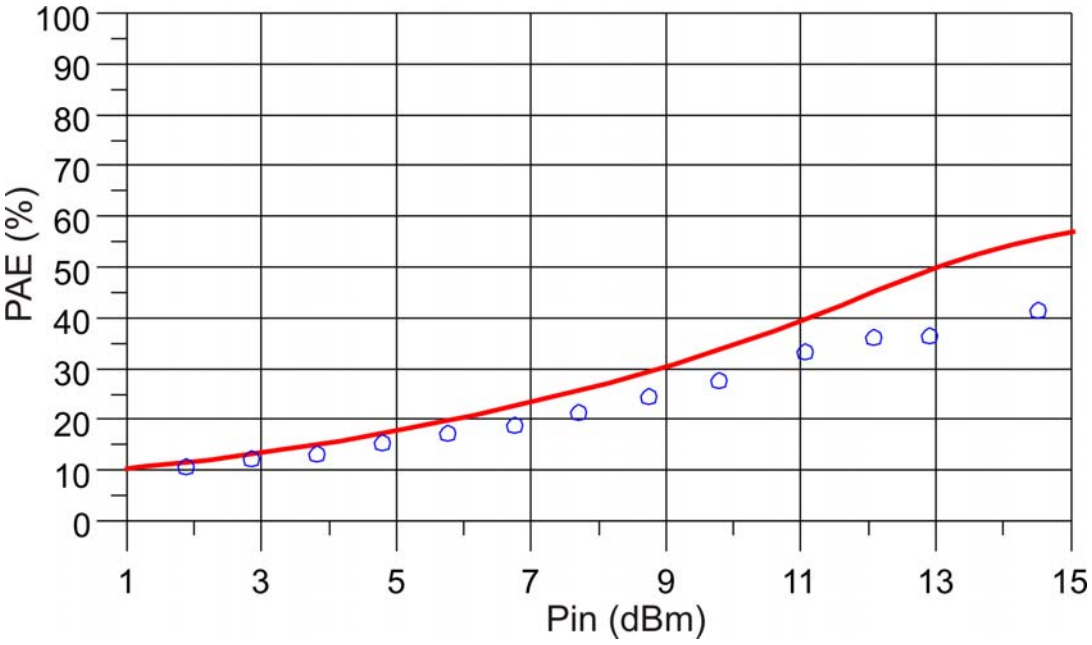


(d)

Figure 5.38 Single-tone power sweep performance of the complete power amplifier from simulation (solid lines) and measurement (symbols) biased at class-AB point (V_{GS0} = -2.1V and V_{DS0} = 9V): (a) gain and output power at fundamental, (b) output power at second harmonic, (c) output power at third harmonic, and (d) power added efficiency.

The measured output power and power added efficiency are compared with simulation results, as shown in Figure 5.38. In Figure 5.38(a), the power amplifier has around 10 dB large-signal gain as predicted by simulation and the corresponding 1-dB compression point P_{1dB} occurs with the input power level of 15 dBm. Very good fitting of the output fundamental power between simulation and measurement has been obtained. Regarding the output power at higher order harmonics, it can be seen that perfect agreement for the third harmonic is achieved. For both harmonics prediction, simulation can predict the trend very well. There is 5 to 10 dB difference for the second harmonic at very low output power level. The reason behind is seen in the imperfection of the nonlinear large-signal model for extracting the power level at the second harmonic. Good fitting results regarding power added efficiency is also obtained. It can be seen from Figure 5.38(d) that the discrepancy is within 5% at the 3-dB back-off region, which is the main operation region of interest.

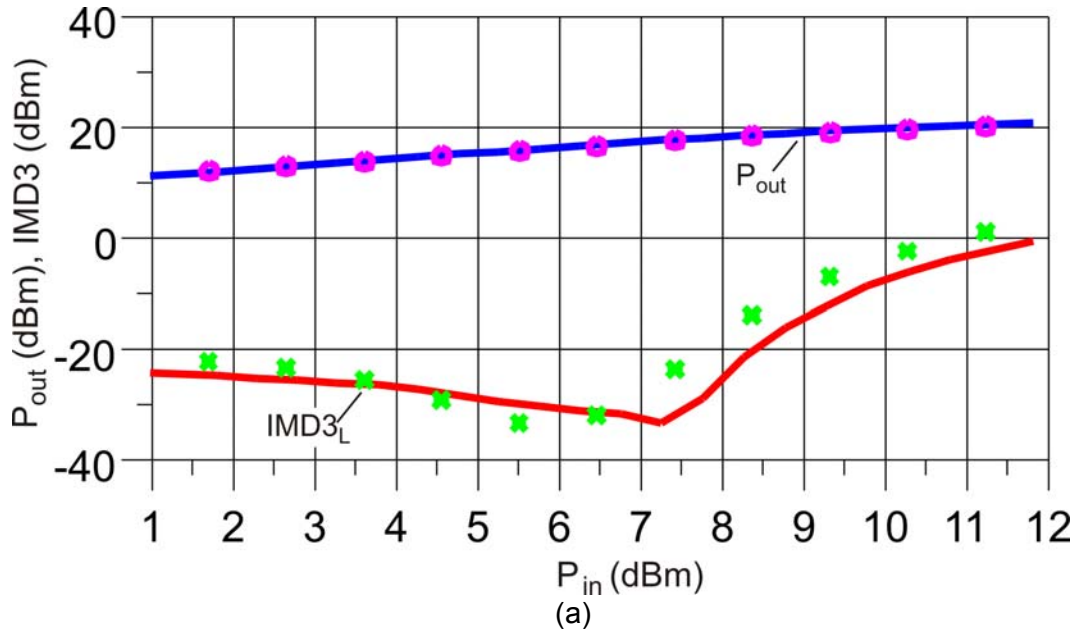
2. Two-tone power sweep measurement

Two-tone test is the most widely used method to test the linearity performance of amplifiers. Thus, it has been adopted to analyze the linearity performance of the designed circuit. The measurement system used consists of a dual channel vector signal analyser (VSA) as the receiver, and a multi-tone electronic signal generator as the signal source. Both incoming and outgoing waves at the input side and the output side can be measured. Figure 5.39 shows the comparison of the fundamental output power and the lower IMD3 with 200 kHz and 5 MHz tone spacing, respectively. In cases, very good agreement between measured curves and simulation prediction for both fundamental and IMD3 power is obtained. This confirms that, even under the sophisticated test conditions the final circuit can still meet the targeted design specification without any post-fabrication tuning work.

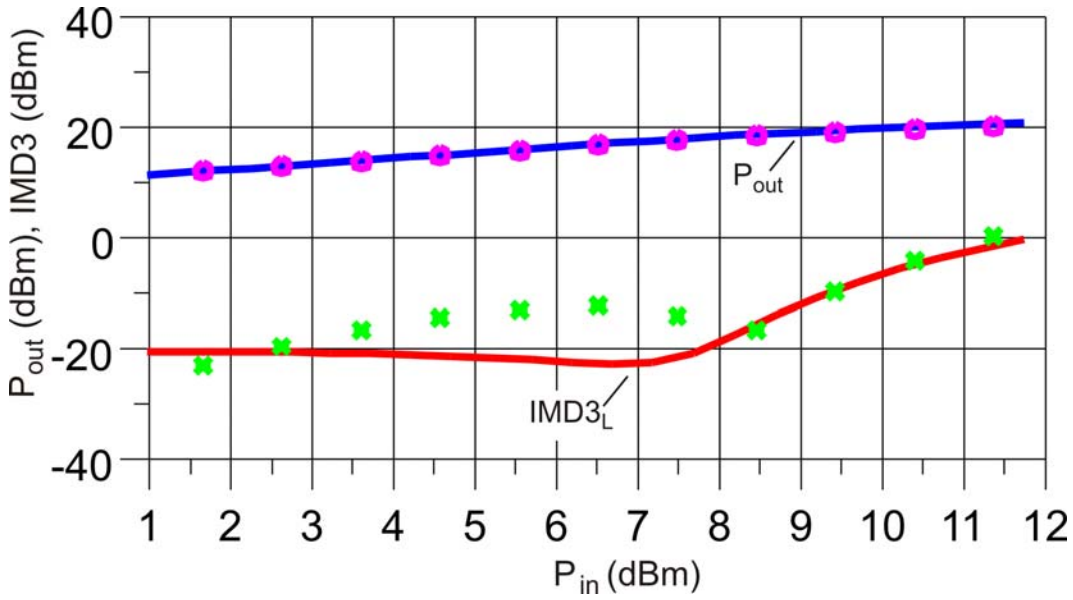
In Appendix D, a class-AB power amplifier using the transistor from the same wafer is designed at the same operating frequency following the conventional design approach. The design procedure is similar to that of the demonstrator. However, as can be seen from Figures D.1-D.3, the design target has not been achieved by the first realized circuit. By making this comparison, the superiority

of the developed partitioning design approach can be clearly seen. The excellent final results obtained for the demonstrator confirms the feasibility of the partitioning design approach for reliable RF power amplifier design.

The ultimate intention of the proposed novel design concept is to tackle the design tasks of advanced power amplifiers with more complicated architectures, such as balanced amplifier, Doherty amplifier, and class-S switching mode amplifier [2, 6 and 120]. In those complex circuits, several active devices are contained. Moreover, the interaction between each interior sub-part becomes very critical for the entire circuit performance. Thus, the design task becomes much more challenging. The partitioning design approach with the distinctive advantage to provide the designer the direct access for evaluating sub-part design separately will greatly facilitate the design and will solve such complex circuit design tasks in an efficient way. The knowledge and experience gained from this class-AB demonstrator design, thus, may be taken as a reliable design basis for more complex nonlinear microwave circuits and systems.



(a)



(b)

Figure 5.39 Simulated (solid lines) and measured (symbols) output power and intermodulation distortion of the composed class-AB power amplifier under two-tone excitation (V_{GS0} = -2.1V and V_{DS0} = 9V) at f_c = 2.14 GHz. Two-tone spacing: (a) Δf = 200 kHz, (b) Δf = 5 MHz.

Chapter 6

Conclusions and Outlook

In this research work, the proposed novel partitioning design approach for RF circuit design, in particular for RF power amplifier design, has been deeply investigated and successfully demonstrated. Its main distinctive superiority compared with the conventional design method in terms of facilitating and accelerating design procedures has been confirmed by a class-AB power amplifier demonstrator design. Following this approach, the aimed target of achieving the reliable circuit design in an innovative straightforward way becomes then a reality, which means that the circuit designer is able to obtain the expected circuit performance predicted in the simulation without tedious iterative post-fabrication tuning work. Furthermore, the access to the interior part of the entire circuit and the feasibility of verifying sub-part circuit enabled by the partitioning design approach in contrast to the conventional approach have been completely proved to be highly essential, in particular for tackling complex circuit design.

The main research conclusions are summarized as follows:

1. One critical factor of the partitioning design approach is the planar-interconnection techniques for assembling separately designed sub-circuits. After observing the practical performance in terms of reliability, repeatability, manufacturability of different techniques using the in-fixture calibrated measurement set up (THLR, up to 6 GHz), silver-painting method has been finally selected. It has the superior properties after

comparison with other connection technologies, such as soldering, multi-wire bonding and copper ribbon. Also, the importance of the chip device mounting using conductive silver epoxy and the careful attention for chip-to-microstrip connection have been clearly stated and explained from a practical point of view.

2. Measurement based large-signal model including trapping and self-heating effects has been developed for the 1.2 mm AlGaAs/GaAs HEMT chip. The model has shown good capability for predicting the output power (for both fundamental and harmonics) and linearity. The design comprising passive SMD resistors, capacitors, and inductors have been modelled using in-fixture measurement. The parasitic effects and mounting effects have been considered. The CAD models have been verified and used in the partitioning design approach.

3. In the course of the class-AB power amplifier design, different sub-circuits of the entire amplifier, such as micro-packaged device, bias networks, matching networks were designed and characterized separately. The redesign (fine-tuning) of the layout of the matching networks to achieve the desired impedance values in the real environment emphasizes the necessity of observing the true performance of each designed sub-part. Excellent agreement between the finally assembled complete power amplifier measurement results and the simulation demonstrates the success of the proposed design approach. It has been shown that it is possible to obtain a first-pass success in the design of RF power amplifier circuits circumventing expenditure and time-consuming reruns.

For the industrial mass production purpose, it is wise to conduct the prototype circuit design during the initial development phase using the partitioning design approach, in order to master the key design aspects efficiently and overcome the design challenges smartly. Once the complete design knowledge is established and design procedure becomes nearly a routine, the focus can then be shifted to the line-production following the simple one-step fabrication procedure. Hence, overall time-to-market of a new product can be minimized by incorporating the partitioning design approach, to be competitive in the fast developing market.

On the basis of the research work accomplished in this dissertation, it is extremely exciting and recommended to apply this novel approach for the design of more complex amplifier architecture circuits demanded by the next generation mobile communication. In the upcoming 4G mobile communications, spectrum efficient modulated signals with higher peak to average power ratio (in the range of 12 – 16 dB) is adopted. As one outstanding candidate, multi-stage Doherty amplifier is considered to obtain high power efficiency at greater dynamic range (12 dB for three-stage) to overcome this challenge. However, it is extraordinarily difficult to tackle such kind of circuit realization following the one-step conventional design approach, since there will be a large amount of ambiguity in the design. Increasing design difficulties will occur with increased circuit complexity. Consequently, it will be a very interesting extension to start a three-stage Doherty amplifier research project based on the partitioning design approach developed in this work.

Appendix A

THLR In-Fixture Calibration

In order to perform non-coaxial measurement, in-fixture calibration method is needed to shift the coaxial reference planes (1´ and 2´) to the DUT measurement plane 1 and 2 [121]. It is a straightforward way to get the information of DUT through in-fixture measurement compared with de-embedding procedure, in which, however, un-certainties may be faced [122].

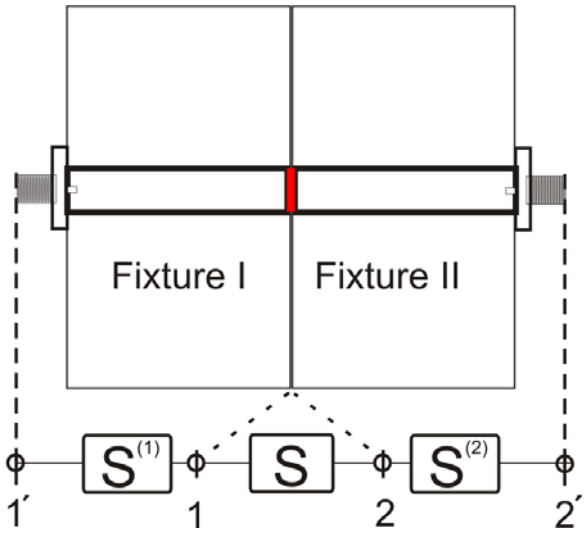


Figure A.1 Definition of the reference planes and S-parameters of the microstrip test fixture [123].

THLR (**T**hrough, **H**igh and **L**ow **R**eflection) in-fixture calibration employed in this work has a wide frequency range compared with the normal TRL (**T**hrough, **R**eflection and **L**oad) calibration procedure [124]. Initially, VNA has been calibrated using the normal SOLT (**S**hort, **O**pen, **L**oad and **T**hrough) calibration setting the reference plane at 1´ and 2´. After that, THLR calibration is performed to calculate the $S^{(1)}$ and $S^{(2)}$ error block using the ideal through, non-critical open, non-critical short and sliding load standards, as listed in Figure A.2. Finally, the calibration plane is shifted to the plane 1 and 2.

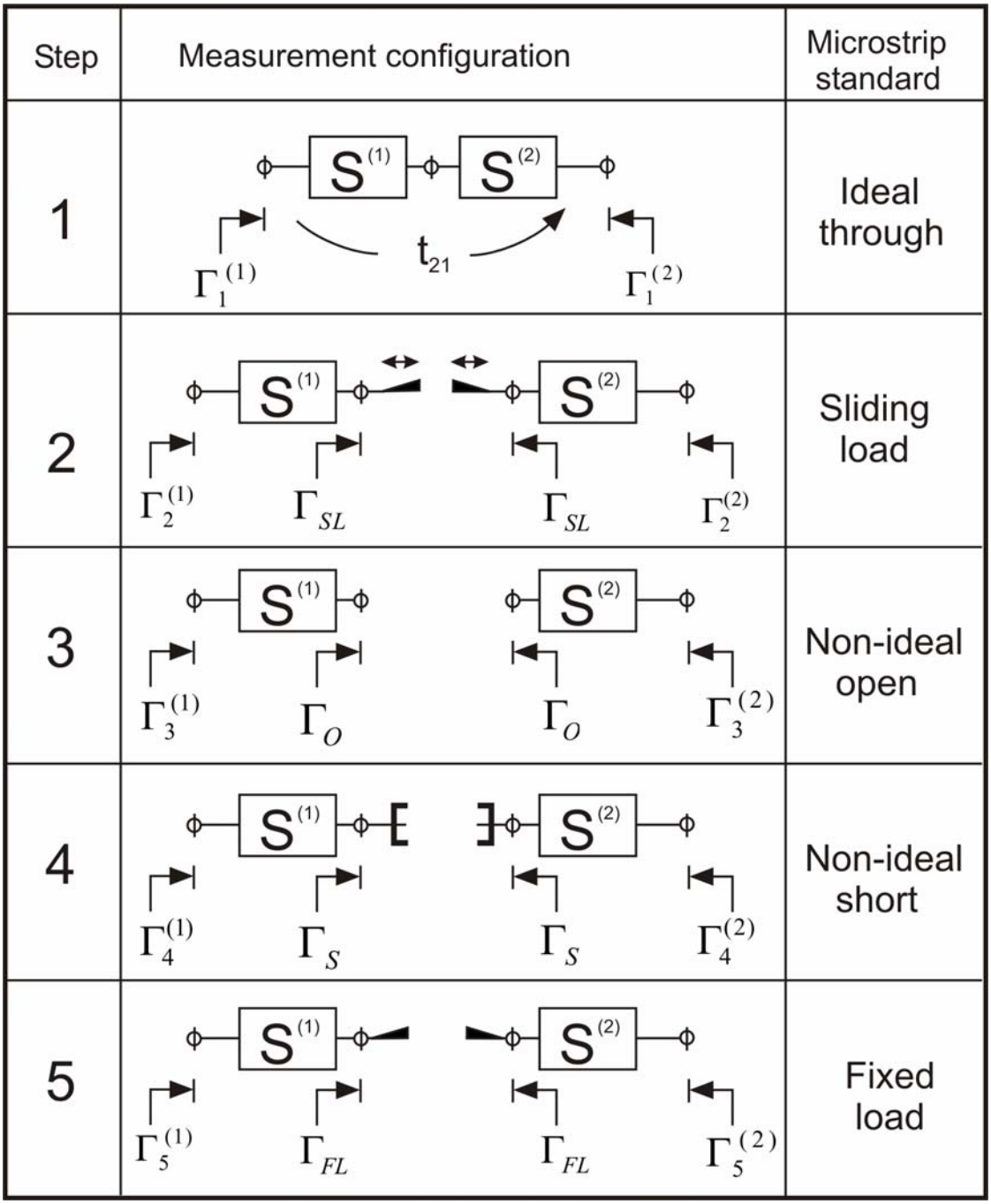


Figure A.2 Series of the calibration steps and standards [123].

In this work, the THLR in-fixture calibration has been performed up to 20 GHz. The error-corrected measurements of the amplitude and phase of an open standard (open in the air) are given in Figure A.3. It can be shown that magnitude of the reflection coefficient at both ports is within 5%, and the phases are less than 6 degrees up to 20 GHz. The results show that this fixture is well-calibrated and thus, it can be used to perform in-fixture measurement reliably.

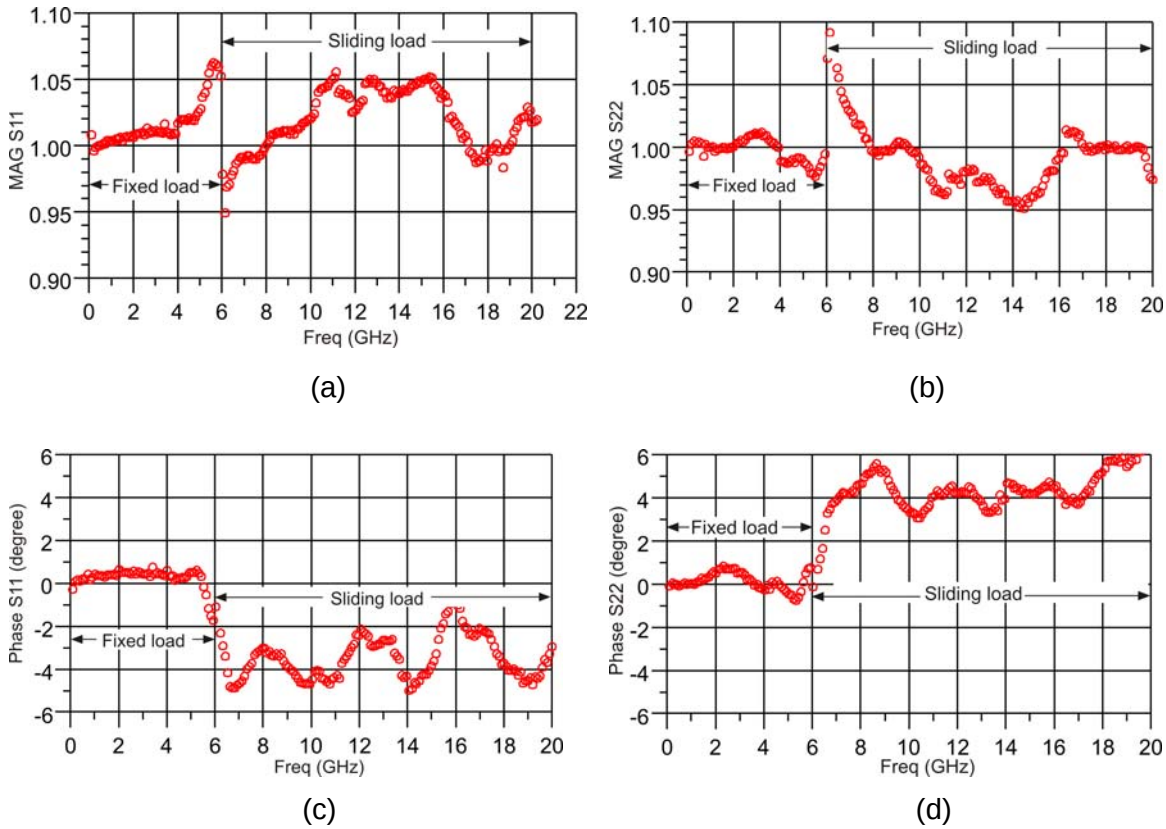


Figure A.3 Error-corrected measurement of an open standard of the calibrated fixture-halves: (a) magnitude of S11, (b) magnitude of S22, (c) phase of S11, and (d) phase of S22.

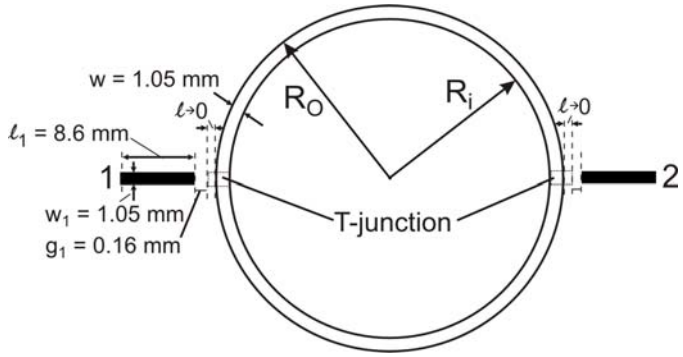
Appendix B

Precise Determination of Substrate Permittivity

For accurate design using microstrip technology, the precise relative permittivity (ε_r) of the substrate material is highly desired [125]. However, the used Teflon substrate relative permittivity stated in the datasheet is 2.51 with $\pm$ 0.04 tolerances. Thus, in order to precisely determine the permittivity of the substrate in use, a ring resonator is fabricated to investigate the substrate material permittivitiy, as shown in Figure B.1. This method has the advantage that calibration system error will not change the resonance frequency of the ring resonator, which is excited through a loose coupling at port 1 and 2. After fabrication, the real dimension of inner and outer radii are exactly measured. And the average diameter is determined by taking the arithmetical average radii R_i and R_o. Then, the S-parameter simulation of the designed ring resonator is performed in ADS. The schematic is given in Figure B.2(a).

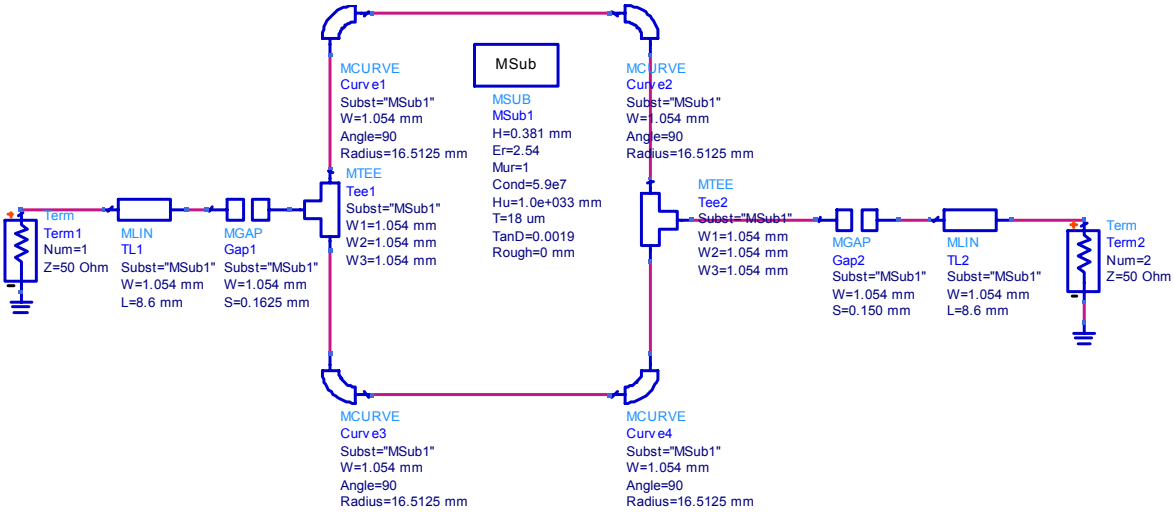
As seen from Figure B.1(a) and (c), microstrip T-junction (Hammerstad's model used in ADS® schematic simulation) is adopted for making the connection of the microstrip curves with the microstrip feeding line, between which gap model is inserted for modeling the coupling effects. Dispersion is included in the gap model and also in the microstrip curve model used. Strictly speaking, the T-junction model adopted in the schematic simulation does not completely reflect the real situation, because the length of the port (connecting with the gap model) is reduced to the limit case, zero. Thus, momentum field simulation is performed to model the reality more exactly. In Figure B.1(d), S21 of the ring resonator from schematic simulation, momentum simulation and measurement is compared. Very good fittings are achieved among them, indicating that the T-junction model limitation does not influence the result noticeably in the considered frequency range.

Finally, the relative permittivity of the Teflon substrate in use is determined to be ε_r = 2.54, on the basis of the results shown in Figure B.1(d).

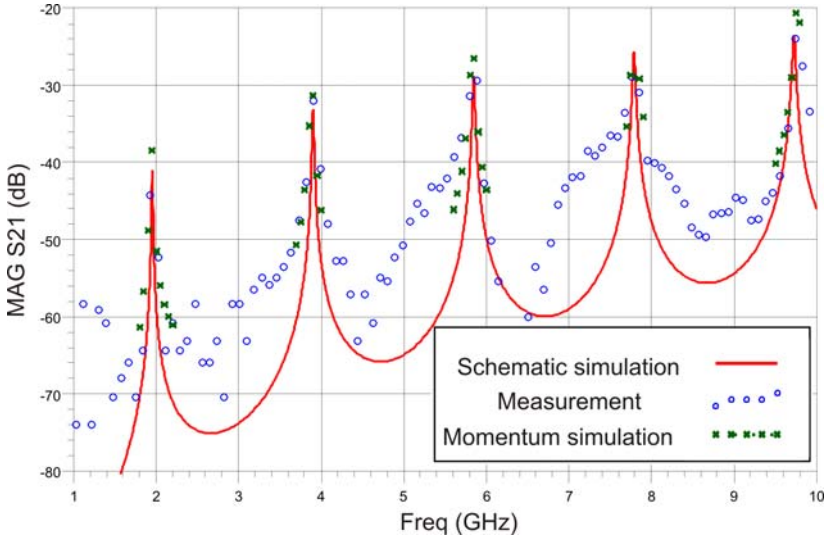


(a)

(b)



(c)

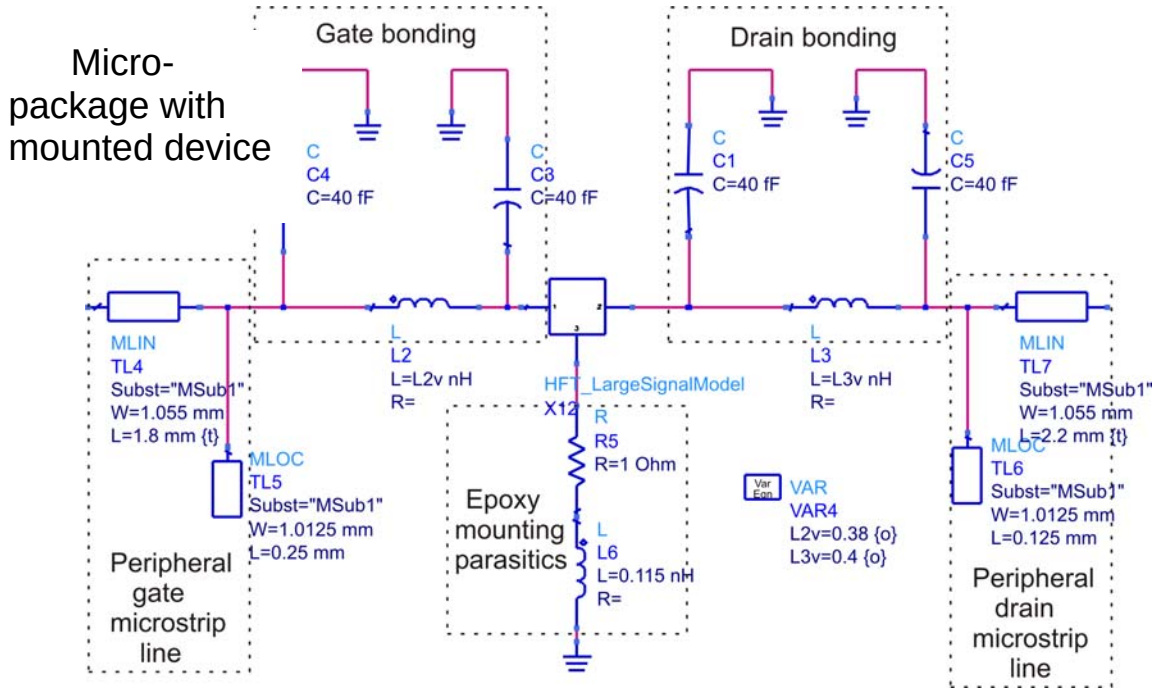


(d)

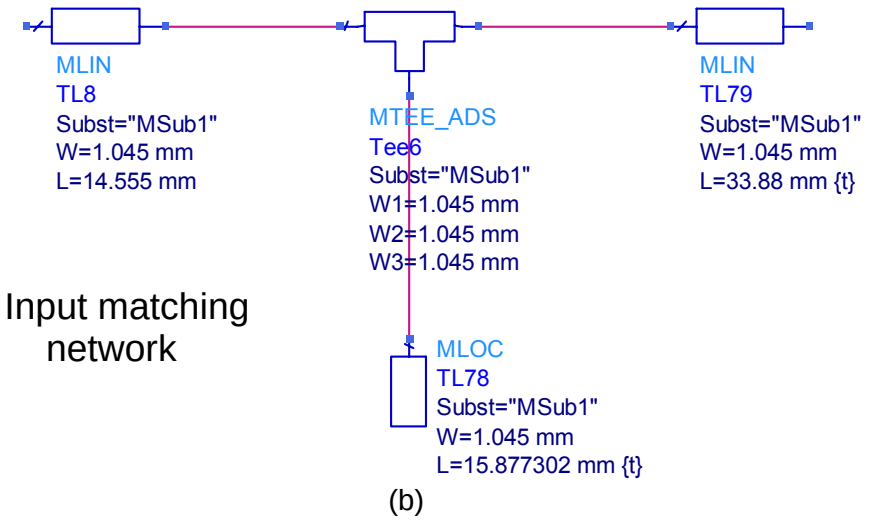
Figure B.1 Ring resonator: (a) schematic, (b) photograph of fabricated circuit, (c) schematic simulation, and (d) S-parameter comparison between measurment and simulation.

Appendix C

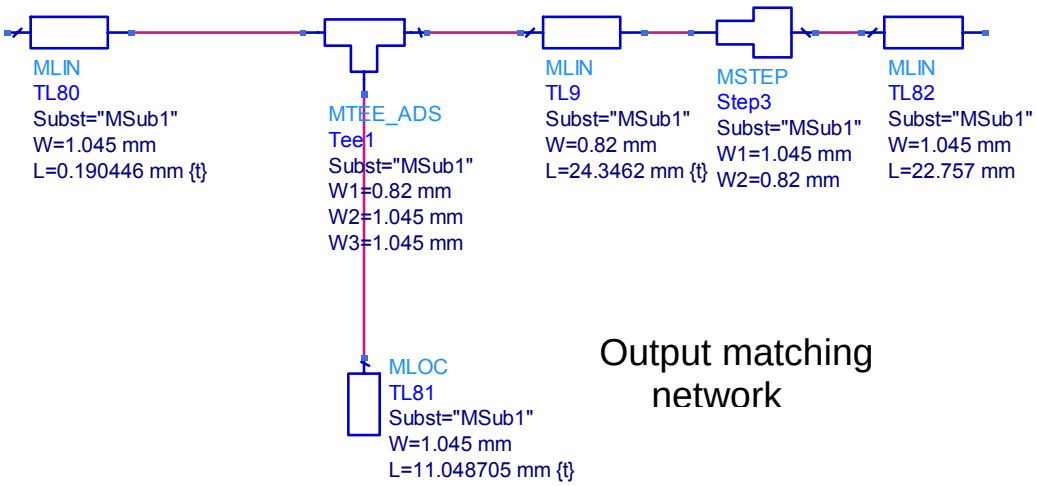
Schematic Circuit of the Designed Power Amplifier Demonstrator



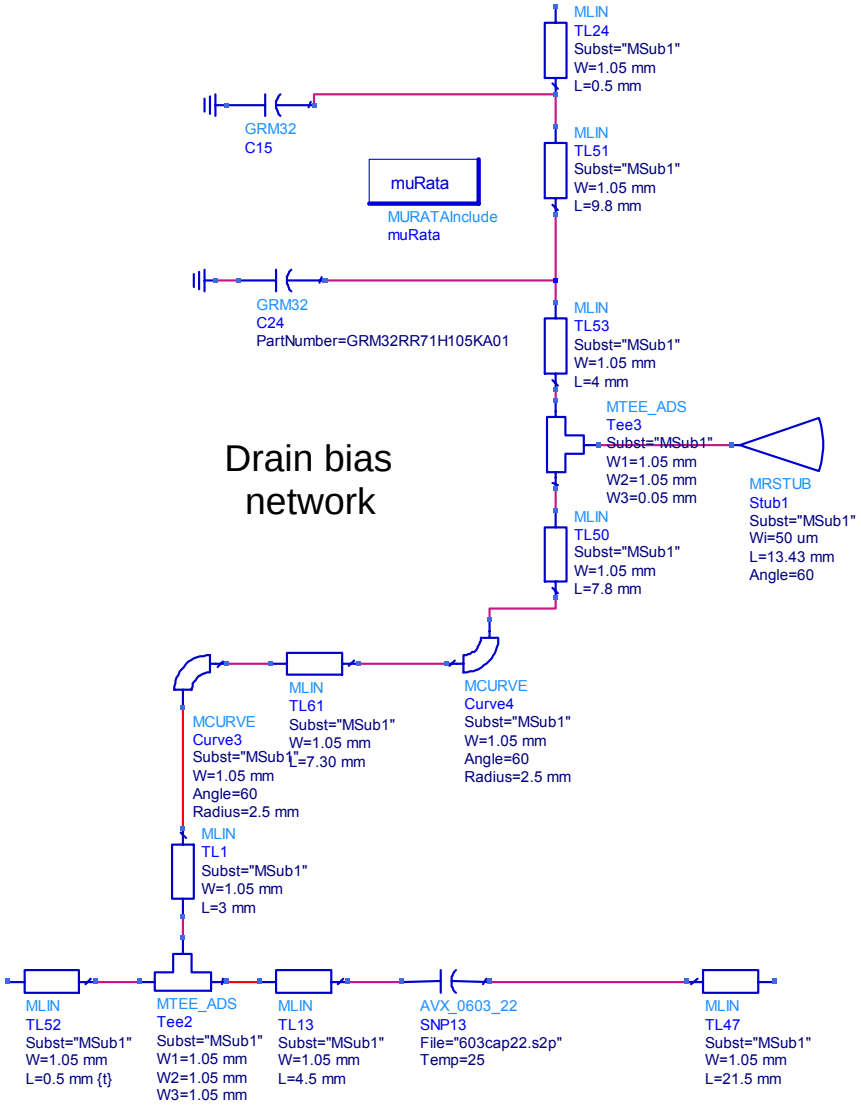
(a)



(b)


MLIN
TL80
Subst="MSub1"
W=1.045 mm
L=0.190446 mm {t}
MTEE_ADS
Tee1
Subst="MSub1"
W1=0.82 mm
W2=1.045 mm
W3=1.045 mm
MLIN
TL9
Subst="MSub1"
W=0.82 mm
L=24.3462 mm {t}
MSTEP
Step3
Subst="MSub1"
W1=1.045 mm
W2=0.82 mm
MLIN
TL82
Subst="MSub1"
W=1.045 mm
L=22.757 mm
MLOC
TL81
Subst="MSub1"
W=1.045 mm
L=11.048705 mm {t}
Output matching network

(c)


MLIN
TL24
Subst="MSub1"
W=1.05 mm
L=0.5 mm
GRM32
C15
MLIN
TL51
Subst="MSub1"
W=1.05 mm
L=9.8 mm
muRata
MURATAInclude
muRata
GRM32
C24
PartNumber=GRM32RR71H105KA01
MLIN
TL53
Subst="MSub1"
W=1.05 mm
L=4 mm
MTEE_ADS
Tee3
Subst="MSub1"
W1=1.05 mm
W2=1.05 mm
W3=0.05 mm
MRSTUB
Stub1
Subst="MSub1"
Wi=50 um
L=13.43 mm
Angle=60
MLIN
TL50
Subst="MSub1"
W=1.05 mm
L=7.8 mm
Drain bias network
MLIN
TL61
Subst="MSub1"
W=1.05 mm
L=7.30 mm
MCURVE
Curve4
Subst="MSub1"
W=1.05 mm
Angle=60
Radius=2.5 mm
MCURVE
Curve3
Subst="MSub1"
W=1.05 mm
Angle=60
Radius=2.5 mm
MLIN
TL1
Subst="MSub1"
W=1.05 mm
L=3 mm
MLIN
TL52
Subst="MSub1"
W=1.05 mm
L=0.5 mm {t}
MTEE_ADS
Tee2
Subst="MSub1"
W1=1.05 mm
W2=1.05 mm
W3=1.05 mm
MLIN
TL13
Subst="MSub1"
W=1.05 mm
L=4.5 mm
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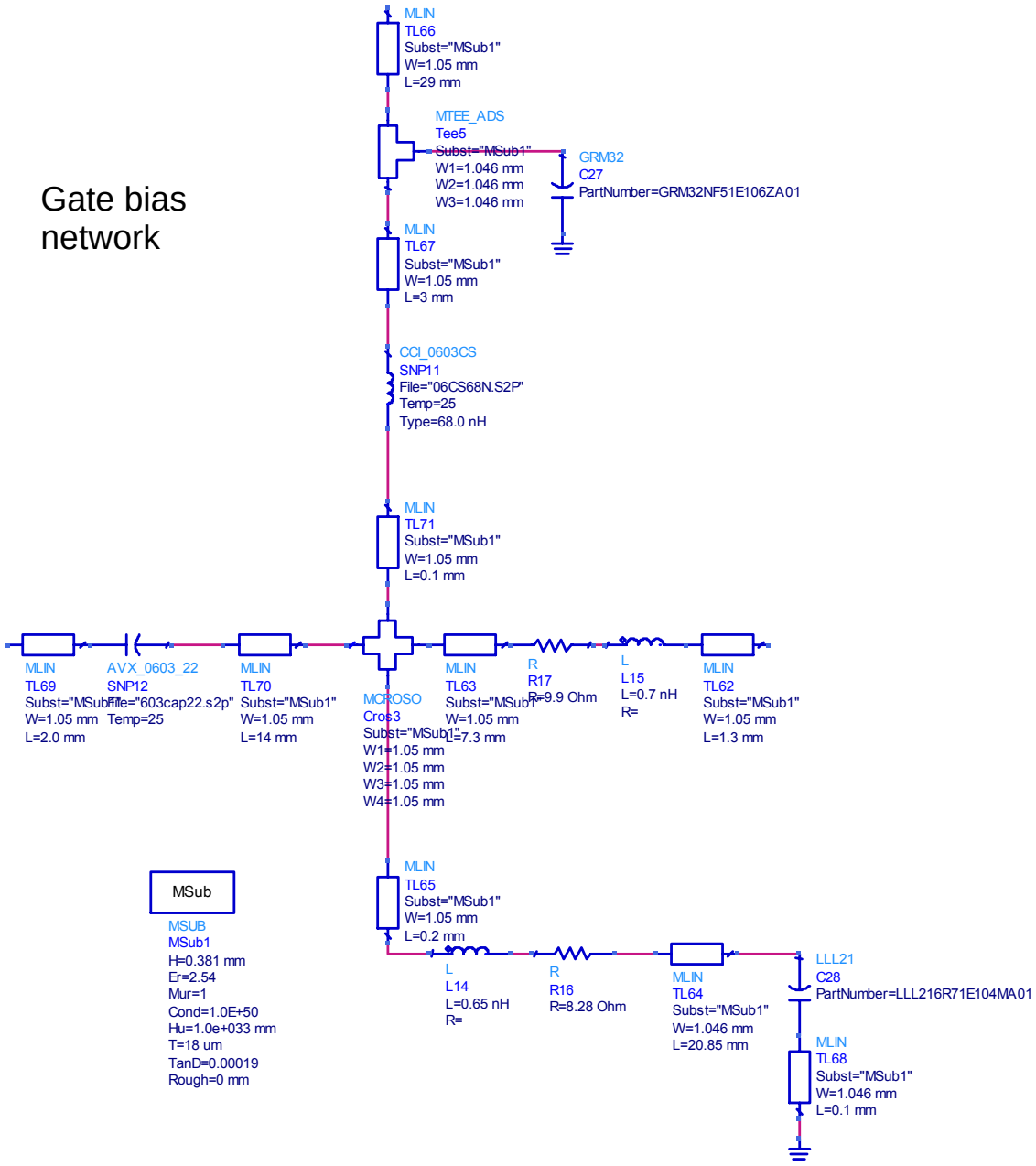
(d)



(e)

Figure C.1 Schematic circuit of the designed demonstrator power amplifier: (a) micro-package with mounted device, (b) input matching network, (c) output matching network, (d) drain bias network and (e) gate bias network.

Appendix D

Power Amplifier Design Following the Conventional Design Approach

Before starting using the proposed novel partitioning design approach, one amplifier has been initially designed following the conventional one-step design approach. It uses the same AlGaAs/GaAs HEMT chip transistor, taken from the same wafer. Design is done also at 2.14 GHz and has the same bias point (V_{GS0} = -2.1V and V_{DS0} = 9V). The chip is mounted on a brass bar using silver epoxy. It is then pasted on the aluminium made fixture again using silver epoxy, which now should be considered causing some uncertainty of grounding. The design of the matching and bias networks are following nearly the same concept developed in Chapter 5. The fabricated amplifier is shown in Figure D.1.

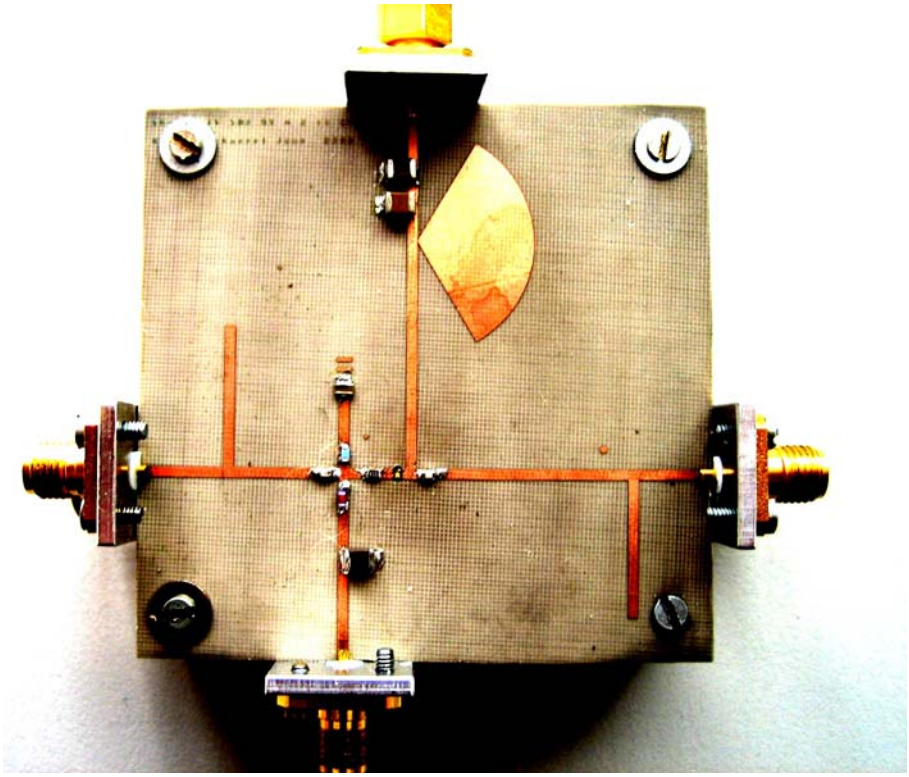
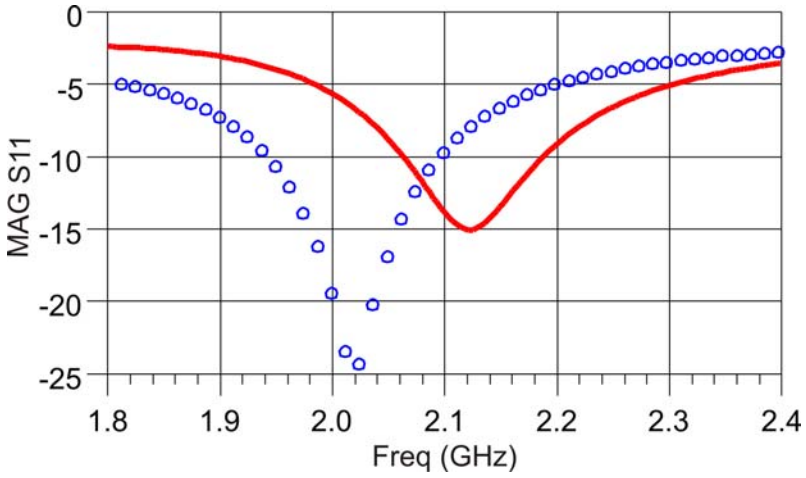
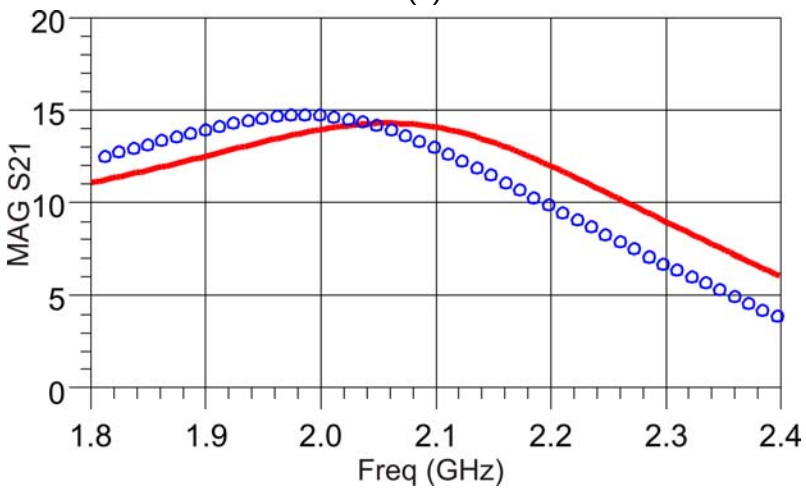


Figure D.1 Power amplifier designed using the one-step conventional design approach.

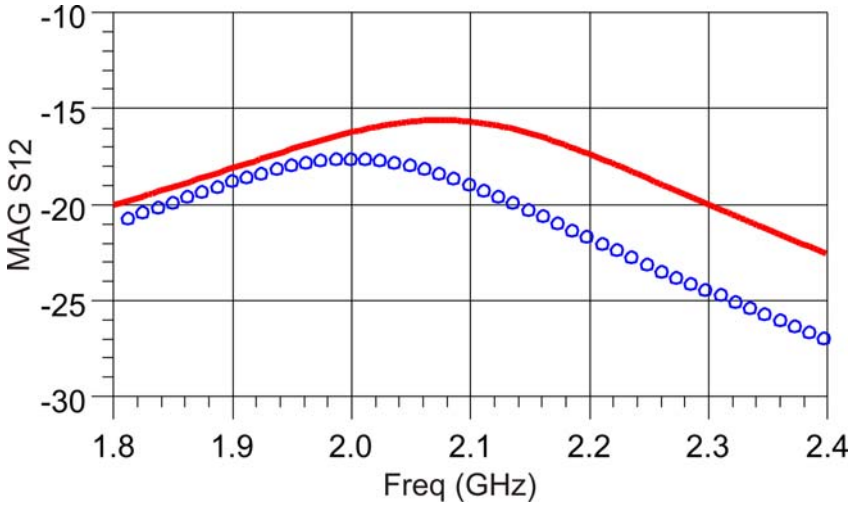
Then, both small-signal and large-signal measurements of the designed power amplifier have been performed. The simulation and the initial measurement results are compared.



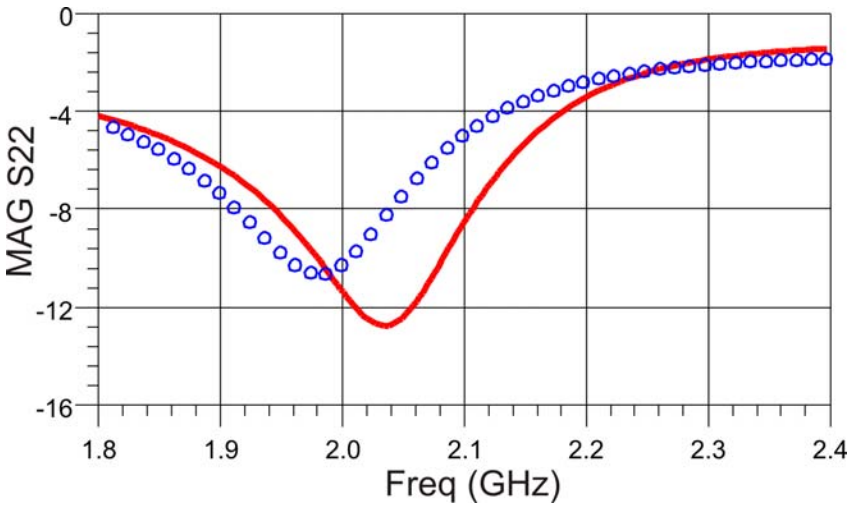
(a)



(b)



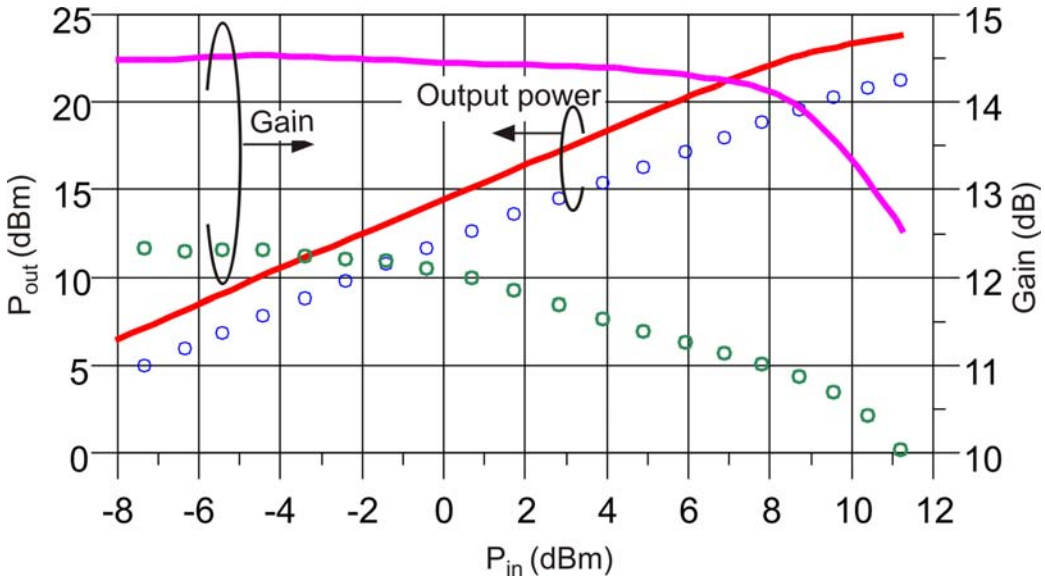
(c)



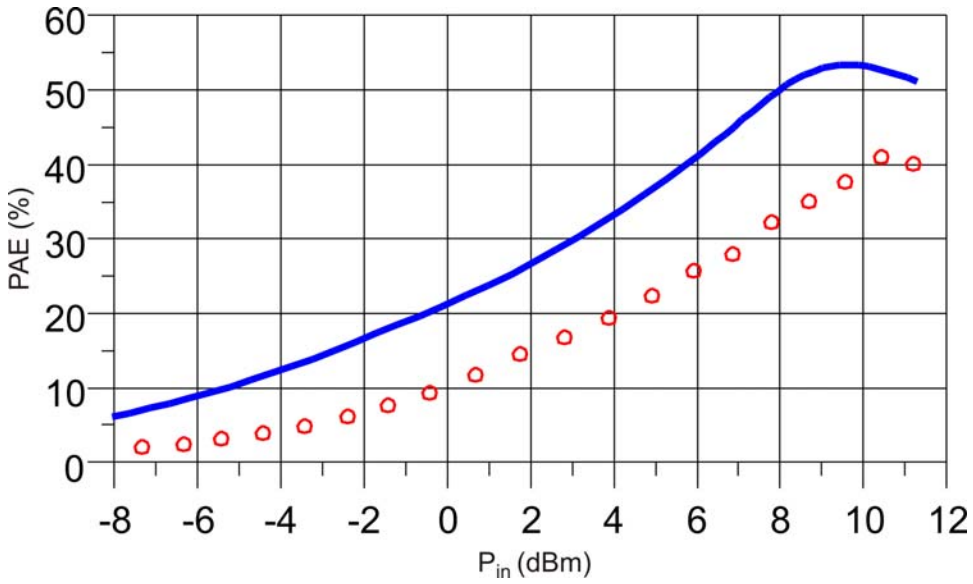
(d)

Figure D.2 S-parameter comparison of simulation (solid lines) and measurement of the fabricated power amplifier following conventional design approach (symbols): (a) magnitude of S11, (b) magnitude of S21, (c) magnitude of S12, and (d) magnitude of S22.

Even though bonding parasitic effects have already been roughly estimated in the initial design phase (0.5 nH bond wire inductance for gate and drain pad-to-microstrip connection estimated initially, perfect grounding assumed for source connection), it can be clearly seen from Figure D.2 that the real small-signal operating frequency in the measurement is shifted to 2 GHz, which is achieved at 2.1 GHz in simulation. Also, the input match is shifted from 2.14 GHz (in simulation) to 2.02 GHz (in measurement).



(a)



(b)

Figure D.3 Comparison of the large-signal single-tone power sweep between simulation (solid lines) and measurement (symbols) of the final power amplifier: (a) output fundamental power and gain, and (b) power added efficiency at 2.14 GHz (biased at V_{GS0} = -2.1V and V_{DS0} = 9V).

The large signal performance of final fabricated power amplifier is compared with the simulation under single tone stimulus in Figure D.3. It can be seen that the measured output power is approximately 2-3 dB lower than the simulated one. Also, the simulated gain curve shows a P_{1dB} value at an input power of 10 dBm, whereas it occurs in measurement for an input power of 4 dBm. Furthermore, PAE differs more than 15% over the entire power range. In conclusion, the results show that acceptable agreement between the initial fabricated power amplifier and simulation could not be obtained. Hence, this discrepancy motivates the application of the novel straightforward design approach for obtaining reliable RF power amplifier design.

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