

Condenser microphone uses dc-coupled impedance converter

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The diaphragm of a condenser microphone is the movable plate of a capacitor. With a polarized capacitor, the vibration of the diaphragm in relation to the back plate produces an ac audio-output voltage. The condenser capsule has a capacitance of 10 to 60 pF; thus, you should connect it to an impedance converter with extremely high input impedance for a flat frequency response.

The conventional impedance con-

verter is a JFET source follower with an additional amplifying and power-decoupling circuit. You supply power to the impedance-converter circuitry using the same microphone-cable conductors that carry the audio signal. The balanced audio pair at the XLR connector's pins 2 and 3 both carry the same positive dc voltage, or phantom power, relative to Pin 1's ground. The amplifying/decoupling circuit contains an audio transformer

DI's Inside

43 Simple sawtooth generator operates at high frequency

46 Dual regulator handles two input voltages

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or a couple of capacitors to separate the dc power from the audio signal.

High-value dc-blocking capacitors can generate measurable and audible distortion (Reference 1). Microphone

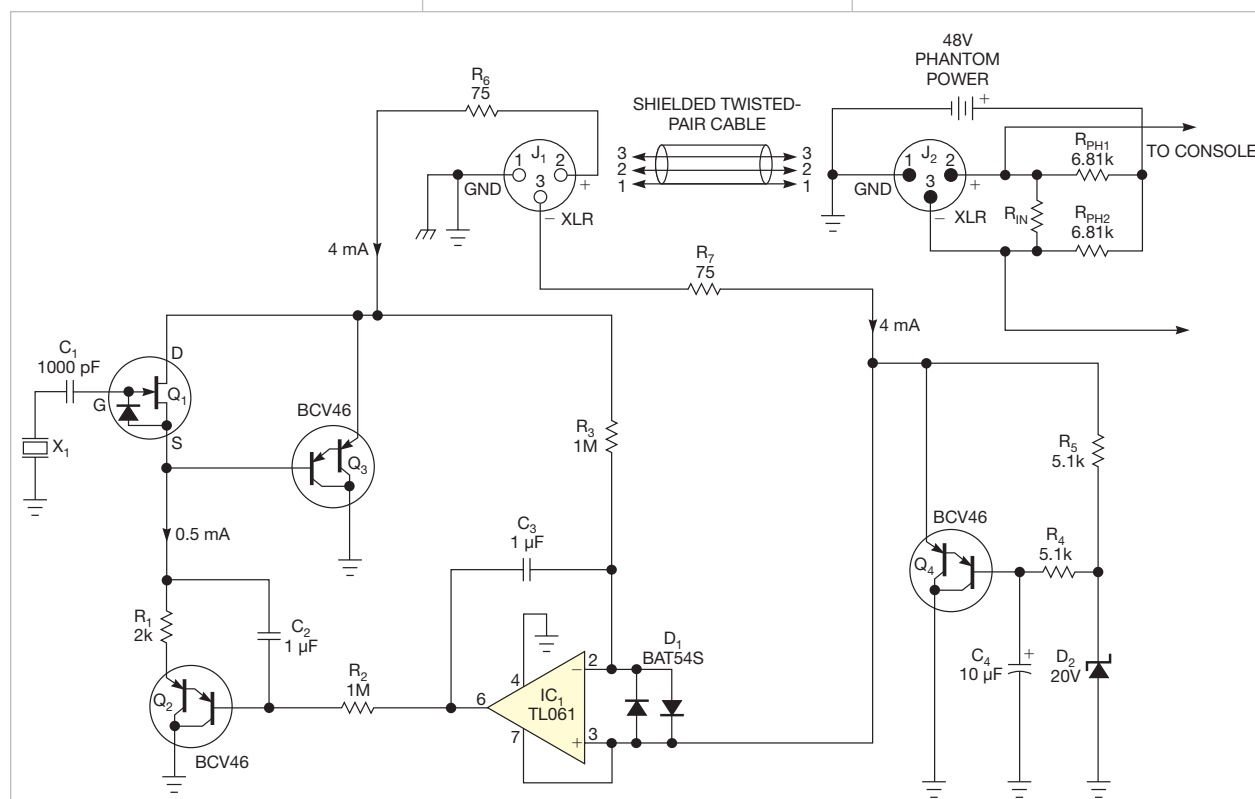


Figure 1 A feedback loop balances the dc voltage on the paired cable conductors, which power high- to low-impedance converter Q_1 .

circuits rarely use the highest-quality capacitors because of space limitations. You can design the impedance converter without dc-blocking capacitors.

Figure 1 shows the self-balanced impedance converter. The self-polarized electret condenser-microphone capsule, X_1 , connects to the high-impedance gate of JFET Q_1 . Q_2 , an ac-current source, loads source follower Q_1 . Q_2 , thanks to C_2 , has high impedance but allows a fixed dc voltage on the Q_1 source.

The circuit sources phantom power at 48V dc through R_{PH1} and R_{PH2} at the mixing-console end of the microphone cable. Q_2 's emitter drives—and R_{PH1} loads—emitter follower Q_3 . The signal from Q_3 's emitter bootstraps the

TABLE 1 PERFORMANCE PARAMETERS

Mixing-console input impedance R_{IN} (k Ω)	Peak input clipping voltage (V)	Input voltage at –80-dB (0.01%) distortion
1.2	3.1	140 mV rms
2.4	5.8	750 mV rms
10	13.6	3.1V rms

drain of Q_1 , reducing the ac voltage across the gate-to-drain capacitance and resulting in lower input capacitance at the gate of Q_1 . R_{PH2} supplies current for shunt-regulator-voltage sources D_2 and Q_4 . R_4 and C_4 attenuate zener-diode noise. Integrator IC_1 compares the dc voltages on the XLR connector's pins 2 and 3 and, through Q_2 and Q_3 , maintains a difference

TABLE 2 PERFORMANCE PARAMETERS FOR JFETs

Q_1 part	A-weighted noise voltage (μ V rms)
2SK596	4
2SK660	3.6
2SK2219	4.1
TF202C	4.6

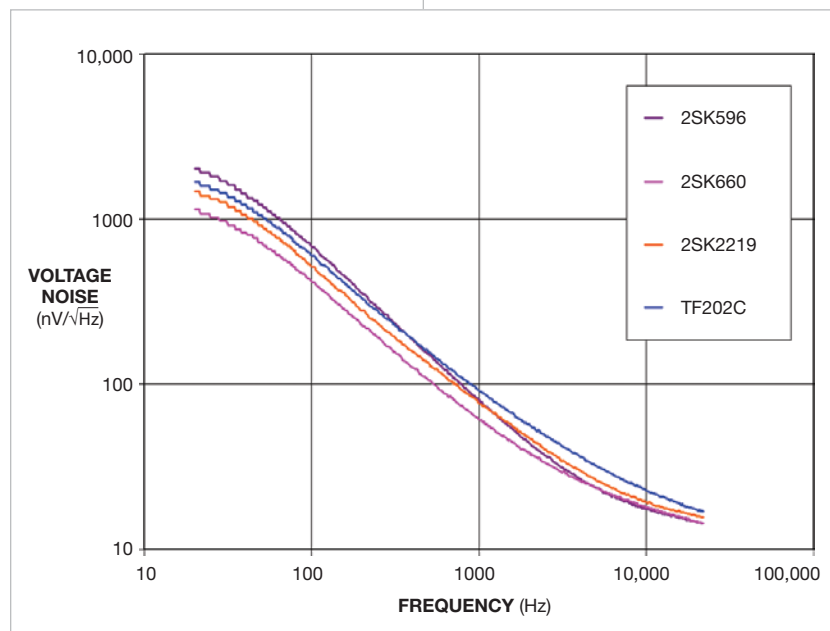


Figure 2 The voltage-noise density versus frequency for the circuit of **Figure 1** varies with different types of input JFET Q_1 . The source impedance of X_1 is 10 pF.

equal to the op amp's input offset voltage. Thus, if the microphone input at the mixer console is transformer-coupled, both ends of its winding are at the same voltage. No dc will flow through the winding and saturate the core. IC_1 should have a common-mode-input-voltage range equal to that of the positive-supply rail. You can accomplish this task using, for example, an op amp with a P-channel JFET input stage. **Tables 1** and **2** and **Figure 2** show typical performance parameters for the impedance converter in **Figure 1**. **EDN**

REFERENCE

1 Gaskell, Robert-Eric, "Capacitor 'Sound' in Microphone Preamplifier DC Blocking and HPF Applications: Comparing Measurements to Listening Tests," Audio Engineering Society, Presentation 130, Paper 8350, May 2011, pg 1, <http://bit.ly/zVcgtc>.

Simple sawtooth generator operates at high frequency

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➡ Pulse-width-modulation signal-generator circuits often use an analog sawtooth-oscillator function, but it also can be useful in other applica-

tions. The inexpensive sawtooth generator in **Figure 1** suits use in low-power applications operating at frequencies as high as 10 MHz and beyond and

those in which ramp linearity and frequency accuracy are not prominent concerns.

The circuit employs a single Schmitt-trigger inverter, which acts as a modified astable multivibrator. The output waveform is the voltage across timing capacitor C_T , which ramps between the lower and the upper threshold voltages of the

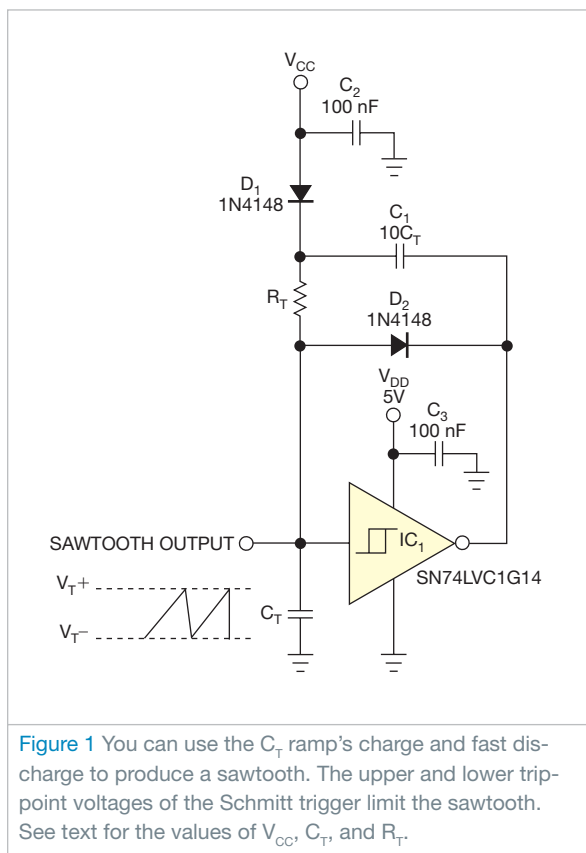


Figure 1 You can use the C_T ramp's charge and fast discharge to produce a sawtooth. The upper and lower trip-point voltages of the Schmitt trigger limit the sawtooth. See text for the values of V_{CC} , C_T , and R_T .

TO IMPROVE FREQUENCY ACCURACY, USE A FAST LOGIC FAMILY WITH LOW PROPAGATION DELAY AND HIGH OUTPUT CURRENT.

inverter. Charging the $R_T C_T$ network at constant voltage causes the ramp, so its response is exponential, approximately linear only for the initial part of the exponential rise.

A simple trick to improve ramp linearity is to charge the $R_T C_T$ network with a higher-voltage source. Capacitor C_1 , which has a value that is at least 10 times greater than that of C_T , acts as a charge pump. When the gate output is low during the falling edge of the sawtooth, capacitor C_1 quickly charges through diode D_1 to V_{CC} minus the for-

ward voltage of D_1 . Meanwhile, capacitor C_T discharges quickly through diode D_2 .

When the falling C_T voltage reaches the Schmitt trigger's lower trip point, V_{T-} , the gate output returns high. The charge on C_1 drives the cathode of D_1 to the sum of the voltage of capacitor C_1 and the gate's high output voltage. D_1 becomes reverse-biased, and the $R_T C_T$ network begins to charge to the voltage on C_1 , along with the gate's high output voltage. When C_T reaches the Schmitt trigger's upper trip point, V_{T+} , the gate's output returns low, and the cycle repeats.

Ramp linearity is proportional to the sum of the V_{CC} and V_{DD} supply voltages. Because V_{DD} is fixed at 5V, you can improve ramp linearity if V_{CC} can assume a value higher than that of the inverter. You can estimate the ramp's nonlinearity error using the following equation:

$$E_{NL}\% = \left(\frac{M_I - M_F}{M_I} \right) 100,$$

where $E_{NL}\%$ is the percentage of nonlinearity error, M_I is the initial slope of the ramp, and M_F is the final slope of the ramp, and

$$E_{NL}\% = \left(\frac{V_{T-}^+ - V_{T-}^-}{V_{CC} + V_{DD} - V_F - V_{T-}^-} \right) 100,$$

where V_F is the forward-voltage drop across D_1 .

The $R_T C_T$ time constant sets the frequency, F_O , of the sawtooth signal. You can estimate the frequency by applying a simple model to the circuit, which neglects the discharge time of C_T and any discharge of C_1 , yielding

the following equation:

$$F_O = \frac{1}{K R_T C_T},$$

where K is a constant, which the following equation defines:

$$K = \ln \left(\frac{V_{CC} + V_{DD} - V_F - V_{T-}}{V_{CC} + V_{DD} - V_F - V_{T+}} \right).$$

By simulating the circuit with $C_T = 100$ pF and $R_T = 2.2$ k Ω , which agree with the values that the equations theoretically calculated, you can obtain ramp-nonlinearity errors of 28% with both V_{CC} and V_{DD} equal to 5V, 18% with V_{CC} of 10V and V_{DD} of 5V, and 14% with V_{CC} of 15V and V_{DD} of 5V.

The breadboarded circuit has $V_{DD} = V_{CC} = 5V$, $C_T = 100$ pF, and $R_T = 2.2$ k Ω . IC₁ is a standard dual-in-line, eight-pin 74HC14, which has a maximum propagation delay of 15 nsec versus 4.4 nsec for the SN74LVC1G14 inverter with a V_{DD} of 5V. The frequency is approximately 12.7 MHz.


C_T should be a low-leakage film capacitor, and its value should be kept low to reduce its charging and discharging of a large amount of energy. Select C_T with a large enough value compared with the gate's input capacitance and unwanted stray capacitances so that they do not introduce a significant error. Select R_T with a small enough value that the load impedance, gate input, and stray capacitances do not introduce significant error. You can use any CMOS Schmitt-trigger inverter to test the circuit. To improve frequency accuracy, however, you should use a fast logic family with low propagation delay and high output current, such as the single-gate SN74LVC1G14 from Texas Instruments.

You should measure the threshold trigger voltages, especially V_{T-} , directly from the circuit under test before using the preceding equations. Quickly discharging C_T to ground through a finite-propagation-delay inverter causes the lower limit of the ramp to reset below the lower threshold, V_{T-} . You can compensate for the resulting error if you use the measured value of V_{T-} , which takes this effect into account. **EDN**

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Dual regulator handles two input voltages

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 The circuit in **Fig 1** supplies both 3.3 and 5V to transitional circuits that employ both the new 3.3V and older 5V devices. Additionally, because the regulator accepts either 3.3 or 5V inputs, you could plug it into either a new 3.3V system or an old 5V system.

The circuit consists of two sections: a dc/dc converter and a double-pole, double-throw (dpdt) switch. The dpdt switch comprises a pair of dual n-channel MOSFETs (Q_2 and Q_3) and their associated high-side drivers.

Upon power-up, the comparator in IC₂ determines the state of the circuit. The comparator's output, IC₂ pin 6, goes to the input of the MOSFET driver, IC₁. The driver internally generates a gate-drive voltage 8.8V above the device's

supply voltage. This high voltage drives the appropriate MOSFETs in Q_2 and Q_3 .

IC₂ is also the heart of a flying-capacitor, buck/boost dc/dc converter. Unlike other switching-regulator schemes, this topology needs no transformers. Transistor Q₁ controls this section's output voltage, V_S. When V_{IN} is at 5V, Q₁ is off, forcing the section to operate as a step-down converter. In this mode, the section produces 3.3V, which goes to the output through Q_{3B}. Also in this mode, 5V power goes directly through Q_{2A}, and Q_{3A} and Q₄ are both off.

When V_{IN} is 3.3V, IC₁ turns on Q₁, shorting out the 140-k Ω resistor and forcing the dc/dc-converter section into step-up mode. In this mode the converter section generates 5V at V_o, powering the 5V

output via Q_{2B} . Also in this mode, 3.3V goes directly from the circuit's input to the output via Q_{3A} . Q_{2A} and Q_{3B} are both off.

No-load quiescent current consumption is approximately 500 μA . Lower-frequency converters would reduce power consumption at the expense of a larger inductor. The efficiency of the dc/dc-converter section is 73% in either mode. But because this power accounts for only half of the circuit's output power, the circuit's overall efficiency is approximately 80% with $V_{\text{IN}}=3.3\text{V}$ and 86% with $V_{\text{IN}}=5\text{V}$. **EDN**

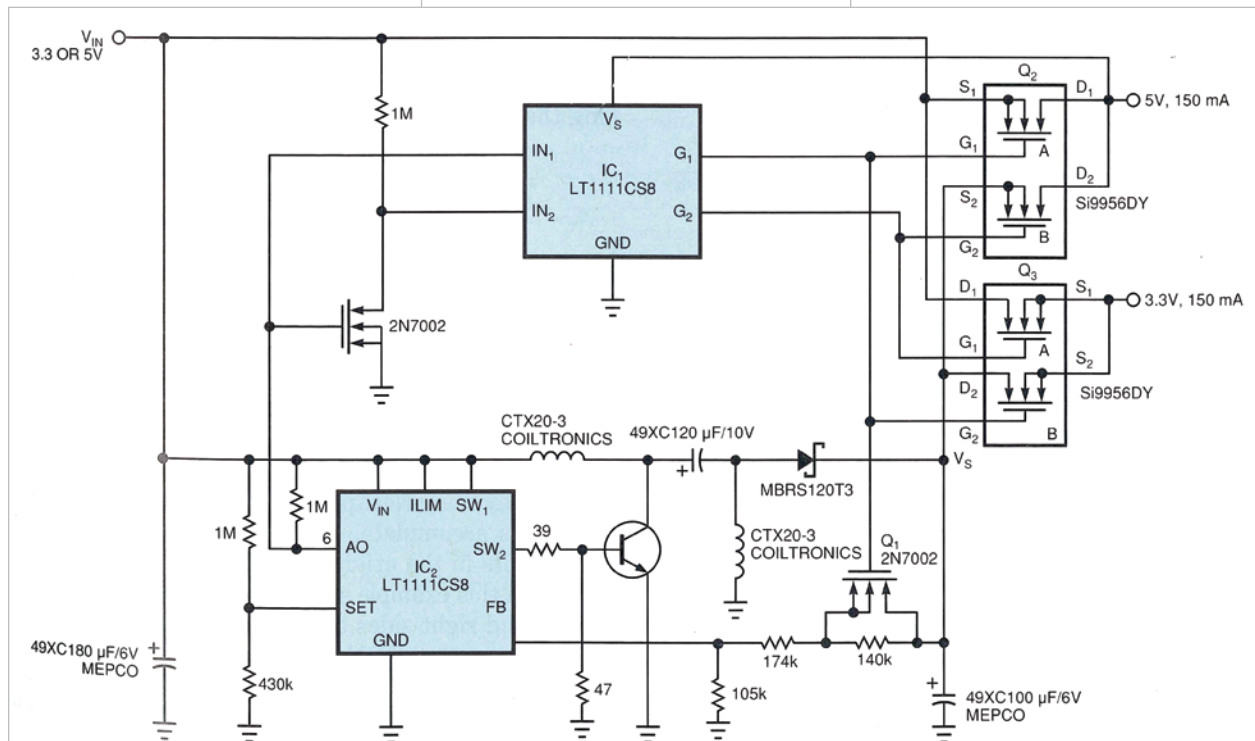


Figure 1 During the transition from 5V components to 3.3V components, dual-output regulators such as this one will let engineers design surface-mount pc boards bearing both 3.3 and 5V devices. Further, this novel regulator will accept either 3.3 or 5V input power.