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Ultra-Low Voltage Push-Pull Converter for Micro Energy Harvesting

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***Abstract*—Ultra-low power electronic devices, as by the way of example sensor nodes, can be powered by environmental energy harvesting. Thermo generators, solar cells, inductive generators, or radio frequency antennas provide an extremely low output voltage that must be amplified to generate a suitable power supply. This work presents an autonomous self-starting ultra-low voltage DC-DC converter that starts operations at 9 mV. The circuit is inspired by the classical zero voltage switching push-pull Royer oscillator, suitably modified by using JFETs to operate at low voltages. Thanks to the soft switching of the transistors and to the symmetrical use of the transformer, it can reach high voltage gain, high frequency, and high efficiency. Theoretical and simulation-based optimizations were used to design the converter; the results were experimentally verified with several prototypes.**

***Index Terms*— Boost converter, energy harvesting, low input voltage, push-pull, soft switching, high efficiency**

I. Introduction

ENERGY harvesting is getting more and more interesting for wireless sensor applications in embedded systems, health monitoring, civil engineering structures, automotive, aircraft monitoring, hazardous environments, etc. [1-3]. Very low amounts of energy are collected from the environment using small transducers and used to feed low power circuits such as autonomous sensors. Energy can be collected from several environmental sources [1]: solar, organic, vibrations, thermal, electromagnetic field (both near and far-field at radiofrequency). One of the eco-friendliest energy sources, the thermal energy, can be converted into electric energy via Seebeck effect. Miniaturized thermoelectric generator (TEG) devices have been successfully fabricated and applied to small-scale thermal energy harvesting applications. However, due to the physical dimension and temperature gradient limitations, the induced voltage level is rather low in the range of 50mV/K - 100mV/K [4]. A voltage level of at least 1 volt is required to supply conventional electronic circuits as, by the way of example, wireless sensors for internet-of-things applications. Efficient converters are required to transform the low input voltage to a level suitable for typical electronic devices, 1-5 V. In principle, the input voltage can be boosted using conventional DC-DC converters, but, again, DC-DC converters need power to start-up. Hence, self-starting ultra-low voltage boost converter architectures are required. Several autonomous self-oscillating low-voltage low-power DC-DC converters have emerged in recent years both from industrial and academic research [5-7]: almost all of them are based on the classical Armstrong oscillator. Aim of this work is to demonstrate for the first time, at least in the author knowledge, that the Royer oscillator [8] can be modified with normally-on JFETs switches to start at ultra-low input voltages. Although the Royer oscillator, based on BJTs and MOSFETs, is widely used in high efficiency push-pull power converters [8], it is not used in low voltage applications because of the positive device threshold. The advantage with respect to the Armstrong oscillator is that the Royer oscillator is symmetric, it maximizes the use of the magnetic core, and can be exploited in zero-voltage switching (ZVS) push-pull converters. ZVS is the key to maximize the power conversion efficiency η. Furthermore, thanks to the negative threshold of JFETs, the oscillation at ultra-low input voltages is nearly sinusoidal.

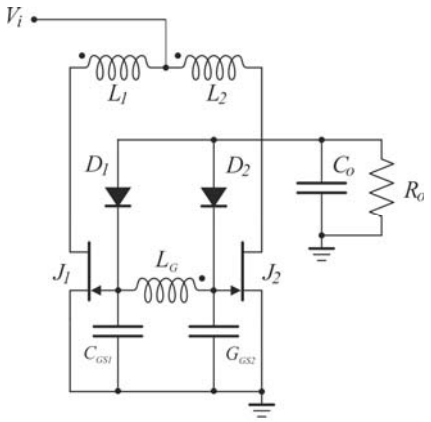

Fig. 1. Non isolated push-pull boost converter.

II. Operating Principle

The Royer oscillator is a relaxation oscillator based on a center-tapped transformer. It has the advantages of simplicity, low component count, easy transformer isolation, maximum use of the core and, in turn, reduced size and weight of the transformer. The output of the classic Royer circuit is a square wave, nevertheless it can be modified by adding a resonant capacitor to turn into a harmonic oscillator. The circuit consists of a transformer with a center-tapped primary winding L_1, L_2, a feedback winding L_G (Fig. 1) and (optionally) a secondary winding L_O (Fig. 2). The two halves of the primary are driven by two transistors in push-pull configuration. The feedback winding couples a small amount of the transformer flux back into the transistor's bases and

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provides a positive feedback that generates the oscillation. In order to design an ultra-low-voltage converter, here the bipolar transistors are replaced by normally-on JFETs (J_1, J_2) that are switched-off at negative gate voltage by the feed-back winding. A negative voltage large enough is achieved thanks to a large winding ratio in the transformer.

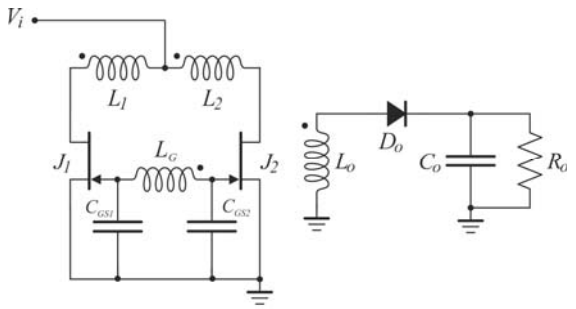

Fig. 2. Isolated push-pull boost converter.

At start-up, due to the ineliminable small differences of the two JFETs, one transistor tends to be more conductive, the feedback winding L_G accelerates the turn-on action, it switches-off the other transistor, and the oscillation gets started. Fig. 3 shows the simulations of the voltage and currents when the oscillation is stable. When the current is flowing in one leg of the circuit, for example through L_1, the voltage on the feedback winding L_G resonates with the gate capacitances and oscillates almost sinusoidally. The voltage on the gate of J_1 reaches its maximum and starts falling. On the contrary, the voltage on J_2 after reaching its minimum starts rising.

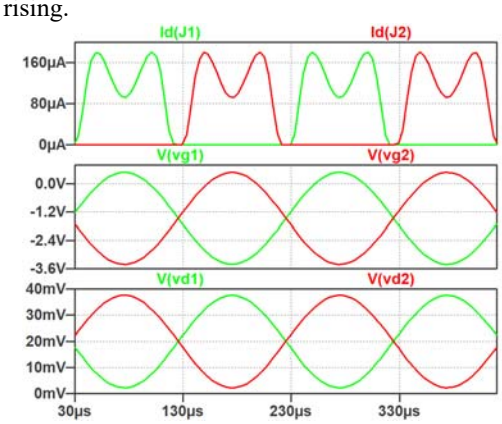

Fig. 3. Simulated voltage and currents in the converter (*Vi=20mV*): current in the inductor L_1 (green line) and L_2 (red line), gate voltage of J_1 (green line) and J_2 (red line), drain voltage of J_1 (green line) and J_2 (red line).

The transistor J_1 gets more and more resistive while J_2 gets more conductive, and the current is progressively diverted from L_1 to L_2. If the windings ratio is large, the gate voltage of J_1 gets negative enough to reach the gate-source cutoff voltage (V_P), J_1 turns-off, J_2 turns-on and the current is completely switched to L_2. The cycle is identical on the other leg (L_2, J_2), and the current is alternatively switched between L_1 and L_2.
The transistors J_1 and J_2, respectively, push and pull the two ends of the transformer with 50% duty cycle and the feedback winding L_G resonates with the gate capacitor C_{GS1} and C_{GS2} at constant frequency. The switching frequency depends on the power supply voltage, the inductance of the primary winding, the winding ratio n, the conductance and the gate capacitances of the JFETs. It can be accurately computed only by means of circuit simulations. Nevertheless, it can roughly be analytically evaluated by observing that when J_1 is switched-on, J_2 is switched-off and the current flows only in one leg of the circuit. In this half period the circuit is almost equivalent to an Armstrong oscillator. Same considerations hold for the other half period. Hence, the simplified equations of the Armstrong oscillator, slightly modified to account for the effect of two JFETs, can be used to evaluate at a glance the oscillation frequency [6].

$$f_o \cong \frac{1}{2\,\pi\, n \sqrt{L\, C_{GS}/2}} \qquad (1)$$

where $L = L_1 = L_2$, $n = \sqrt{L_G/L}$, and $C_{GS} = C_{GS1} = C_{GS2}$ the gate capacitances. It is worth noting that the JFETs, as in the conventional Royer oscillator, switch at almost zero voltage, that theoretically eliminates the losses due to the channel resistance and the parasitic device capacitances.

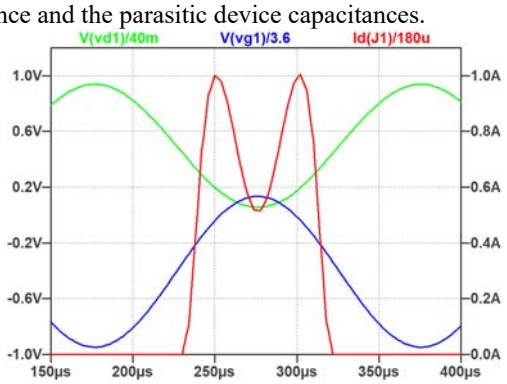

Fig. 4. Normalized voltage and currents on the switch J_1 (*Vi=20mV*): drain voltage (green line), gate voltage (blue line), drain current (red line, right tics).

In Fig. 4, the normalized drain and gate voltages of J_1, along with the drain current, are shown together. One can see that the drain voltage (switching voltage) increases, reaches its peak, and eventually drops down to zero: here the gate voltage gets larger than the cut-off voltage (V_P is negative) and the switch is turned on. The JFET turns on at nearly zero-voltage and zero-current. Then the current through L_1 increases, draws energy from the input, and eventually turns-off at nearly zero drain voltage and zero current. Therefore, the JFET losses approach zero regardless the operating frequency. Although the input voltage is extremely low, it is the key to minimize the power dissipation, and to maximize the efficiency. One of the most relevant sources of losses, indeed, is the JFETs on-resistance that is inherently high in order to have low cutoff voltage (i. e. the channel is lightly doped). On the other hand, the low cut-off voltage and the low zero gate voltage current (I_{DSS}) are essential to trigger the start-up oscillations. Furthermore, in this converter, thanks to the resonance between the transformer and the gate capacitances, when the current flows in the JFETs the drain voltage V_{DS} is around the minimum of the sinusoidal waveform (Fig. 4). It further increases the overall efficiency because to trigger the

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oscillation the resistance must be of several Ohms. Finally, J_1 and J_2 push and pull the current at the two ends of the transformer and periodically reverse its current. It prevents the saturation of the core material: hence, high frequency, very small transformers can be used. All these features make the converter a suitable candidate for efficient ultra-low voltage energy harvesting systems.

III. Converter Start-up

The converter is based on a modified Royer oscillator connected to a full wave diode rectifier (non-isolated topology), or to an output winding (isolated topology). For the sake of simplicity, in order to investigate the converter start-up process, we discuss only the oscillator start-up. The approximation is justified by Fig. 5 that shows as the current flows to the load only for a very small amount of time each half wave; in the rest of the period the oscillator is virtually disconnected. In the oscillator's theory, there are some conditions that guarantee the oscillation start-up.

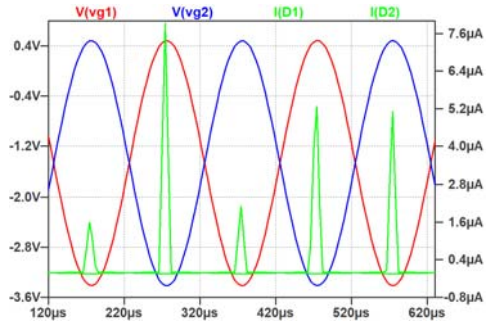

Fig. 5. Current on the output diodes (*Vi=20mV*) green lines. Gate voltages of J_1 and J_2 red and blue lines respectively.

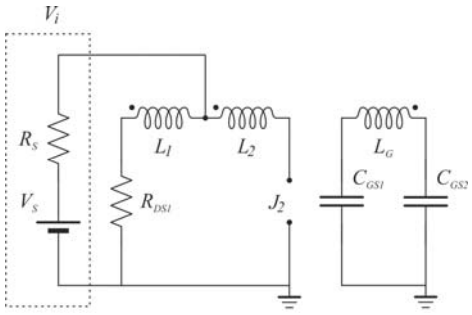

Fig. 6. Equivalent circuit of the oscillator in the half period when J_1 is turned-on. Same considerations hold in the other half period.

Those conditions can be analytically estimated assuming the following approximations [6]: we consider the oscillator disconnected from the load, the input source is a voltage generator (V_S) in series with its internal impedance (R_S), the JFET and the transformer parasitic capacitances are reported at the JFETs gates. Besides, we assume: no magnetic loss in the transformer (coupling factor k = 1), negligible winding resistances with respect to R_S, the JFETs operate in the linear region. Hence, the drain current can be expressed as

$$I_D = \frac{2\,I_{DSS}}{V_P^2}\left(V_{GS} - V_P - \frac{V_{DS}}{2}\right) V_{DS} \qquad (2)$$

Under these conditions the differential equation of the gate voltage is analogous to that of [6], slightly modified to account for two gate capacitances in series to L_G

$$\frac{d^2\,V_{GS}}{dt^2} + 2\,\lambda\frac{d\,V_{GS}}{dt} + \omega_0\,V_{GS} = 0 \qquad (3)$$

were

$$\lambda = \frac{\dfrac{V_P^2}{2\,I_{DSS}(V_{GS}-V_P)} + R_S}{n} - \frac{V_P^2\left(V_S - \dfrac{V_{GS}}{n}\right)}{2\,I_{DSS}(V_{GS}-V_P)^2} \qquad (4)$$
$$n\,C_{GS}\left(\dfrac{V_P^2}{2\,I_{DSS}(V_{GS}-V_P)} + R_S\right)^2$$

λ is the damping factor, $\omega_0 = 2\pi f_0$ the resonance pulsation. It is a nonlinear second order differential equation that cannot be solved analytically since λ is function of V_{GS}. Nevertheless, although simplified, two important equations can be worked out following the approach of [6]:

$$V_{Smin} > \frac{2\left(n+\frac{1}{2}\right)I_{DSS}\,R_S - (n+1)V_P}{2(n+1)^2} \cong \frac{I_{DSS}\,R_S + |V_P|}{2\,n} \qquad (5)$$

$$n_{min} > \frac{1}{\left(\dfrac{V_S}{2\,I_{DSS}R_S - V_P}\right) - \sqrt{\dfrac{C_{GS}}{2L}}\,\dfrac{2\,I_{DSS}R_S - V_P}{I_{DSS}}} \qquad (6)$$

where V_{Smin} is the start-up voltage and n_{min} the minimum winding ratio to trigger the oscillation. One can see that a large number of windings leads to a low startup voltage: on the other hand, large n leads to high inductance losses and bulky transformers.

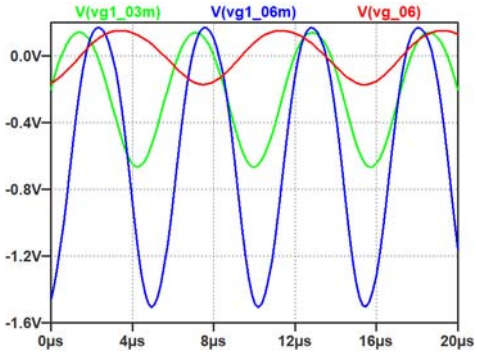

Fig. 7. Royer vs. Armstrong oscillator: green line Royer oscillator at *Vi*=3mV, blue line Royer oscillator at *Vi*=6mV, red line Armstrong oscillator at *Vi*=6mV. Simulation models and parameters are the same for both converters: JFETs BF862, diodes 1N4148, primary inductors 1µH, secondary inductors 100 mH, k = 0.98.

Furthermore, eq. (5) shows that, thanks to the series of C_{GS1} and C_{GS2}, the effect of the gate capacitance is halved with respect to the Armstrong oscillator and, at least theoretically, the minimum start-up voltage too. Simulations were carried out by means of the LTspice circuit simulator to validate the above equations. The theoretical and simulated minimum start-up voltages differ at most of 30% in a wide range of device parameters. Nevertheless, at very low input voltages the transformer losses become more and more relevant and the assumption of ideal transformer (k = 1) breaks down. Simulations with realistic models and $0.9 < k < 1$ show that the input voltage can be pushed down to 3 mV if the gate capacitance is small enough: in good accordance with (5) $V_{Smin} = (I_{DSS}\,R_S + |V_P|)/2n \cong 1.5\,mV$. Fig. 7 shows the

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simulations of the gate voltage oscillation of J_1 at V_i = 3mV and V_i = 6mV compared with the Armstrong oscillator. The Armstrong oscillator starts at 6 mV, its frequency is roughly one half, and the peak to peak amplitude is four times smaller.

IV. Experimental Results

Several prototypes were simulated, fabricated, and measured. The selection of each component and of the oscillation frequency is important to maximize the output voltage and the conversion efficiency. As stated above, a relevant source of losses is the JFETs on-resistance that is inherently high because of the low V_P and I_{DSS} required to trigger the start-up oscillations (eq. 5). A good compromise for our prototype is the JFETs PF5102 with V_P = - 0.7 V, I_{DSS} = 4 mA, C_{GS} = 9.56 pF. The transformer was fabricated on the cores KEMET ESD-R-47B and ESD-R-38B. The rectifier is based on the conventional low voltage 1N4148 diodes. Simulations were carried out by means of the LTspice.

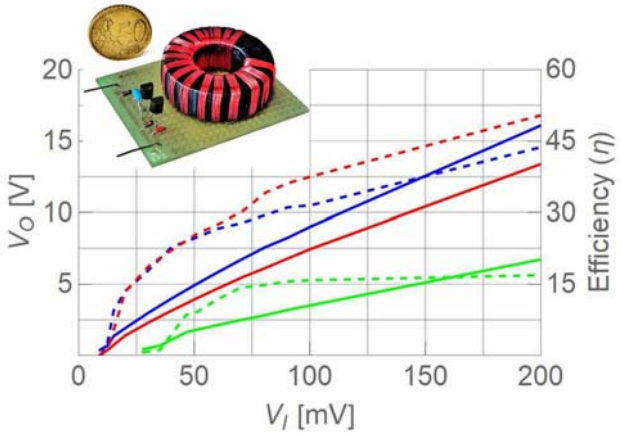

Fig. 8. Experimental results at ultra-low input voltages. Output voltage: circuit A blue solid line, circuit B red solid line, circuit C green solid line. Efficiency: circuit A blue dashed line, circuit B red dashed line, circuit C green dashed line. R_O = 3.3 MΩ, C_O = 10 nF. Inset: prototype A (Vo = 0.39V @ 9.21 mV, 1.83 V @ 20 mV, 4.97 V @ 50mV).

Three prototypes were first designed and optimized by means of simulations, then fabricated and measured:
A) non-isolated optimized at input voltages 20 mV (n = 240)
B) non-isolated optimized at input voltages 100 mV (n = 160)
C) isolated optimized at input voltages 100 mV (n = 160)
The input and output voltages were measured with a four channels oscilloscope Keysight DSOX3014A, the input voltage is generated with an adjustable low dropout regulator LT3083. The input current is inferred by sensing the DC voltage drop across a low tolerance small resistance (1 Ω) in series with the power generator: at very low voltage it is a relevant issue. We expect that the sensing of the input current via the resistance dropout influences negatively the oscillator and causes a higher start-up voltage. Hence, the measurements represent a worst case: we believe that the circuit can be even better than our measurements. Furthermore, the transformer of our first prototypes represents a weakness as well: it is handcrafted and, in order to accommodate the required windings, it results rather bulky and introduces relevant stray capacitances. It leads to considerable losses and, despite the core material could withstand higher frequencies (1 MHz), it limits the overall frequency. Nevertheless, simulations show that the converter, if the gate capacitance is as low as 1 pF (integrated circuits) and the input voltage is larger than 100mV the converter could operate at frequencies of about 1 MHz. In Fig. 8 the measured output voltages of the three prototypes are shown. One can see at a glance that the non-isolated topologies (A, B) start oscillating at about 10 mV, and the isolated one (C) at about 30mV due to the larger number of windings. It is worth mentioning that simulations can reproduce measurements only assuming low ideality factors k < 0.7, and accounting for the coils' serial resistances and stray capacitances. The measured voltage gain (G_V = V_O/V_I) of circuit A, by the way of example, is in the order of 100 (it varies with the input voltage) while in the simulations with better transformer parameters (k > 0.9) it is 160. It suggests that the transformer can be optimized with better cores, thinner wires, and accurate windings layout. Furthermore, the transformer losses explain the lower gain ($G_V \approx 40$) of the prototype C: the number of windings is roughly doubled as well as the parasitics. Nevertheless, despite the transformer requires optimizations, the converter shows a very high voltage gain: at 20 mV the measured output voltage is 1.7 V (3.3 V in the simulations), at 100 mV is 8.97 V (16 V in the simulations) and at 200 mV is 15.4 V (32 V in the simulations). The smallest measured start-up voltage is 9 mV (prototype A, optimized at 20 mV): at 10 mV the measured output voltage is 0.6 V (G_V = 60) and the simulated 3.38 V (G_V = 169). Low input voltage requires many feedback winding, large L_G and, in turn, lower frequencies (Eq. 1). Hence, to design a high gain, high frequency converter C_{GS} must be as small as possible. Fig. 8 also shows the efficiency η at low input voltages and power. The converter B is slightly more efficient than the converter A because of the smaller number of windings: η = 8% at 11 mV, up to 50 % at 200 mV and larger than 50 % for an input voltage in the range of 300-500 mV. Again, the simulated efficiency with realistic parameters is larger: above 50% for input voltages of 20-50 mv and larger than 70% at 50-200 mV. At low input voltages about 40% of the overall losses comes from the transformer series resistances and leakage inductances, 20% to the JFETs series resistance and 5% to the output diodes. The most relevant measured features of the converters at ultra-low input voltages (3.3 MΩ output load) are shown in Tab. 1. At larger output currents (R_O < 100 kΩ), as for the conventional Royer converter, the efficiency increases drastically, the transformer is smaller, while the startup voltage rises. It is worth noting that the Royer converter at high voltages easily exceeds η = 90%.

	Startup Voltage	Max. Frequency	Max. G_V	Max. η	Min. P_{IN}
A	9 mV	41.38 kHz	99	54.4 %	0.8 µW
B	10 mV	70.67 kHz	93	57.0 %	1.4 µW
C	28 mV	84.17 kHz	38	18.7 %	4.0 µW

Table 1. Measured main parameters of the three converters.

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Table II shows a performances comparison with the state-of-the-art integrated and discrete low-voltage and low-power converters. Our converter achieves the lowest start-up voltage (9 mV) except [14]*, where extremely low startup voltage (6 mV) is achieved by means of 7 cascaded transformers, a voltage multiplier, and Schottky diodes: it is an excellent result, but the efficiency is low (max. η = 8.2 %). The transient behavior of prototype A at startup and changing the load condition is shown in Fig. 9. Finally, energy-harvesting systems often include an energy-storage device to accumulate charge and supply a burst of current whenever it is required.

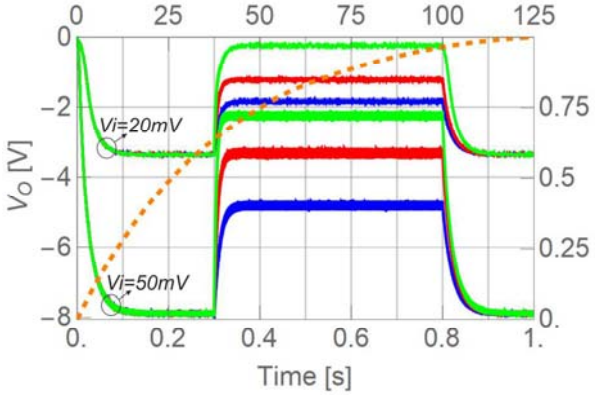

Fig. 9. Transient output voltage through light to heavy load conditions at 20 and 50 mV input voltage (bottom-left axes): 10 MΩ → 1 MΩ blue line, 10 MΩ → 470 kΩ red line, 10 MΩ → 330 kΩ green line. Charging time of a 4 µF capacitor (top-right axes) orange dashed line (conv. A).

To reproduce this condition a capacitor is connected to the converter at V_I =15 mV. In Fig. 9 the measured charging time is shown. The circuit can charge a 4 µF capacitor to 1V in 2 minutes and, more importantly, the oscillation starts despite the large conductance of the capacitor at 0 V.

Ref.	V_I at Startup	V_O at Startup	Min. Inp. Power	Max. Eff.	Prototype specs
[10]	80 mV	1.3 V	1.4 mW	60 %	Integrated
[11]	120 mV	1.2 V	880 µW	30 %	Part. Int.
[12]	140 mV	1.3 V	830 µW	20 %	Integrated
[13]	200 mV	2.5 V	5.8 mW	66 %	Discrete
[9]	100 mV	1 V	3 µW	25 %	Discrete
[14]	62 mV	N.A.	42.2 µW	N.A.	Discrete
[14]*	6 mV	0.1÷0.3 V	0.49 µW	8.2 %	Discrete
[15]**	20mV	1 V	2 µW	64 %	Integrated
[16]	15 mV	0.15 V	2 µW	1.7 %	Piezo trasf.
[17]	60 mV	1 V	N.A.	59 %	Part. Int.
[18]	70 mV	1.25 V	12 µW	60 %	Part. Int.
Our	9 mV	0.39 V	0.8 µW	57%	Discrete

Table 2. Comparison with the state-of-the-art low-voltage autonomous DC-DC converters. * Circuit [14] with 7 cascaded transformers with different output stages and loads. ** Not self-starting, it requires a battery of 600mV.

V. Conclusion

This work shows that the Royer converter, suitably modified with JFET switches, can be successfully used at ultra-low input voltages. It has the advantages of simplicity, zero voltage switching, maximum use of the magnetic core, and sinusoidal waveforms. It is the key to achieve high voltage gain, high efficiency, and low start-up voltages. The lowest measured start-up voltage is 9 mV although simulations show that, with careful optimization of the transformer and of the switching devices, it could start at voltages as low as 3 mV. At input voltages in the range of 200-300mV the output voltage exceeds 10V and the efficiency 50 %.

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