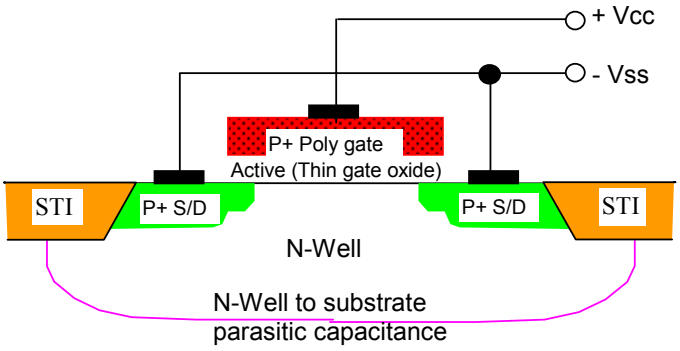
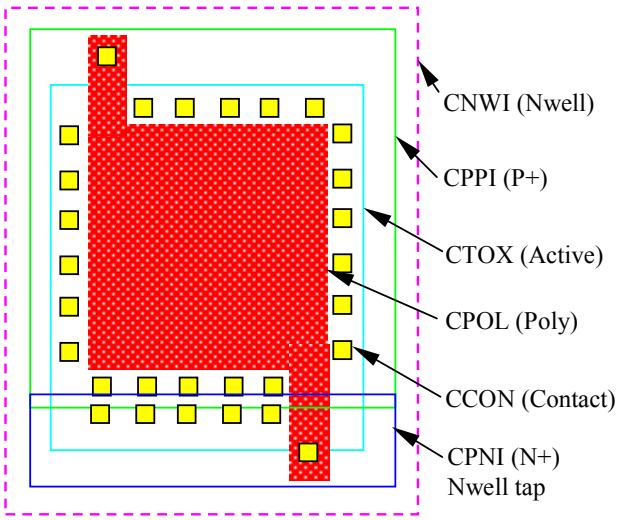
5. Thin oxide capacitors.

5.1: Pmos gate capacitors:

For a gate voltage in excess of the threshold voltage, a capacitor could by using a PMOS transistor with the source/drain region biased to the Nwell. It is recommended to use the high voltage PMOS (PMOSOX3) transistor.
New intrinsic capacitance model introduces in BSIM3V3.2 is used in the last release of spice model (R200 or higher). This model takes into account of poly gate depletion in the inversion region and quantum effect in the accumulation region. Accurate value of the capacitor could be obtained now by spice simulation.

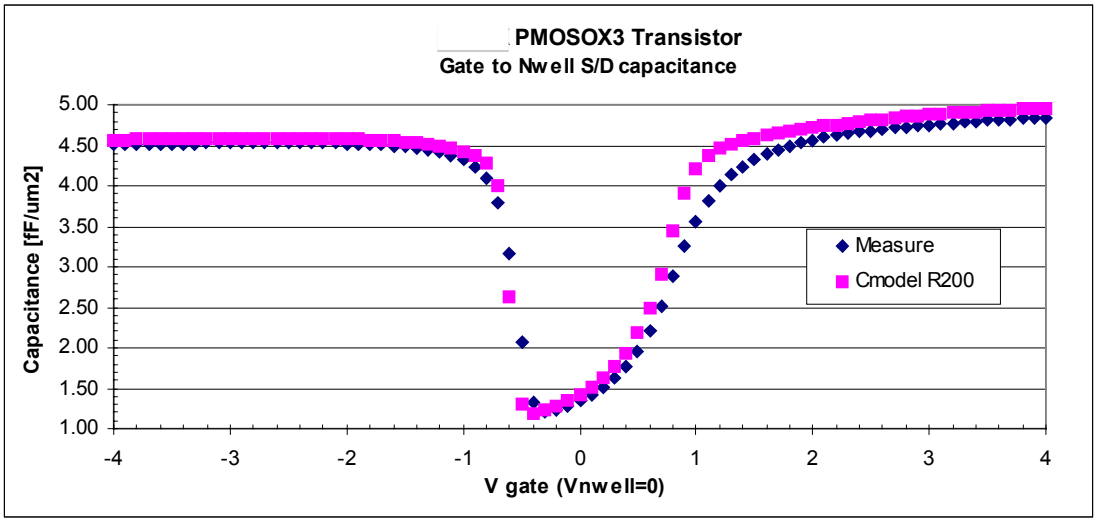




PMOSOX3, 3.3 Volt gate oxide:

Max Capacitance @27 °C @-3.3 V,	Typical:	4.6	fF/um2
	Specification:	[4.1, 5.1]	fF/um2
linearity coefficient @27 °C,	highly non linear, see graph hereafter.		

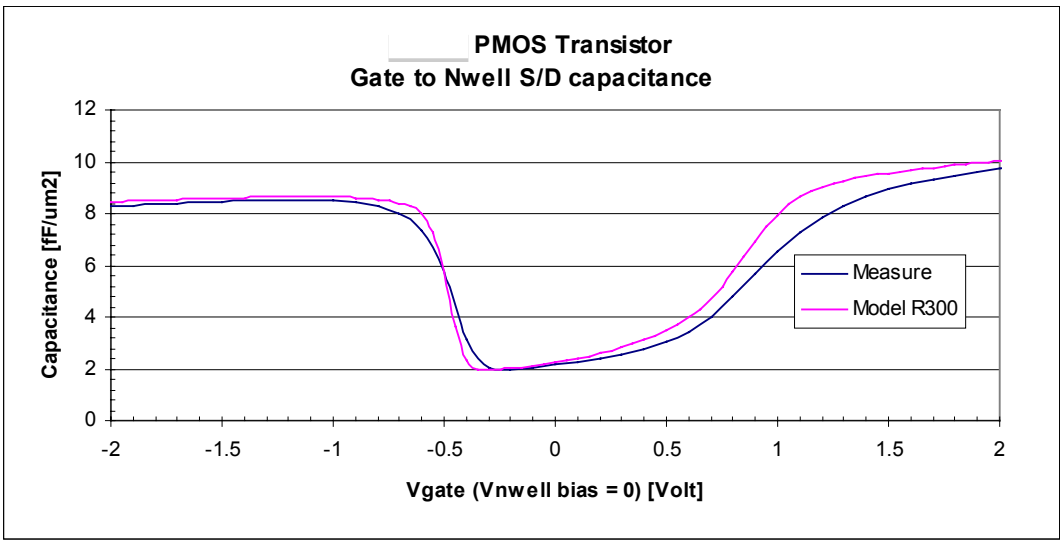
The plots 5.1a and 5.1b exhibits the difference between measurement and simulation:



5.1a: R200 Spice model Vs measurement PMOSOX3 gate oxide transistor

PMOS, 1.8 Volt gate oxide:

Max Capacitance @27 °C @1.8 V,	Typical:	8.5	fF/um2
	Specification:	[7.8, 9.2]	fF/um2
linearity coefficient @27 °C,	highly non linear, see graph hereafter.		



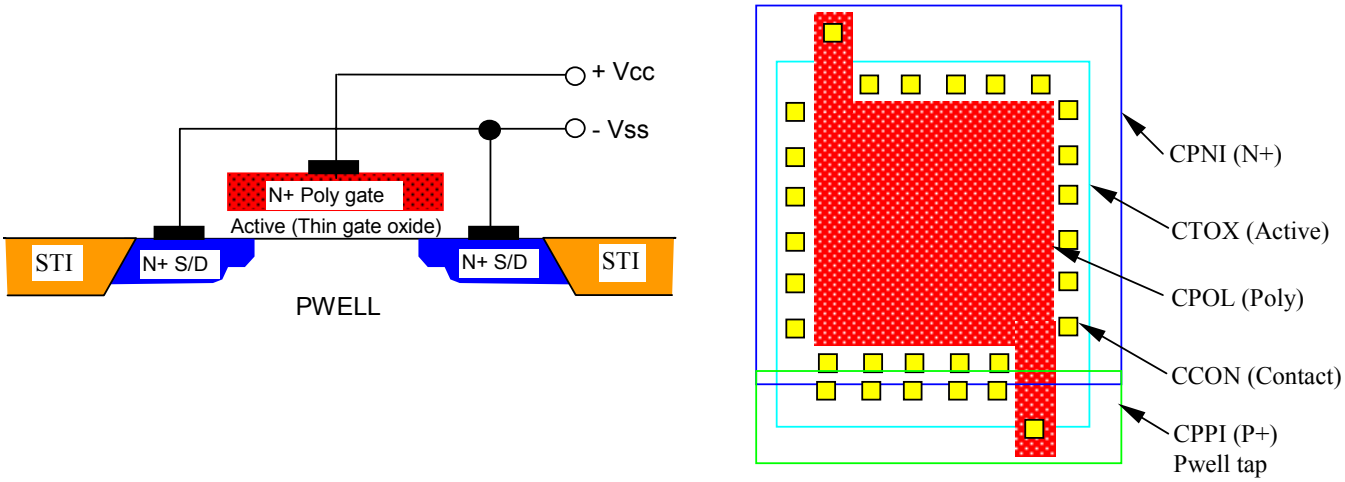
Plot 5.1b: R300 Spice model Vs measurement PMOS gate oxide transistor

The simulation have been conducted with the following net list (Hspice 2001.4):

```
**
.options post=1
.options co=240 ingold=2  numdgt=6  acct=0 dccap=1
*opts  itrprt brief nopage nomod

M1 1 2 0 3 pmos w=493 l=36 m=3

.temp=25
vds 1 0 dc 0
vgs 2 0 dc 0
vbs 3 0 dc 0
.dc vgs -2 2 0.05

.print dc lx18(m1)

.LIB                    process_tolerances              *
.LIB                    mos_nom                 *
.LIB                    techno                  *
.LIB                    nonmc                   *
.LIB                    nonmatching                     *
.LIB                    model_58k                       *
.LIB                    rhigh                   *
.LIB                    chigh                   *

.end
```

5.2: Nmos gate capacitors:

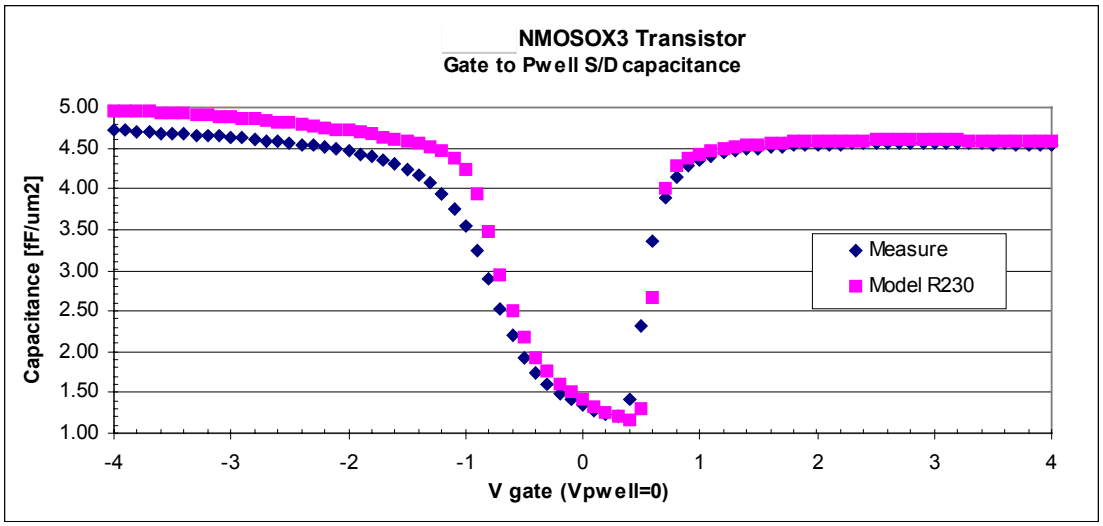
For a gate voltage in excess of the threshold voltage, a capacitor could by using a NMOS transistor with the source/drain region biased to the VSS. It is recommended to use the high voltage NMOS (NMOSOX3) transistor.
New intrinsic capacitance model introduces in BSIM3V3.2 is used in the last release of spice model (R200 or higher). This model takes into account of poly gate depletion in the inversion region and quantum effect in the accumulation region.
However, the best fit of the model is obtained in the inversion region. This is the normal polarization use of the N type MOS transistor and of the capacitor.



NMOSOX3, 3.3 Volt gate oxide:

Max Capacitance @27 °C @3.3 V,	Typical:	4.6	fF/um2
	Specification:	[4.1, 5.1]	fF/um2
linearity coefficient @27 °C,	highly non linear, see graph hereafter.		

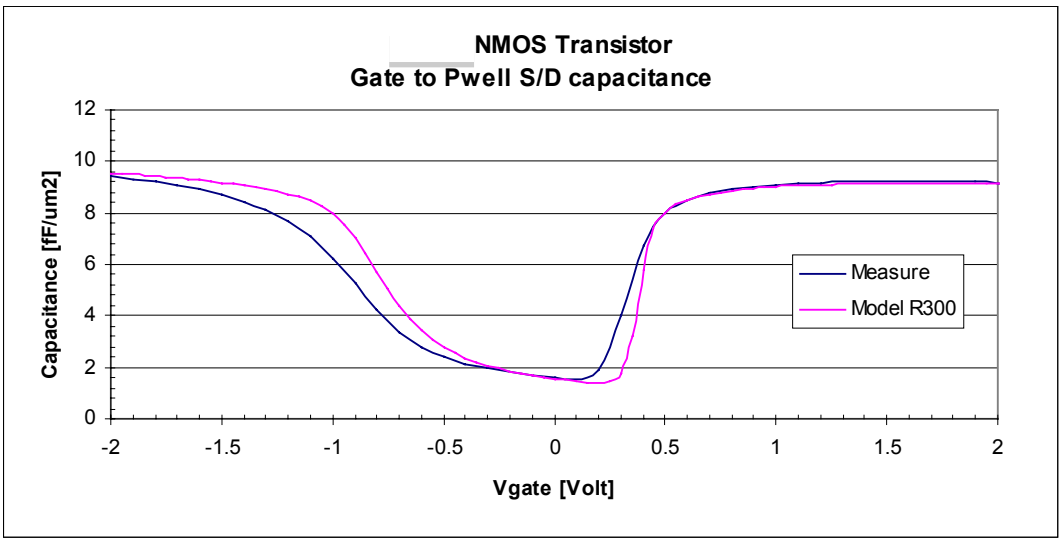
The plots 5.1a and 5.1b exhibits the difference between measurement and simulation:



5.1a: R230 HSpice model Vs measurement NMOSOX3 gate oxide transistor

NMOS, 1.8 Volt gate oxide:

Max Capacitance @27 °C @1.8 V,	Typical:	9.1	fF/um2
	Specification:	[8.4, 9.8]	fF/um2
linearity coefficient @27 °C,	highly non linear, see graph hereafter.		



Plot 5.1b: R300 HSpice model Vs measurement NMOS gate oxide transistor

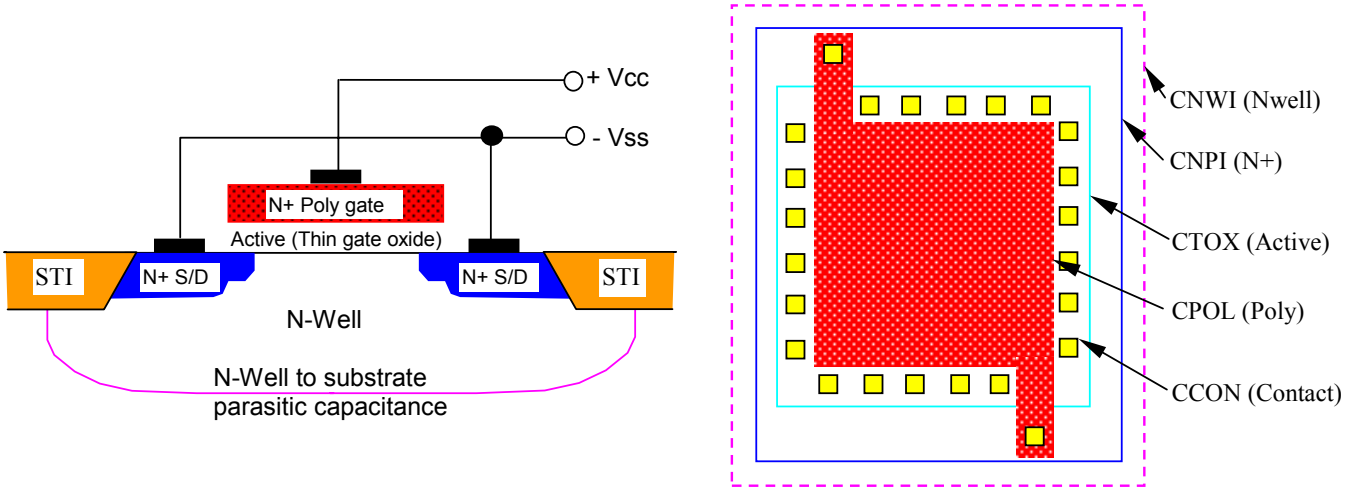
The simulation have been conducted with the following net list (Hspice 2001.4):

```
**
.options post=1
.options co=240 ingold=2  numdgt=6  acct=0 dccap=1
*opts  itrprt brief nopage nomod

M1 1 2 0 3 nmos w=493 l=36 m=3

.temp=25
vds 1 0 dc 0
vgs 2 0 dc 0
vbs 3 0 dc 0
.dc vgs -2 2 0.05

.print dc lx18(m1)

.LIB                    process_tolerances              *
.LIB                    mos_nom                 *
.LIB                    techno                  *
.LIB                    nonmc                   *
.LIB                    nonmatching                     *
.LIB                    model_58k                       *
.LIB                    rhigh                   *
.LIB                    chigh                   *

.end
```

5.3: N+ over Nwell gate capacitor:

This capacitor is done by N+ poly plate over gate oxide over Nwell. Due to the type of poly gate (N+) the Vt of this capacitor is shifted to -1.2 Volt.
A model has been created from the charge thickness capacitance equation described in the BSIM3V3.2 Berkeley manual. These models presented has a SUBCK are available in the release 200 (or higher) of the spice model:

CAP_ MOS: 1.8 Volt, 32Ang thin gate oxide
CAP_OX3: 3.3 Volt, 70Ang thick gate oxide

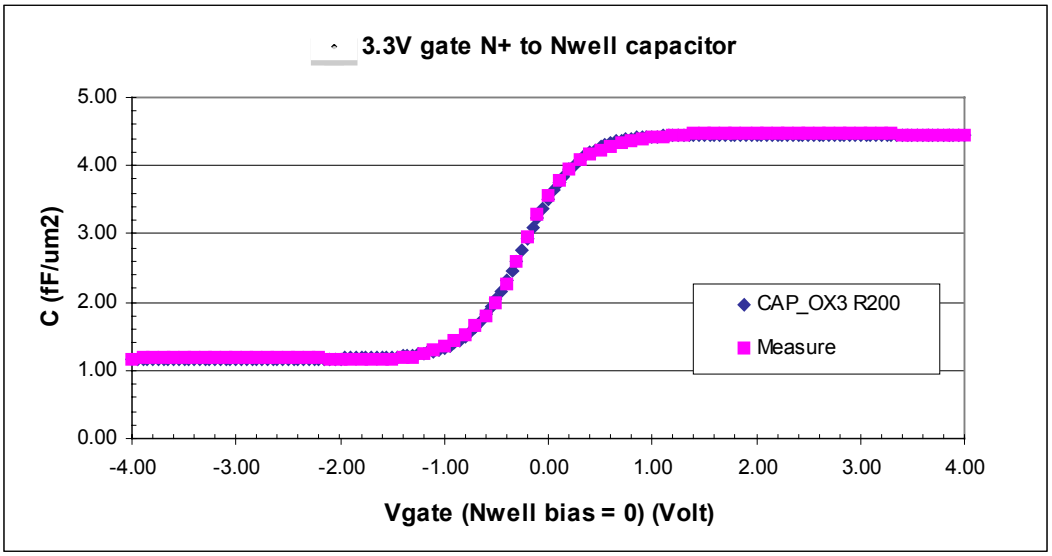


Depending of quantum effect in accumulation side of the PMOS capacitor, and of the depletion effect in the poly gate of the N+/Nwell capacitor, the typical value could be different.

CAP_OX3, 3.3 Volt gate oxide:

Max Capacitance @27 °C @3.3 V,	Typical:	4.5	fF/um2
	Specification:	[4, 5]	fF/um2
linearity coefficient @27 °C,	highly non linear, see graph hereafter.		

The plots 5.2a and 5.2b exhibit the difference between model and simulation:

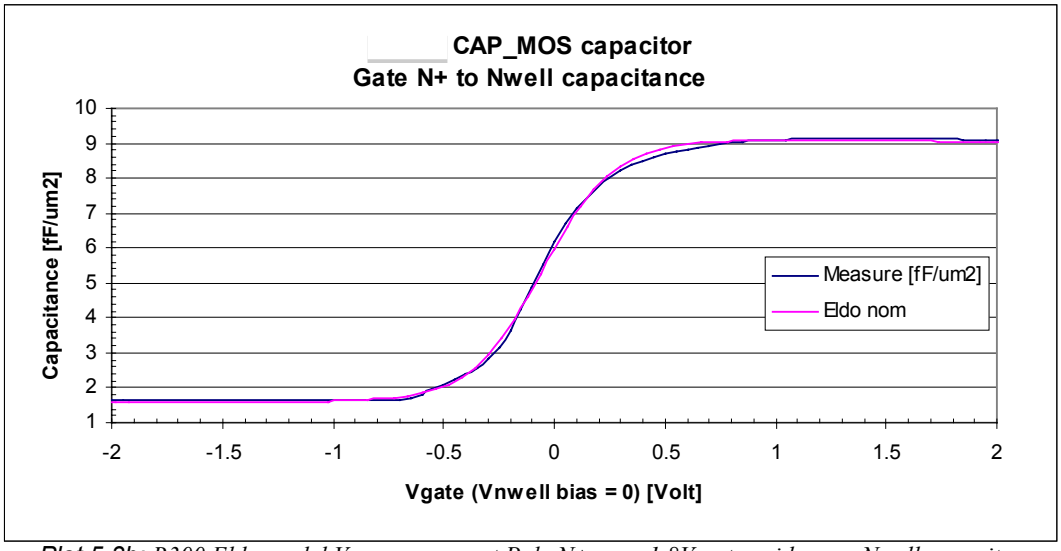


Plot 5.3a: R200 HSpice model Vs measurement Poly N+ over 3.3V gate oxide over Nwell capacitor

CAP_MOS, 1.8 Volt gate oxide:

Max Capacitance @27 °C @3.3 V,	Typical:	9.1	fF/um2
	Specification:	[8.4, 9.8]	fF/um2

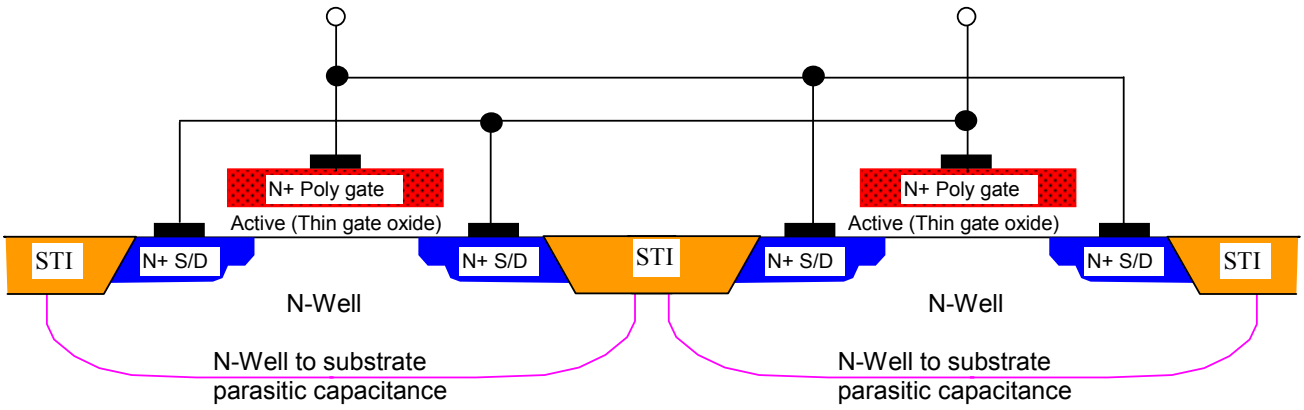
linearity coefficient @27 °C, highly non linear, see graph hereafter.



Plot 5.3b: R300 Eldo model Vs measurement Poly N+ over 1.8V gate oxide over Nwell capacitor

5.4: Anti parallel N+ over Nwell gate capacitor:

In order to use the capacitor with a negative or positive bias on the gate (with assuming that the Nwell bias is always positive to the substrate) it could be possible to connect in anti parallel mode the N+ to Nwell gate capacitors,
The total value of the capacitance is the total of the accumulation capacitance and the inversion capacitance. Previous model will be used for simulation.



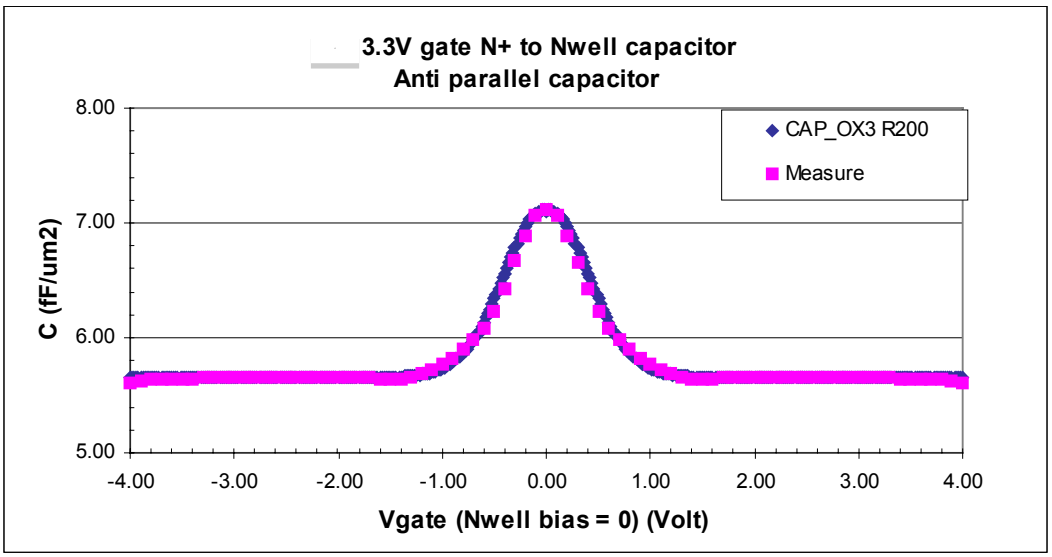
The following specified values are for an anti parallel capacitor composed of two poly plates. Example for a unit 10*10 um2 CAP_OX3 capacitor:

The total area of the thin oxide capacitor will be 10*10*2 um2, but only one plate will be take into account.

The total capacitance @3.3 Volt will be 10*10*5.6 = 560 fF.

CAP_OX3, 3.3 Volt gate oxide anti parallel capacitor:

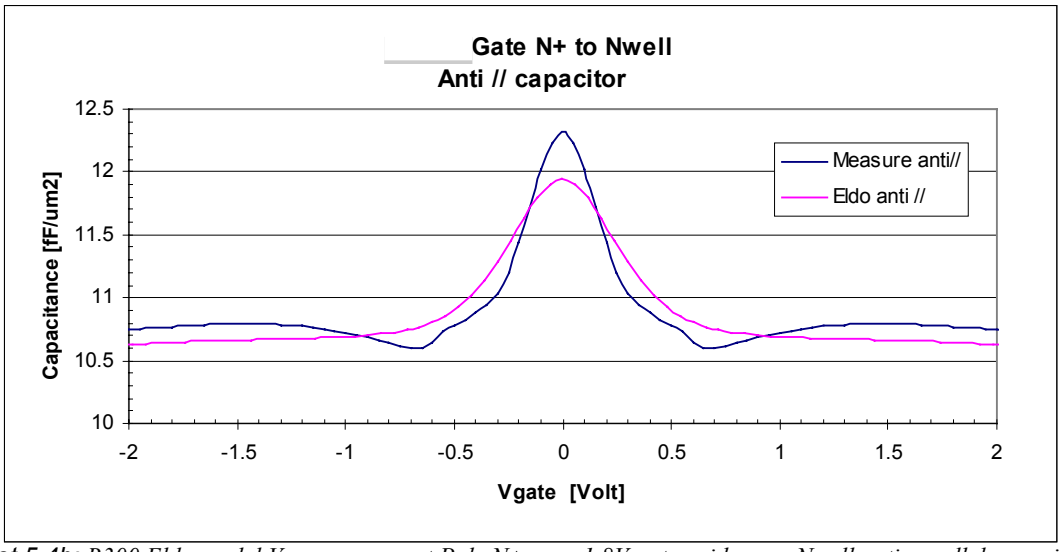
Capacitance @27 °C @3.3 V,	Typical:	5.6	fF/um2
	Specification:	[5, 6.3]	fF/um2
linearity coefficient @27 °C,	highly non linear, see graph hereafter.		



Plot 5.4a: R200 HSpice model Vs measurement Poly N+ over 3.3V gate oxide over Nwell anti parallel capacitor

CAP_MOS, 1.8 Volt gate oxide anti parallel capacitor:

Capacitance @27 °C @3.3 V,	Typical:	10.7	fF/um2
	Specification:	[9.8, 11.5]	fF/um2
linearity coefficient @27 °C,	highly non linear, see graph hereafter.		



Plot 5.4b: R300 Eldo model Vs measurement Poly N+ over 1.8V gate oxide over Nwell anti parallel capacitor