A 10-bit 40MS/s Successive Approximation Register A/D Converter

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Abstract – A 10 bit, 40MS/s successive approximation register is presented in this paper. The whole structure consists of a fully-differential capacitor array along with a comparator and SAR control logic. The total power consumption is 35mW.

Introduction

Compared with other popular types of ADC architecture, successive approximation register (SAR) ADC provides numbers of advantages. With only one comparator in the whole system, SAR can achieve the demand for low power consumption. High resolution and accuracy can be achieved using capacitor array during data conversion. Combined with these factors, SAR becomes an ideal component for some portable or battery-powered instruments. The overall system architecture is shown in Figure 1.

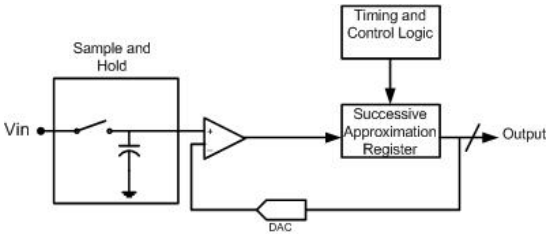

Figure. 1 Conceptual system architecture for 10 bit SAR ADC

The capacitor array is realized using C-2C differential two-stage weighted capacitor (TWC) [1]. Compared with the conventional binary-weighted capacitor array (BWC) [2], TWC occupies smaller area and provides higher conversion speed. Also, since the unit capacitor of C-2C is larger than BWC's, thus implies that C-2C has better capacitor mismatch tolerance. One drawback occurs when using capacitor array is the existence of parasitic capacitance, which can somehow deteriorate the linearity of the array.

In this paper, a 10 bit fully differential successive approximation ADC with 40MS/s is presented.

Comparator Design

A high-speed CMOS comparator is illustrated in Figure 2 [2]. It is consisted of a differential input stage, two flip flops and a S-R latch. Two non-overlapping clocks are also required. With no extra offset cancellation in this design, low power consumption, small die area and comparison speed can be achieved. The comparator is designed to operate at a 2.5V power supply with a sampling rate of 440MS/s.

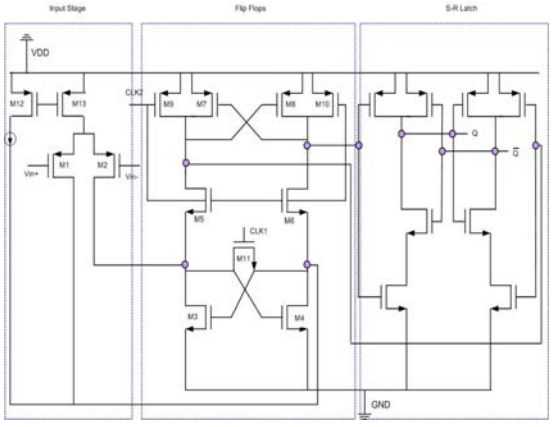

Figure. 2 Comparator Topology

As discussed in the class, there are three phases in one cycle. When CLK1 is high, comparator is in the reset mode, which forces node a and b to be equal. Next, when both CLK1 and CLK2 are low, M3 and M4 start to regenerate. When CLK1 is low and CLK2 is high, transistors M3, M4, M7, M8 form two back to back inverters that cause voltage at node a and b to grow exponentially in the opposite directions. The S-R latch part is used to store the output after the third phase and remains in this state in the next reset mode. Figure 3 represents the time diagram for the whole conversion process. There're 11 cycles for one conversion. Fist cycle is for the reset mode, and the other ten cycles are for determining each MSB's.

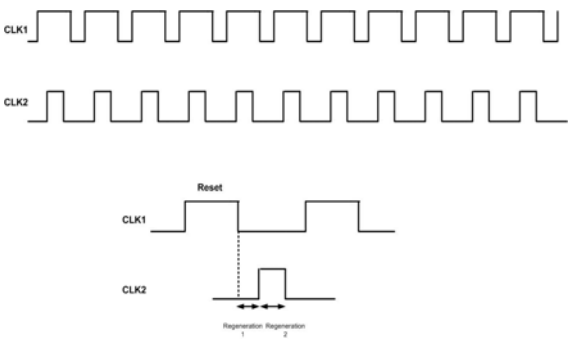

Figure. 3 Time Diagram for CLK1 and CLK2

SAR Algorithm

Figure 4 shows the basic architecture of differential two-stage weighted capacitors. In order to have binary outcomes, a dummy capacitor is added at the end of the array. During the sample mode, the switches connected to V_s are close and both upper and lower capacitor arrays are connected to V_{in}. The switches connected to V_s are opened for the hold mode. Thus, the total charge in both upper and lower array become as following,

$$Q^+ = (V_s - V_{in}^-) \times 2C$$

$$Q^- = (V_s - V_{in}^+) \times 2C$$

Next, for regeneration part, the MSB for lower and upper part are connected to $Vref_{f2}$ and $Vref_{p2}$ respectively and the rest capacitors are connected to $Vref_{f1}$ and $Vref_{p1}$.The general equations for ten times conversion are as following,

$$V^+ = V_s - V_{in}^- - Vref_{p2} + Vref_{p2} + A_9 \times \frac{Vref_{p1} - Vref_{p2}}{2} + A_8 \times \frac{Vref_{p1} - Vref_{p2}}{2^2} + A_7 \times \frac{Vref_{p1} - Vref_{p2}}{2^3} + ... + A_0 \times \frac{Vref_{p1} - Vref_{p2}}{2^{10}} - Vref_{p2}$$

$$V^- = V_s - V_{in}^+ + Vref_{n2} + A_9 \times \frac{Vref_{n1} - Vref_{n2}}{2} + A_8 \times \frac{Vref_{n1} - Vref_{n2}}{2^2} + A_7 \times \frac{Vref_{n1} - Vref_{n2}}{2^3} + ... + A_0 \times \frac{Vref_{n1} - Vref_{n2}}{2^{10}}$$

Choose $Vref_{p1}$ and $Vref_{n2}$ equal to ground, $Vref_{n1}$ and $Vref_{p2}$ to be 1 V. The equation becomes

$$V^+ - V^- = Vin^+ - Vin^- + Vref - \frac{A_9 \times Vref}{2} - \frac{A_8 \times Vref}{2^2} - \frac{A_7 \times Vref}{2^3} - .....$$

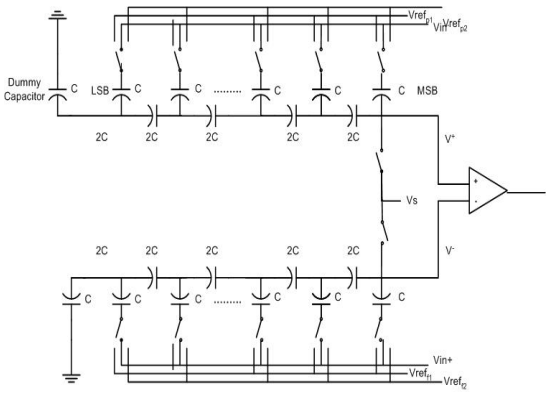

Figure 4 Differential capacitor array

SAR Control Logic

Step	Input DAC Signal										Comp O/P
0	0	0	0	0	0	0	0	0	0	0	N/A
1	1	0	0	0	0	0	0	0	0	0	a_9
2	a_9	1	0	0	0	0	0	0	0	0	a_8
3	a_9	a_8	1	0	0	0	0	0	0	0	a_7
4	a_9	a_8	a_7	1	0	0	0	0	0	0	a_6
5	a_9	a_8	a_7	a_6	1	0	0	0	0	0	a_5
6	a_9	a_8	a_7	a_6	a_5	1	0	0	0	0	a_4
7	a_9	a_8	a_7	a_6	a_5	a_4	1	0	0	0	a_3
8	a_9	a_8	a_7	a_6	a_5	a_4	a_3	1	0	0	a_2
9	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	1	0	a_1
10	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	1	a_0

Table 1 FSM sequence for N=11

A sequential finite state machine (FSM) is used in the conversion process as shown is table 1 [4]. A 3 inputs shift register is implemented in this control logic. For step 0, all the registers are forced to 0. The conversion process starts with the initialized state, which forces the MSB register to 1 and 0 for the others. This can be realized by using a synchronized reset signal. For a generic step (m=1, …., 10), three possible actions are chosen by register on a single bit:

I. shifting the guessing 1 to the next register ($k+1^{th}$)

II. using the output from the comparator

III. storing the output of the k^{th} register (memorization)

The internal structure of a shift register is shown in Figure ?. It is composed by a d flip flops with a multiplexer and a decoder. As shown in the figure, by controlling the inputs of A and B, MUX is able to choose one of the three inputs.In order to set SAR in the right mode, A and B are selected from the output of previous flip flops stage and the output of K^{th} flip flops itself respectively. Truth table for FF outputs is shown in Table 2.

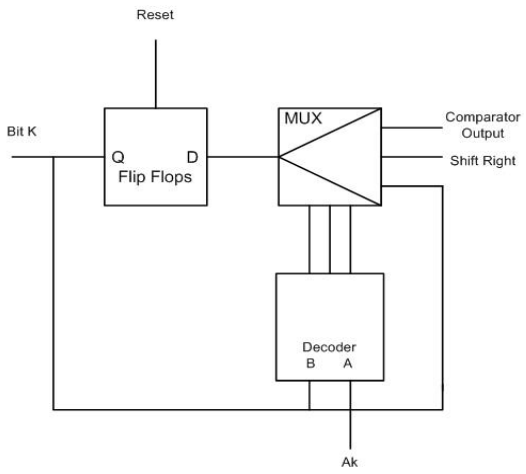

Figure. 5 Structure of shift register

A	B	Operation
1	-	memorize present stage
0	1	comparator o/p
0	0	shift to the next register

Table 2 Truth Table for FF output

Simulation Results

The following figures show the results of our simulations. Figure 6 shows the digital output during the conversion process. Figure 7 and 8 are the digital output for sine wave and ramp input respectively. The DNL and INL for the ADC converter are shown in figure 9 and 10. By using Matlab, the SNDR for our design is about 26.78dB. ENOB is around 4.12.

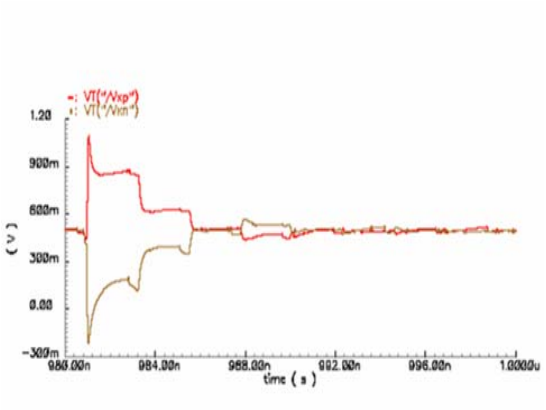

Figure. 6 Digital output for ten times conversion.

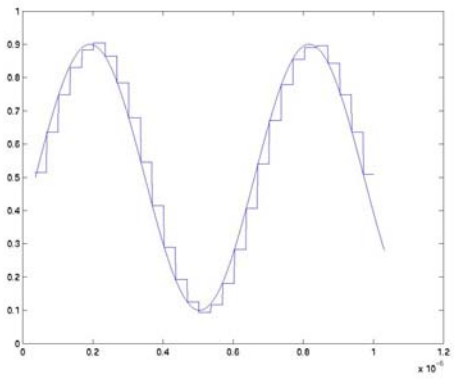

Figure. 7 Sine wave input and digital output for 400MS/s.

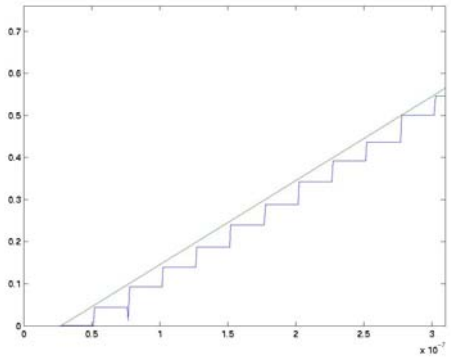

Figure. 8 Digital output for ramp input using Matlab

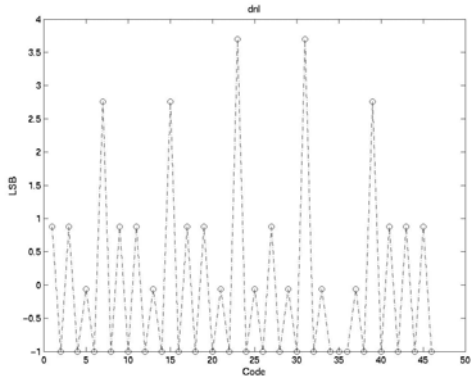

Figure. 9 DNL simulation using Matlab

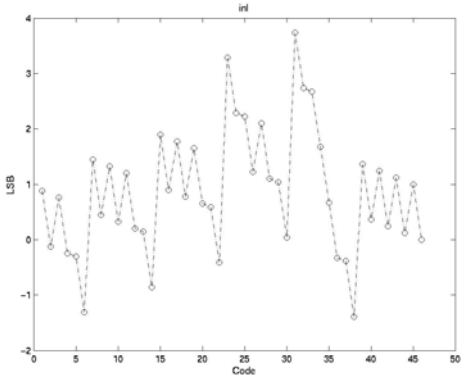

Figure. 10 INL simulation using Matlab.

Conclusion

A CMOS 10-bit successive approximation register was presented and simulated in this paper. It consists of a comparator, a differential C-2C capacitor array and a control logic. Total power consumption is 35mW.

Reference

[1]James L. McCreary, “Matching Properties and Voltage and Temperature Dependence of MOS Capacitors,” IEEE Journal of Solid-State Circuits, Vol. SC-16, No.6, December 1981

[2] James L. McCreary, Paul R. Gray, “All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques-Part 1,” IEEE Journal of Solid-State Circuits, Vol. SC-10, No.6, December 1975.

[3]Bahzad Razavi, “Data Conversion System Design,” IEEE Press.

[4]A. Rossi and G. Fucili, “Nonredundant Successive Approximation Register for A/D Converters,” Electronics letters, Vol.32, No. 12, 6th June 1996.