Low Power Voltage Reference Architectures

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***Abstract*—In this paper, we present 3 novel methods for generating voltage references. The first architecture focuses on low voltage high precision voltage reference reducing the variation to 5mV from 105mV across temperature of -40 to 100°C. The second architecture focuses on low voltage low power reference bringing down current consumption to half. The third one is a hybrid architecture with lesser voltage reference variation and lesser power consumption but has higher operational voltage.**

Keywords: Low power, Voltage reference, Subthreshold.

I. Introduction

With the scaling of transistor sizes and reduction in voltage of operation, power consumed by circuits has become a critical parameter in circuit design. In this paper, we introduce 3 novel low-voltage low-power voltage reference circuits which consume lesser power and generate reference with better accuracy as compared to present architectures.

Although, a bipolar junction transistor based bandgap reference is commonly used for voltage reference, the limit on power consumed by the circuit restricts the use of bandgap reference. The circuit presented in [1] uses two NMOS's operating in subthreshold region to generate bandgap reference and consumes lesser power compared to traditional bandgap reference. The circuit presented in [2], which is also shown in Fig. 1, generates voltage reference by using the difference between threshold voltage of depletion NMOS(nhvnative) and enhancement NMOS(nhv). The generation of voltage reference in Fig. 1 is explained below.

The current through the NMOS in subthreshold region can be written as [3] [4]:

$$I = \mu \frac{W}{L} I_0 [1 - e^{-V_{DS}/V_T}] e^{(V_{GS} - V_{TH} - V_{off})/nV_T} \quad (1)$$

where I_0 is a characteristic current, n is a slope factor, V_G, V_D and V_S are gate, drain and source voltages respectively, V_T is kT/q, W and L are length and width of NMOS, V_{TH} is threshold voltage and V_{off} is offset voltage. For $V_{DS} >> V_T$, (1) simplifies as:

$$I = \mu \frac{W}{L} I_0 e^{(V_{GS} - V_{TH} - V_{off})/nV_T} \quad (2)$$

Using (2), the current in nhv (M1) and nhvnative (M3) can be written as:

$$I_{M1} = \mu_{M1} \frac{W_{M1}}{L_{M1}} I_0 e^{(V_G - V_{TH_{M1}} - V_{off_{M1}})/n_{M1}V_T} \quad (3)$$

$$I_{M3} = \mu_{M3} \frac{W_{M3}}{L_{M3}} I_0 e^{(V_G - V_{REF1} - V_{TH_{M3}} - V_{off_{M3}})/n_{M3}V_T} \quad (4)$$

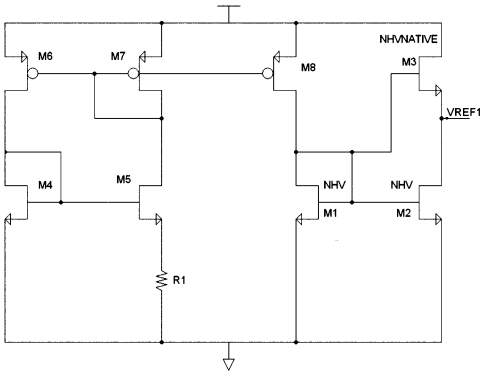

Fig. 1. Voltage Reference Generation

For nhv and nhvnative the slope factors are very close to each other, independent of process corner. Hence, $n_{M1} \approx n_{M3} = n$. Solving (3) and (4) simultaneously we get V_{REF1} as:

$$\begin{aligned} V_{REF1} &= V_{TH_{M1}} - V_{TH_{M3}} + V_{off_{M1}} - V_{off_{M3}} \\ &\quad + nV_T \ln \frac{\mu_{M3}}{\mu_{M1}} \frac{W_{M3}}{L_{M3}} \frac{L_{M1}}{W_{M1}} \frac{I_{M1}}{I_{M3}} \end{aligned} \quad (5)$$

For a given process corner, temperature slope of $V_{TH_{M1}}$ and $V_{TH_{M3}}$ are very close to each other. Since, V_{off} is independent of temperature and the last term in (5) is a weak function of temperature, the performance of V_{REF1} depends only upon the difference in the temperature coefficients between the threshold voltages of M1 and M3.

II. New Voltage Reference Circuit

In this section we will introduce the new circuit designs to improve accuracy of voltage reference and reduce power requirement of reference circuit as compared to circuit presented in Fig. 1.

A. Voltage Reference with Improved Accuracy

Although, the circuit shown in Fig. 1 cancels the variation across process, the difference in the temperature coefficient of threshold voltages between M1 and M3 results in a poor voltage reference. Performance of the circuit can be improved by compensating for the difference in slope of $V_{TH_{M1}}$ and $V_{TH_{M3}}$. The circuit shown in Fig. 2 uses the voltage proportional to absolute temperature (PTAT) from the beta-multiplier [3] to cancel the temperature variation. In Fig. 2, transistors M4, M5, M6 and M7 form the beta-multiplier. The voltage

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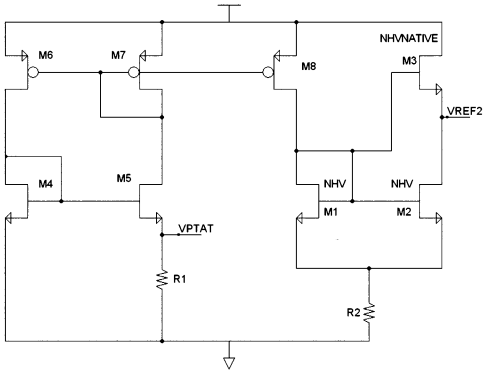

Fig. 2. Voltage Reference Generation with PTAT Addition

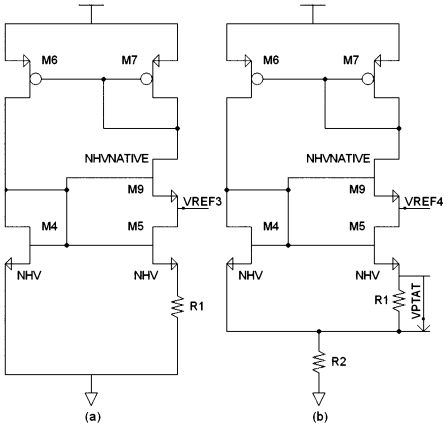

Fig. 3. Reduced Power Voltage Reference Generation

V_{PTAT} is proportional to absolute temperature [3] and is given by

$$V_{PTAT} = n_{M4} V_T \ln\left(\frac{W_{M5}}{L_{M5}} \frac{L_{M4}}{W_{M4}}\right) \tag{6}$$

Thus, the current through M7 can be written as

$$I_{M7} = \frac{V_{PTAT}}{R_1} \tag{7}$$

The current through M7 is mirrored in M8. Hence the voltage at the source node of M1 and M2 can be written as

$$V_{M1_S} = \frac{W_{M8}}{L_{M8}} \frac{L_{M7}}{W_{M7}} \left(1 + \frac{W_{M2}}{L_{M2}} \frac{L_{M1}}{W_{M1}}\right) I_{M7} R_2 \tag{8}$$

Using (5) and (11), V_{REF2} can be given by

$$V_{REF2} = V_{REF1} + V_{M1_S} \tag{9}$$

The voltage reference generated by (9) is more accurate than (5) since the variation of threshold voltages across temperature is compensated by the addition of PTAT voltage generated from beta-multiplier circuit.

B. Voltage Reference with Reduced Power Consumption

Power consumed by the circuit shown in Fig. 1 can be reduced if the voltage reference is generated from the same beta-multiplier which is used to generate bias currents. Fig. 3(a) shows the voltage reference circuit which consumes less power and gives better performance than that of Fig. 1. By following the same procedure described above for calculating V_{REF1}, V_{REF3} can be given by:

$$\begin{aligned} V_{REF3} &= V_{TH_{M4}} - V_{TH_{M9}} + V_{off_{M4}} - V_{off_{M9}} \\ &\quad + nV_T \ln \frac{\mu_{M9}}{\mu_{M4}} \frac{W_{M9}}{L_{M9}} \frac{L_{M4}}{W_{M4}} \frac{I_{M4}}{I_{M9}} \end{aligned} \tag{10}$$

The power consumed by circuit in Fig. 3(a) is lesser compared to the circuit in Fig. 1 since, bias current generation circuit also generates the voltage reference, hence reducing power consumption to half.

C. Merging Low Power Reference with High Precision Reference

We can combine low power voltage reference with high precision voltage reference to achieve a better voltage reference generation circuit as shown in Fig. 3(b). Once again, the voltage at source node of M4 can be written as

$$V_{M4_S} = R_2 I_{M7} \left(1 + \frac{W_{M6}}{L_{M6}} \frac{L_{M7}}{W_{M7}}\right) \tag{11}$$

Hence the voltage reference generated by this circuit is given as:

$$V_{REF4} = V_{REF3} + V_{M4_S} \tag{12}$$

and I_{M7} is given by (7). The voltage reference generated by (12) has same accuracy compared to (9) but consumes lesser power since it uses beta-multiplier for voltage reference generation.

III. Simulation Results

Circuits presented in this paper are simulated for 130nm technology node. Fig. 4 shows variation of voltage reference generation schemes across temperature with constant supply voltage of 1.8V on a typical process corner. V_{REF2} and V_{REF4} show significant improvement in performance after compensating for the temperature coefficient of threshold voltages.

Fig. 5 shows variation of voltage reference generation schemes across supply voltage at room temperature of 30°C and typical process corner.

Fig. 6 shows variation of voltage reference generation schemes across different process corners at constant supply voltage of 1.8V at room temperature of 30°C along with corner names on the xaxis. For e.g. FS stands for fast PMOS and slow NMOS.

Table I shows a comparison of current consumed and variation across temperature for existing voltage reference and proposed schemes. The comparison is done at constant supply voltage of 1.8V on typical process corner.

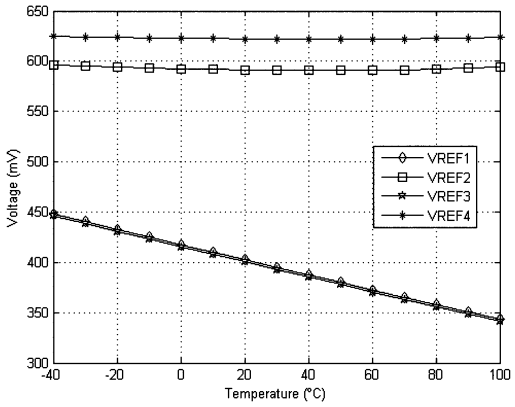

Fig. 4. Simulation Results for Different VREF Circuits across temperature

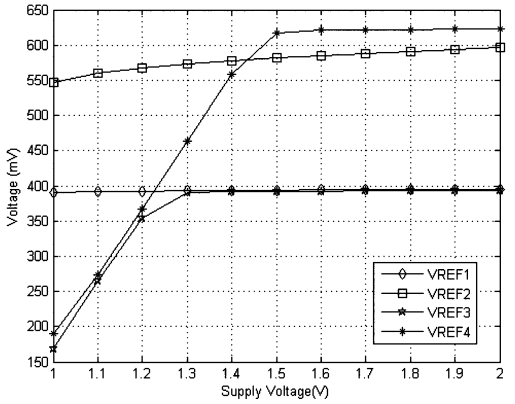

Fig. 5. Simulation Results for Different VREF Circuits across supply voltage

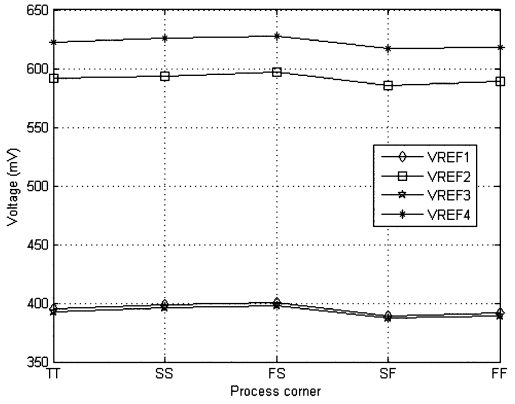

Fig. 6. Simulation Results for Different VREF Circuits across process corners

TABLE I
COMPARISON BETWEEN DIFFERENT VREF SCHEMES

Voltage reference	Current consumed(nA)	Variation across temperature(mV)
V_{REF1}	40	105
V_{REF2}	40	5
V_{REF3}	20	105
V_{REF4}	20	3.2

IV. CONCLUSION

In this paper, we have introduced three new low-power high-accuracy voltage reference circuits. The accuracy of voltage reference is improved by using PTAT voltage from beta-multiplier circuit. The power consumption is reduced by merging voltage reference generation with bias current generation. The simulation shows that the variation reduces to 3.2mV for high precision circuit compared to 105mV for present architecture. The power consumed by circuit comes down and becomes equal to the power required by beta-multiplier circuit.

An additional requirement for the proposed voltage reference circuits is the depletion NMOS which is a byproduct of the standard CMOS fabrication process. This depletion NMOS shows higher variation compared to the depletion NMOS fabricated in controlled environment. The simulation results presented in this paper use the former depletion NMOS. In order to achieve further accuracy of voltage reference, fabrication of depletion NMOS can be controlled by introducing additional masks.

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