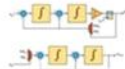


## Signal Processing In The Density Domain (Part III)

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Electronic Design

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I'm more excited about writing this series of columns on density domain than any of my other writings. Modulators are fundamental building blocks in a system designer's bag of tricks, and I don't see them getting the attention they deserve. They are as fundamental as a D flip-flop and should be as iconic to the practicing designer.

Among my responsibilities at Cypress, I occasionally go to colleges or universities to help a professor set up a laboratory for a microcontroller-based system class. I'm surprised to see that if delta-sigma modulation is discussed at all, it is only as the front half of an analog-to-digital converter (ADC).

Density signal processing has much more to offer the mixed-signal designer than simple analog-to-digital, or digital-to-analog, conversion. You didn't learn the stuff I'm talking about here at school. After a cursory search of research papers, I've found it isn't being discussed there either. (Of course, now I'll get e-mail from researchers who are working in this field, but I figure this is a sneaky and easy way to make contact with them.)

### Analog Modulators And Filters

A modulator converts an analog or digital signal into a density stream, while a filter converts a digital stream to an analog or digital signal (see "Signal Processing In The Density Domain (Part II)"). Three common types of modulation include pulse width modulation, pseudorandom modulation, and delta-sigma modulation.

Now when you see a flip-flop symbol, it represents an idea. You most likely went through the theory and construction of one while in school. Unless you're a logic cell designer, you really no longer worry about the implementation. Its performance can be defined by a handful of parameters. (In this case, setup, hold, delay, rise and fall times, and voltage levels for logic states.)

It's also the same with modulators and filters. First you get a brief discussion about the theory and implementation, and from then you just treat them as black boxes. First, the theory.

An analog filter is just that: an analog filter. For further information, I recommend *The Active Filter Cookbook* by Don Lancaster. It is an excellent reference for the working engineer, and it's my goal to someday be able to write half as well as Don. I have bought about eight copies in my life because they kept being stolen. I can't think of a higher praise for a book than for it to be so "stealable."

In part II of this series, I showed and described an implementation of an analog pulse-width modulator (PWM). Since I know of no practical design for an analog pseudorandom modulator (PRM), that leaves the delta-sigma modulator. Figure 1 shows a block diagram for a two-stage delta-sigma modulator (DSM) and a second-order low pass filter.

It is called "delta-sigma" because each stage has a subtractor (delta) and an integrator (sigma). This example is a two-stage filter, but it could have easily been just one stage or even a higher number of stages. For this modulator, its performance can be defined by this handful of parameters:

- The number of stages
- The reference ( $Ref_H$  and  $Ref_L$ )
- The quantization clock ( $f_a$ )

I included the filter to show how remarkably similar they are. The DSM used the filter as part of its topology. This is not uncommon. An adaptive differential pulse code modulation (ADPCM) encoder uses an ADPCM decoder as part of its implementation. (In fact, there are a lot of similarities between delta-sigma modulation and ADPCM, but I will save that for a future column.)

### Digital Modulators

A digital modulator takes a digital value and converts it to a density stream. Figure 2 shows three of them. On the top left is the PWM. When its count value goes below the density value, it goes high. The output frequency will be the clock divided by the period (counter modulo). The important parameters for a PWM are:

- The size of the period (i.e., the number of counter steps)
- The sample clock ( $f_s$ )

A 16-bit PWM with a 48-MHz clock will have a resolution of 65,536 steps and an output frequency of 732 Hz independent of the density value.

On the top right is the PRM. It uses a pseudorandom counter instead of a down counter. When its count value goes below the density value, it goes high. At each stage, the output has a probability of being on that is equal to the density value divided by the number of counter states. The output frequency is:

$$f_{PRM} = \begin{cases} \frac{1}{2} d \cdot f_s & : d \leq 0.5 \\ \frac{1}{2} (1 - d) \cdot f_s & : d > 0.5 \end{cases}$$

The important parameters for a PRM are:

- The size of the period (i.e., the number of counter steps)
- The sample clock ( $f_s$ )

A 16-bit PRM with a 48-MHz clock and a density value of 20,000 will have a resolution of 65,536-1 steps. Its density will be 30.5% (20,000/65,535), and its output frequency will average to 7.32 MHz.

The DSM is at the bottom of Figure 2. The sigma part is an adder and register used to make an accumulator, while the delta is the overflow for the adder. For an 8-bit adder and a density value of 128, the carry will output every other time (50%). For a density value of 64, the carry will output every fourth time (25%). For a density value of 63, the carry will output mostly every fourth time but occasionally every fifth time for an average of 1 out of 4.0635 times (63/256). The output frequency is:

$$f_{DSM} = \begin{cases} d \cdot f_s & : d \leq 0.5 \\ (1 - d) \cdot f_s & : d > 0.5 \end{cases}$$

The important parameters for a delta-sigma modulation PRM are:

- The size of the adder (i.e., the number of bits)
- The sample clock ( $f_s$ )

A 16-bit DSM with a 48-MHz clock and a density value of 20,000 will have a density of 30.5% (20,000/65,536) and an output frequency of 14.65 MHz.

A big problem with PWMs is that, for a constant clock, the output frequency decreases as the resolution increases. The dithered modulator attempts to fix this (Fig. 3).

For this topology, the comparator must be changed to allow a digital input to control whether or not the comparison is  $A < B$  (logic 0) or  $A \leq B$  (logic 1). This means the pulse width can be increased by a single count through digital control. Dither this input and you get the equivalent of fractional counts.

The PWM has its own counter-sized density register. It will output a pulse determined by the density value and the new digital input. When the PWM counts down to zero, it will reset the counter and output a carry (tc) pulse. This pulse's frequency is the same as the PWM's output and must be used to clock the dithering hardware because the PWM's output has no frequency with a density of zero to 100%.

This clock is used to clock the DSM. It has its own density value register and adder size. If the DSM has a density of 50%, it will cause every other PWM period to increase by one count average of one-half counts. This is called a delta-sigma modulated PWM (DSMPWM). The important parameters for a DSMPWM are:

- PWM period size (i.e., the number of counter steps)
- The sample clock ( $f_s$ )
- The DSM adder size

A 16-bit DSMPWM, comprising an 8-bit PWM and 8-bit DSM with a 48-MHz clock and a 20,000 value, will have:

- A PWM density value of 78 (upper byte) resulting in an output frequency of 187 kHz
- A DSM density value of 32 (lower byte) resulting in a PWM pulse-width increase in one out of eight PWM periods.

The pulse-width modulation will be 78 counts for seven periods and 79 for a single period resulting in an average of 78.125 counts. The modulator type has a constant output frequency while able to get high resolution without sacrificing output frequency.

It is not necessary to use a DSM to dither the PWM. Other dithered PWM types include a pseudorandom modulated PWM (PRMPWM) or a pulse-width modulated PWM (PWMPWM).

In my next column, I will describe the construction of digital density filters and show practical examples.

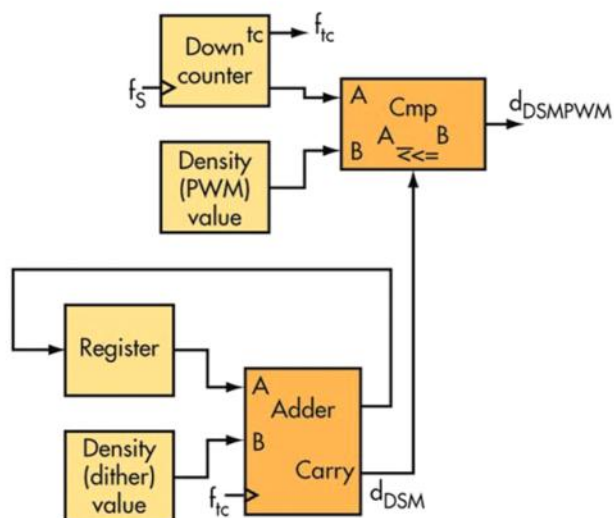


Fig 3. To increase the effective resolution of a PWM, the pulse width can be modulated to provide fractional counts.

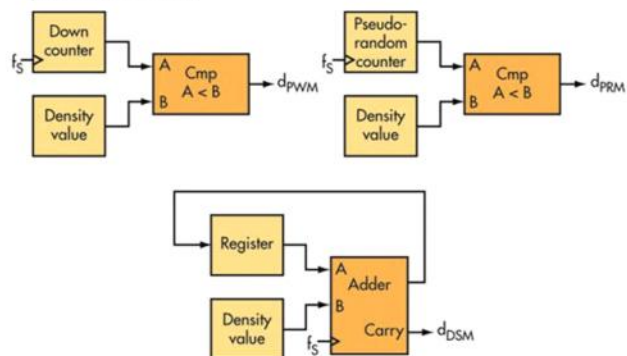


Fig 2. Compare the PWM, PRM, and DSM. Note that the difference between a PWM and a PRM is the type of counter used.

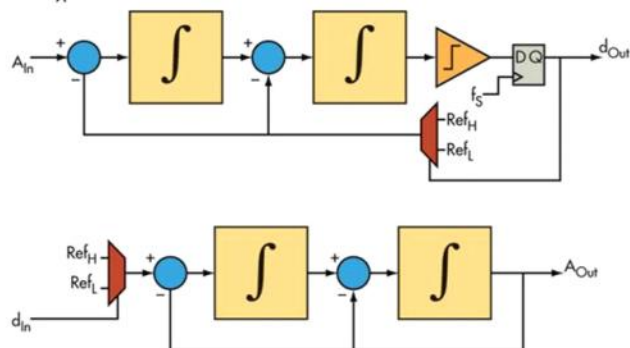


Fig 1. A DSM and its corresponding filter look remarkably similar. The primary difference is the signal being fed back.

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