PSoC® 3, PSoC 4, and PSoC 5LP – Temperature Measurement with a Diode

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Software Version: PSoC Creator™ 3.1 CP1 or later
Related Application Notes: For a complete list of the application notes, click here.

AN60590 explains diode-based temperature measurement using PSoC® 3, PSoC 4, and PSoC 5LP. The temperature is measured based on the diode forward bias current dependence on temperature. This application note details how the flexible analog architecture of PSoC 3, PSoC 4, and PSoC 5LP enables you to measure diode temperatures using a single PSoC device.

Contents

Introduction

Temperature is the most common and frequently measured environmental variable. Temperature measurements typically use one of the four sensors: thermocouple, thermistor, diode, and resistance temperature detector (RTD). The primary criteria for choosing a sensor are cost, accuracy, and temperature range.

Table 1 offers a comparison of four different types of temperature sensors, enabling you to choose the appropriate one for your application. This application note focuses on diodes. Refer to the Related Application Notes section for references on using RTD, thermocouple, and thermistor sensors with PSoC.

Table 1. Comparison of Temperature Sensors

Parameter	RTD	Thermocouple	Thermistor	Diode
Temperature range (0 °C)	–200 to +850	–250 to +2350	–100 to +300	–50 to +150
Sensitivity at 25 °C	0.387 Ω/°C	40 µV/°C (K-type)	416 Ω/°C	250 µV/°C
Accuracy	High	Medium to high	Medium	Low
Linearity	Good	Fair	Poor	Good
Typical cost (US $)	$3–$80	$3–$15	$0.2–$10	<$0.2
Typical usage	Surface mount for onboard temperature 3- and 4-wire up to a few hundred meters	<100 meters	Surface mount for onboard temperature Leaded for <1 meter	Onboard temperature
Resource requirement	Excitation current, amplifier, ADC, reference resistor	Amplifier, ADC, voltage reference, and another temperature sensor for cold junction	Excitation current, ADC, reference resistor	Excitation current, amplifier, ADC
Response time	Slow	Fast	Fast	Slow
Computational complexity (best possible accuracy)	High	Very high	Very high	Medium

Diode-based temperature measurement is suited for low-cost temperature sensing applications with temperature ranges from –50 °C to +150 °C and an accuracy of 2 °C to 5 °C. With on-chip current DACs and a 20-bit Delta Sigma ADC, PSoC 3 and PSoC 5LP enable high-resolution, accurate temperature measurement using only an external diode and a calibration resistor. PSoC 4 has on-chip current DACs and a 12-bit SAR ADC, so it can do medium accuracy and resolution temperature measurement. Table 2 gives a detailed comparison between PSoC 3/PSoC 5LP and PSoC 4 of resolution, accuracy at 125 °C worst case, and numbers of I/O pins for single-diode and multiple-diode sensing.

Table 2. Comparison of PSoC 3/PSoC 5LP and PSoC 4 for Diode Temperature Sensing

	Resolution	Accuracy	Number of I/O Pins for Single Diode	Number of I/O Pins for Multiple Diode (N ≥ 2)
PSoC 3 and PSoC 5LP (20-bit ADC configuration)	0.1 °C	2.37 °C	3	Depends on the available I/O pins. N diodes needs (N + 2) I/O pins. Note that the diodes here are configured as antiparallel diode pairs.
PSoC 4	1 °C	5.7 °C	6	Depends on the available I/O pins. N diodes needs (2N + 6) I/O pins. Note that the diodes here are not configured as antiparallel diode pairs.

Diode-based temperature measurement is typically used in one of the following two ways:

- Most CPU processors and some application-specific integrated circuits (ASICs) provide access to thermal diodes in their architecture to measure the temperature of the processor core. This temperature measurement is used for thermal management functions such as fan speed control to cool the processor core. PSoC 3, PSoC 4, and PSoC 5LP can be used to interface with those thermal diodes to measure the core temperature and perform fan speed control.

- It is also possible to use general-purpose transistors (such as 2N3904) in the diode-connected configuration for temperature measurement in any application. The reason to opt for a general-purpose transistor would be the extremely low transistor cost along with less stringent accuracy requirements.

The Diode Equation

The following equation gives the current I through a forward-biased diode:

$$I = I_s \, e^{\frac{V}{\eta V_T}}$$ Equation 1

Where,

V – The diode forward voltage drop

I_s – The reverse saturation current

η – A constant (called "ideality factor") that has a value between 1 and 2, depending on the material and the physical structure of the diode

V_T – The thermal voltage given by:

$$V_T = \frac{kT}{q}$$ Equation 2

Where,

k – Boltzmann's constant (1.38×10^{-23} joules/Kelvin)

T – The absolute temperature in Kelvin

q – The magnitude of electronic charge (1.602×10^{-19} coulomb)

The temperature-dependent factors in Equation 1 are I_s and V_T. The reverse saturation current I_s typically doubles for every 5 °C rise in temperature. I_s depends on the physical properties of the diode. V_T is directly proportional to the temperature.

Measuring Diode Temperature

The technique for measuring the diode temperature is based on applying two different known currents to flow through the diode and measuring the diode voltage in each case.

For two different currents I_1 and I_2, such that $I_2 = NI_1$,

$$I_1 = I_s \, e^{\frac{V1}{\eta V_T}}$$

$$I_2 = I_s \, e^{\frac{V2}{\eta V_T}}$$

$$\frac{I_2}{I_1} = N = e^{\frac{V_2 - V_1}{\eta V_T}}$$ Equation 3

Taking natural logarithm on both sides,

$$\ln(N) = \frac{(V_2 - V_1)}{\eta V_T}$$ Equation 4

Using Equation 2 in Equation 4, the temperature (T) in Kelvin is given by:

$$T \,(in\,Kelvin) = (V_2 - V_1) * \frac{q}{\ln(N) * k * \eta}$$

$$T(in\,Kelvin) = c * \Delta V$$

$$T(in\;{}^0C) = (c * \Delta V) - 273$$ Equation 5

Where,

$\Delta V = (V_2 - V_1)$ – The difference in diode forward voltage drops for the two currents I2 and I1.
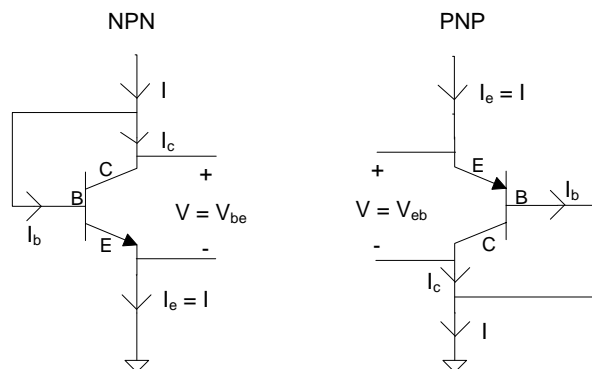
c – A constant given by:

$$c = \frac{(q)}{k * \eta * \ln(N)}$$ Equation 6

Transistor as Diode

Equations 5 and 6 are derived for a diode. For the temperature measurement application, this document uses a transistor in a diode-connected configuration instead of a standalone diode because the variations in the ideality factor 'η' due to manufacturing processes are less in transistors compared to diodes. For example, 2N3904 transistors have a constant ideality factor of 1.004, which is used in this application note.

In the diode-connected configuration, the collector and base terminals of the transistor are shorted together externally. Figure 1 shows that this configuration is for both NPN and PNP transistors. The transistor operates in the active region with the collector-base junction reverse biased and the base-emitter junction forward biased. The voltage (V) across the base and emitter terminals of the transistor is the equivalent of the diode voltage. The collector current (I$_c$) is the one responsible for the generation of the voltage 'V' because I$_c$ is the current entering (NPN) or leaving (PNP) the collector-base junction.

Figure 1. Transistor as Diode

In the temperature measurement application, the ratio of the bias currents I1 and I2 is considered as the ratio of the collector currents as well. This assumption is valid for transistors like 2N3904 that have a constant current gain h_{FE} over the bias current operating range (10 µA – 200 µA).

You can calculate the voltage sensitivity of the transistor-diode to temperature based on Equation 5 and Equation 6.

Voltage sensitivity is the change in voltage for a 1 °C or 1 K difference in temperature, and it is equal to (1/c) based on Equation 5.

For $'\eta' = 1.004, 'N' = 20$, you get $'c' \approx 3860$ Kelvin/volt. For this value of 'c', the voltage sensitivity is 259 µV/°C.

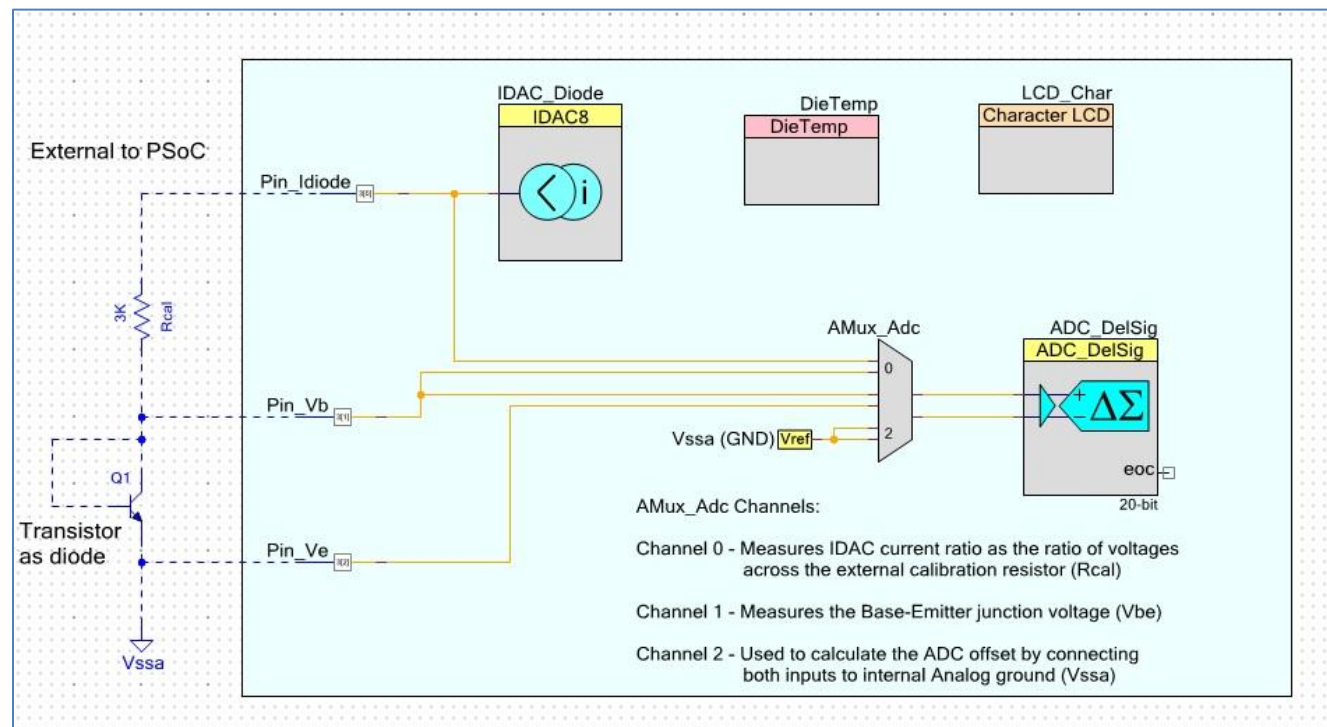$$T(in\ ^0C) = (\Delta V * 3860) - 273 \hspace{2cm} \text{Equation 7}$$

Measuring Diode Temperature Using PSoC 3 and PSoC 5LP

PSoC 3 and PSoC 5LP have a powerful analog architecture that enables the accurate measurement of diode temperature. The implementation in PSoC 3 and PSoC 5LP is based on Equation 5. Figure 2 is the top design schematic (*TopDesign.cysch)* for this implementation showing the external diode-connected transistor and the external calibration resistor. This calibration resistor is used to accurately calculate the IDAC current ratio 'N' given in Equation 6.

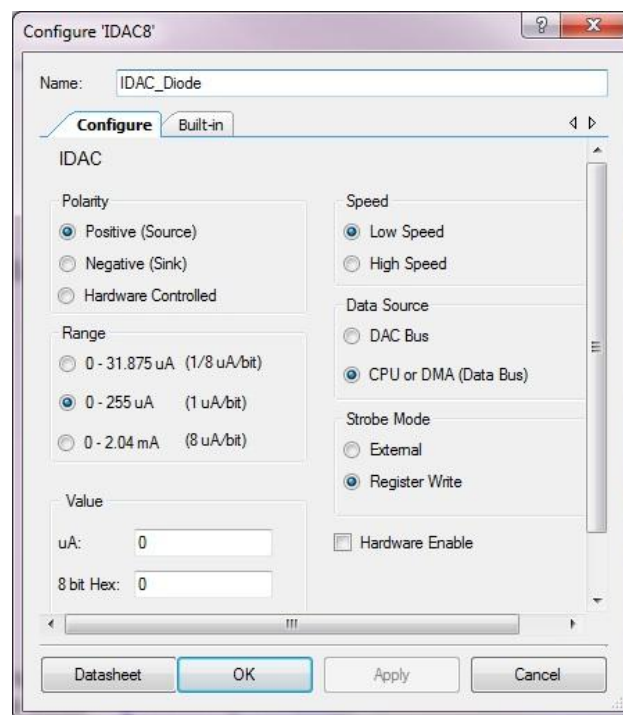Figure 2. Single-Diode Topology for PSoC 3 and PSoC 5LP

Functionality

■ The current DAC (IDAC) forces the two known currents I1, I2 through the transistor diode.

■ The corresponding base-emitter voltages V1 and V2 are measured using the Delta Sigma ADC.

■ Equation 5 is then used to calculate the temperature in firmware.

■ To ensure that the IDAC current ratio 'N' (N = I2/I1) in Equation 5 is computed accurately, a calibration resistor is connected at the output of IDAC in series with the transistor diode. The ratio of voltages across the calibration resistor gives the IDAC current ratio. This calibration removes the error due to IDAC offset, nonlinearity in temperature measurement. By using the high-resolution Delta Sigma ADC, the current ratio can be calculated very accurately.

■ The Analog Multiplexer Component in PSoC Creator™ is used to multiplex the ADC inputs to perform IDAC calibration, temperature calculation, and ADC offset calculation.

■ The ADC offset calculation is performed by shorting the internal analog ground (V_{SSA}) to the two ADC inputs and measuring the ADC output. This ADC offset correction is used while doing the IDAC calibration to measure the current ratio accurately.

■ The DieTemp Component is used to measure the PSoC die temperature. Whenever the internal die temperature changes by 10 °C, the current ratio 'N' is recalculated to ensure that any IDAC current drift over temperature does not affect the temperature measurement accuracy. The die temperature is used instead of the external diode temperature since it is possible for the diode and the PSoC to be in different thermal zones.

Component Configuration

Current DAC (IDAC) Configuration

The IDAC configuration settings are shown in Figure 3. The IDAC is configured for current sourcing mode, and the IDAC data register is updated by the CPU in firmware. The two currents that are sourced by the IDAC to flow through the diode are 10 µA and 200 µA, respectively. This makes the ratio factor 'N' in Equation 6 equal to '20'. For currents in this range, the self-heating of the diode is also at a minimum, and its effect on temperature measurement can be ignored without compromising the accuracy of the measured temperature.

Figure 3. IDAC Configuration for PSoC 3 and PSoC 5LP

ADC Configuration

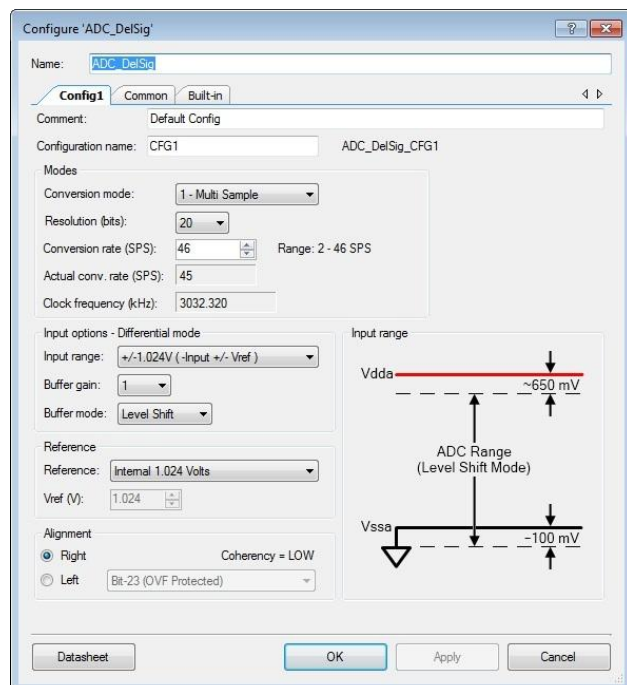The Delta Sigma ADC configuration settings are shown in Figure 4.

The ADC is set to differential input mode since the voltage is measured across the two terminals—the base and emitter terminals (V_{be}) of the transistor. The differential mode is used to perform a 4-wire measurement technique, which eliminates the effect of PCB trace resistance and internal analog routing resistance on the measured diode voltage. A detailed discussion on the effects of PCB trace resistances and best practices for mixed-signal board layout is given in the application note AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations.

The voltage V_{be} is usually about 0.5 V–0.7 V at room temperature for the bias currents that are used in this application. The voltage drop (V_{be}) changes by about 0.25 mV for every 1 °C increase in temperature. So in the region of temperature measurement (which is the diode operating temperature of –50 °C to +150 °C), the V_{be} voltage is a positive value less than 1 V. Thus the ±1.024-V range is chosen for the ADC input range. The ADC bit resolution is set to the maximum available 20 bits. In the ±1.024-V range, 20-bit ADC configuration, the voltage resolution is 2 µV. A 0.1 °C temperature resolution corresponds to a 25-µV voltage resolution. So with this ADC configuration, it is possible to measure the temperature to a resolution of less than 0.1 °C.

For a 1 °C resolution, 16-bit ADC configuration, which has a resolution of 32 µV, should be more than enough. With the lower end PSoC 3 and PSoC 5LP families, which only

have a 12-bit Delta Sigma ADC, a resolution of 2 °C can be obtained.

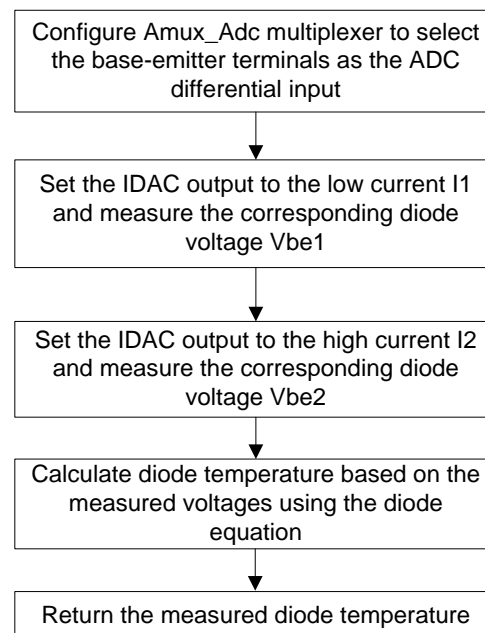Figure 4. ADC Configuration for PSoC 3 and PSoC 5LP

The reference for the ADC is the on-chip 1.024-V reference voltage. The **Buffer Mode** is configured for **Level Shift** mode, as the negative input of the ADC would be very close to V$_{SSA}$ (analog ground). See the ADC component datasheet in PSoC Creator to learn about these settings in detail.

Firmware Details

The project *A_SingleDiode* provided with the application note has the implementation done as shown in Figure 2. The files *SingleDiode.h* and *SingleDiode.c* in the project provide the C functions related to the diode temperature measurement. The function `InitializeDiodeMeasurement()` is called once at the start of the main code. This function configures and starts the Components (ADC, IDAC, AMUX, DieTemp) required for temperature measurement. It also does a IDAC calibration by calling the function `CalibrateIdac()`, which is used to calculate the IDAC current ratio 'N' used in the temperature measurement.

The function `GetDiodeTemperature()` is the function that you should call when a temperature measurement needs to be done. Figure 5 shows the algorithm implemented by this function.

Figure 5. Temperature Measurement Algorithm for PSoC 3 and PSoC 5LP

In the diode temperature measurement project, the IDAC current ratio calculation is done every time the PSoC die temperature changes by more than 10 °C. This is because the PSoC 3 and PSoC 5LP IDAC INL parameter varies with temperature (refer to the device datasheet for typical graphs). This results in a change in the IDAC current ratio, which in turn causes a small error in the temperature calculation. So the ratio calculation is done for every 10 °C change by calling the function CalibrateIdac() in the main code.
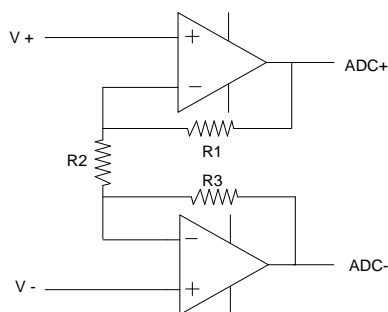
An averaging routine is performed on the voltages measured using the ADC to reduce any noise in temperature measurement. The number of samples used for averaging is decided based on the ADC configuration. A 12-bit ADC configuration requires a higher number of averaging samples than a 20-bit ADC configuration. The definitions in the *SingleDiode.h* file, in which the number of samples to be averaged is chosen based on the ADC bit resolution, support this determination.

Measuring Diode Temperature Using PSoC 4

PSoC 4 also has a powerful analog architecture that enables the measurement of diode temperature. The implementation is based on Equation 5.

With the 12-bit SAR ADC, the quantization error is 0.5 mV with 1.024 internal references. The ΔV_{be} change in voltage per °C is about 0.25 mV. Thus, signal amplification is necessary. Two on-chip opamps in PSoC 4 can be configured as the differential amplifier, as Figure 6 shows.

Figure 6. Two Opamps Configured as Differential Amplifier

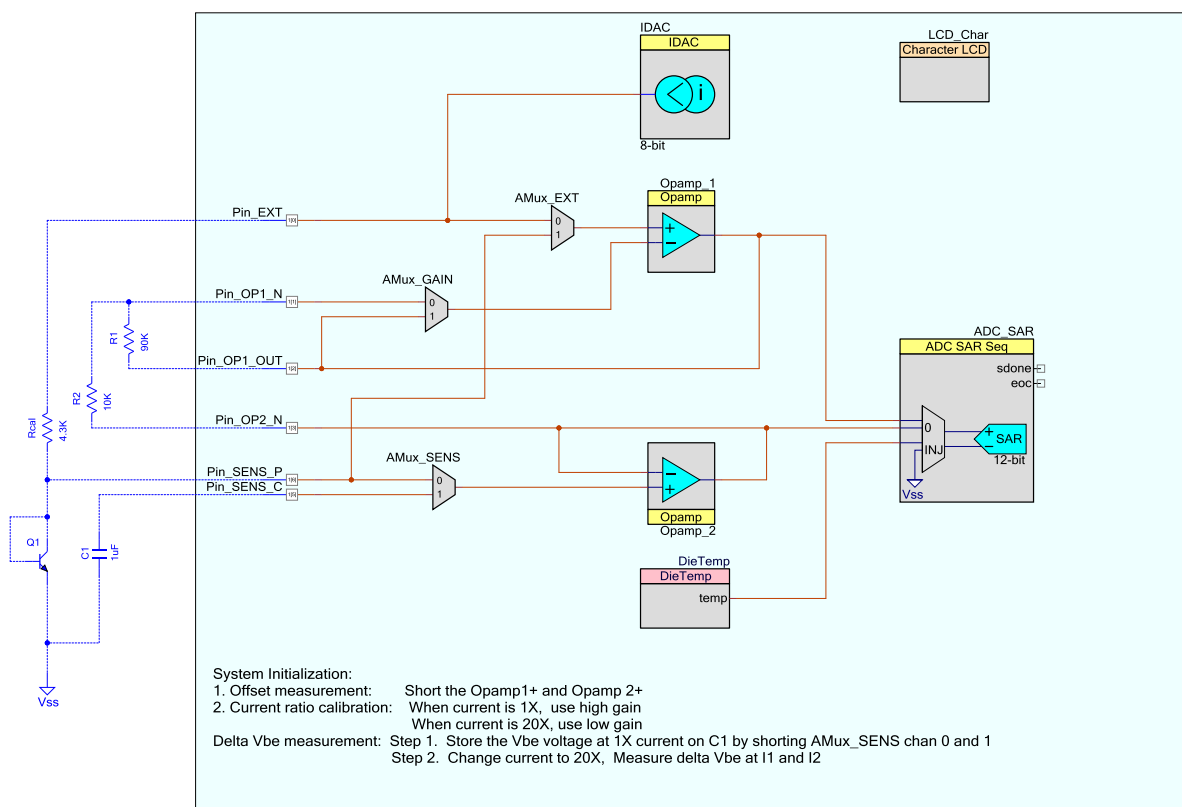The differential gain is equal to ($1 + \frac{R1+R3}{R2}$).

This circuit can even be simplified by removing R3, which reduces the external resistors from three to two. The other benefit of using the asymmetric resistors rather than the common three resistors is that it can result in a bigger gain and keep the common voltage in the range. If R3 is removed, the gain is $(1 + \frac{R1}{R2})$.

What you want to amplify is the ΔV in Equation 5, not the Vbe itself. Otherwise, the gain needs to be limited to a small value since Vbe is usually about 0.5 V–0.7 V at room temperature for the bias currents that are used in this application. To get a high gain and keep the common mode voltage within the opamp's operational spec, one capacitor is introduced to store the Vbe at low current (V1). Then, Vbe at higher current (V2) and V1 are used as the two inputs of the differential amplifier, and the output is sampled by ADC.

IDAC output may differ from the set value due to the offset, nonlinearity in temperature measurement. One external resistor can be used to calibrate these errors. The actual IDAC current I1, I2 can be measured by the voltage across the external calibration resistor (Rcal) under I1 and I2. To reduce the INL effect of ADC, the voltage across Rcal at I1 is amplified by high gain ($1 + \frac{R1}{R2}$), and the voltage across Rcal is not amplified by setting the gain equal to 1. The gain change can be implemented by an analog multiplexer.

Figure 7 is the top design schematic (TopDesign.cysch) for this implementation, showing the external diode-connected transistor, external calibration resistor, external resistors for internal opamps (R1, R2), and one capacitor (C1). This calibration resistor is used to accurately calculate the IDAC current ratio 'N' given in Equation 6. R1, R2 is the external resistors for the two internal opamps, which is configured as the differential amplifier. Capacitor C1 is used to store the Vbe voltage at I1 by shorting AMux_SENS Chan 0 and Chan 1, which will be compared with the Vbe at I2 current by the differential amplifier and then sent to the SAR ADC.

Figure 7. Single-Diode Topology for PSoC 4

Functionality

The current DAC (IDAC) forces the two known currents I1, I2 through the transistor diode and the external calibration resistor.

Offset measurement is the first step of the system initialization. The ADC offset calculation is performed by shorting opamp1+ and opamp2+. To implement it, Chan 1 of AMux_EXT and Chan 0 of AMux_SENS are selected. The AMux_GAIN is used to change the differential amplifier gain since different opamp gain introduces different offset. You need to measure two offsets, low gain offset and high gain offset, which will be used under different conditions. The offsets include the opamp offset and ADC offset. Meanwhile, note that the IDAC needs to be enabled to set a suitable bias for the opamp inputs. Otherwise, Q1 is open and acts as a high-impedance point, which is very sensitive to system noise. The current flows through Pin_EXT to Rcal, Q1 to GND. To make offset measurement more accurate, suitable bias voltage needs to be provided. Thus, for the high-gain offset, the IDAC is set to low current; for the low-gain offset, the IDAC is set to high current.

The offset value will be used in the current ratio calibration and ΔV_{be} measurement.

Current ratio calibration is the second step of the system initialization. To ensure that the IDAC current ratio 'N' (N = I2/I1) is accurate enough, a calibration resistor (R$_{cal}$) is connected at the output of the IDAC in series with the transistor (diode). The ratio of voltages across the calibration resistor gives the IDAC current ratio. To measure this voltage, Chan 0 of AMux_EXT is selected and Chan 0 of AMux_SENS is selected. Set the differential amplifier gain to high (1 + R1/R2) at the lower current (I1), and set the gain to 1 at high current I2 to reduce the INL effect by setting AMux_GAIN.

In the ΔV_{be} measurement, what really matters is the ΔV_{be} at I1, I2. To get the ΔV_{be}, one capacitor, C1, is used to store the V_{be} at I1 by setting AMux_SENS Chan 0 and Chan 1 both connected, and then the cap C1 disconnects from transistor Q1 by setting AMux_SENS Chan 0 disconnected and Chan 1 connected. Next, change the current to I2. The difference between the V_{be} at I2 and V_{C1} is amplified by selecting AMux_EXT to Chan 1 and AMux_SENS to Chan 1. AMux_GAIN is set to Chan 0 to get the high gain.
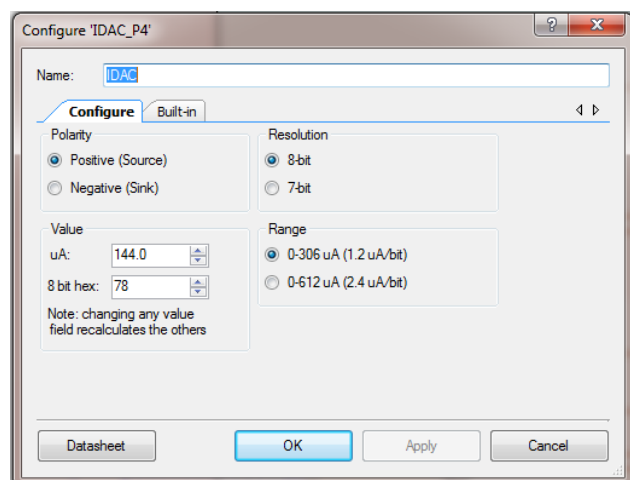
During the AMux_SENS switching, the C1 charge has some leakage due to the distributed capacitance of the AMux_SENS. This acts as a small offset and needs to be calibrated during the ΔV_{be} measurement.

Component Configuration

Current DAC (IDAC) Configuration

Figure 8 shows the IDAC configuration settings. The IDAC is configured for current sourcing mode, and the CPU updates the IDAC data register in firmware. Different from PSoC 3 and PSoC 5LP, the current resolution is 1.2 µA/bit for PSoC 4. The two currents that are sourced by the IDAC to flow through the diode are 9 * 1.2 µA and 180 * 1.2 µA, respectively. This makes the ratio factor 'N' in Equation 6 equal to '20'. For currents in this range, the self-heating of the diode is also at a minimum, and its effect on temperature measurement can be ignored without compromising the accuracy of the measured temperature.
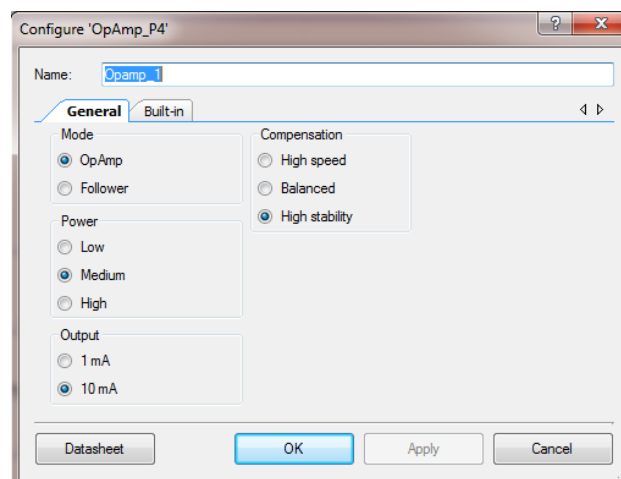
Figure 8. IDAC Configuration for PSoC 4

Opamp Configuration

The two opamps are configured as the differential amplifier, which amplifies the difference in voltage between the positive inputs. Figure 9 shows the configuration settings.

If the diode is on the far side, it is important to use a 4-wire measurement technique, which eliminates the effect of PCB trace resistance and internal analog routing resistance on the measured diode voltage. The application note AN57821 – PSoC 3, PSoC 4, and PSoC 5 Mixed Signal Circuit Board Layout Considerations offers a detailed discussion on the effects of PCB trace resistances and best practices for mixed-signal board layout.

Figure 9. Opamp Configuration for PSoC 4

ADC Configuration

Figure 10 and Figure 11 illustrate the SAR ADC configuration settings.

The ADC Channel 0 is set as differential and connected to the outputs of two opamps. Channel 1 is set as single ended and connected to the die temperature sensor.

With a 1 percent 1.024-V internal reference, the ADC differential input range is ±1.024 V. The voltage V_{be} is usually about 0.5 V–0.7 V at room temperature for the bias currents that are used in this application. Using Equation 6, it can be shown that the change in voltage per °C is about 0.25 mV. There is zero difference between the two voltages at absolute zero (–273.15 °C), while at room temperature there should be (273.15 + 25) * 0.25 mV = 74.5 mV difference between the two voltage readings. From –50 °C to +125 °C, the voltage difference changes from 55.8 mV to 99.5 mV. Suitable opamp gain should be set to make the output within 1.024 V. The bit resolution is set to the maximum available 12 bits. In the ±1.024-V range, 12-bit ADC configuration, the voltage resolution is 500 µV. A 1 °C temperature change generates about 2.5-mV voltages at the ADC input after amplification, so it is possible to measure the temperature to a resolution of less than 1 °C.

Hardware averaging is a unique feature of PSoC 4 that is useful to eliminate the noise and is time-efficient compared with the firmware averaging. Here samples averaged are set to 16.

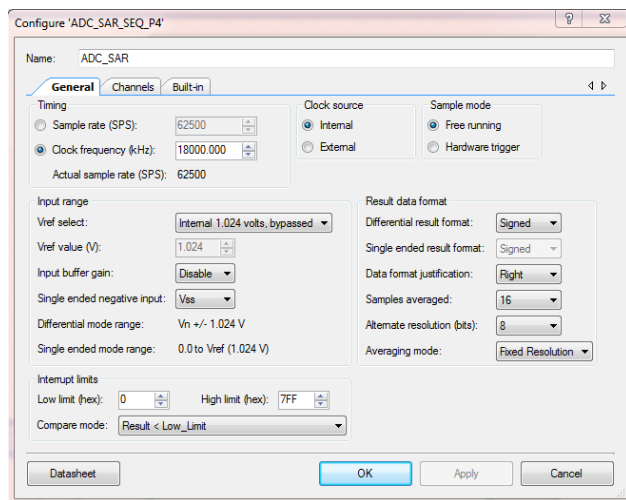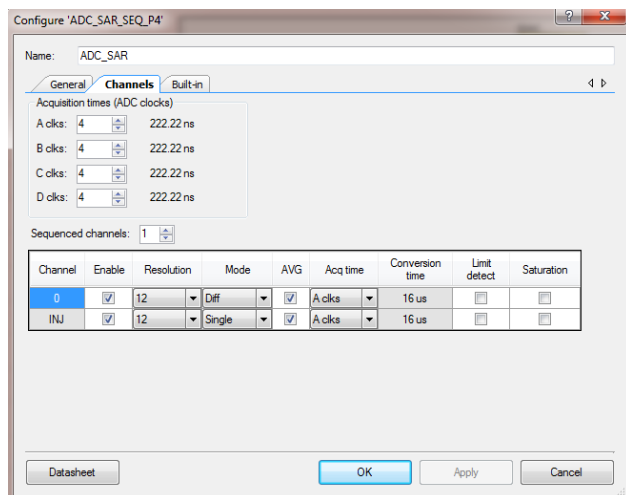Figure 10. SAR ADC General Configuration for PSoC 4

Figure 11. SAR ADC Channel Configuration for PSoC 4

See the SAR ADC component datasheet in PSoC Creator to learn about these settings in detail.
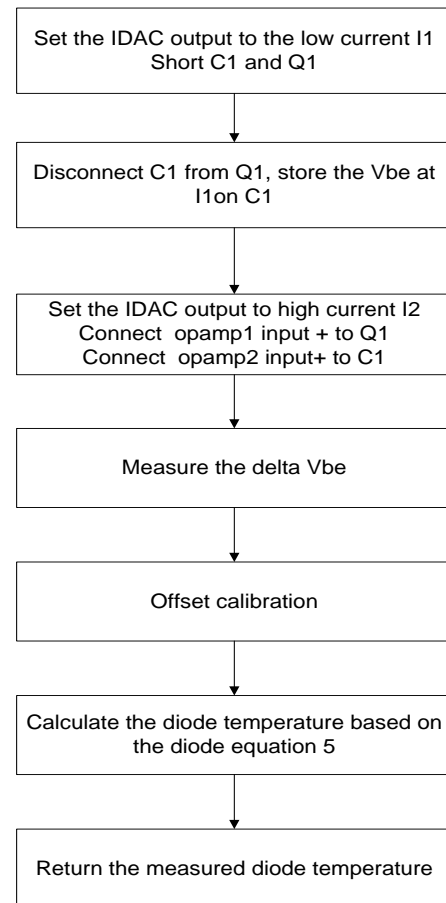
Firmware Details

The project *P4_SingleDiode* provided with the application note has the implementation done as shown in Figure 7. The files *SingleDiode.h* and *SingleDiode.c* in the project provide the C functions related to the diode temperature measurement. The function `InitializeDiodeMeasurement()` is called once at the start of the main code. This function configures and starts the Components (Opamps, ADC, IDAC, AMUX, DieTemp) required for temperature measurement. It also does a IDAC calibration by calling the function `CalibrateIdac()`, which is used to calculate the IDAC current ratio 'N' used in the temperature measurement. In this function, system offset at different gains is also measured, which is used in both current ratio calibration and ΔV_{be} measurement.

The function `GetDiodeTemperature()` is the function that you should call when a temperature measurement needs to be done. Figure 12 shows the algorithm implemented by this function. Offset calibration includes the system offset and the capacitor leakage offset.

Figure 12. PSoC 4 Temperature Measurement Algorithm

In the diode temperature measurement project, the IDAC current ratio calculation is done every time the PSoC die temperature changes by more than 10 °C. This is because the PSoC 4 IDAC INL parameter varies with temperature (refer to the device datasheet for typical graphs). This results in a change in the IDAC current ratio, which in turn causes a small error in the temperature calculation. So the ratio calculation is done for every 10 °C change by calling the function `CalibrateIdac()` in the main code.
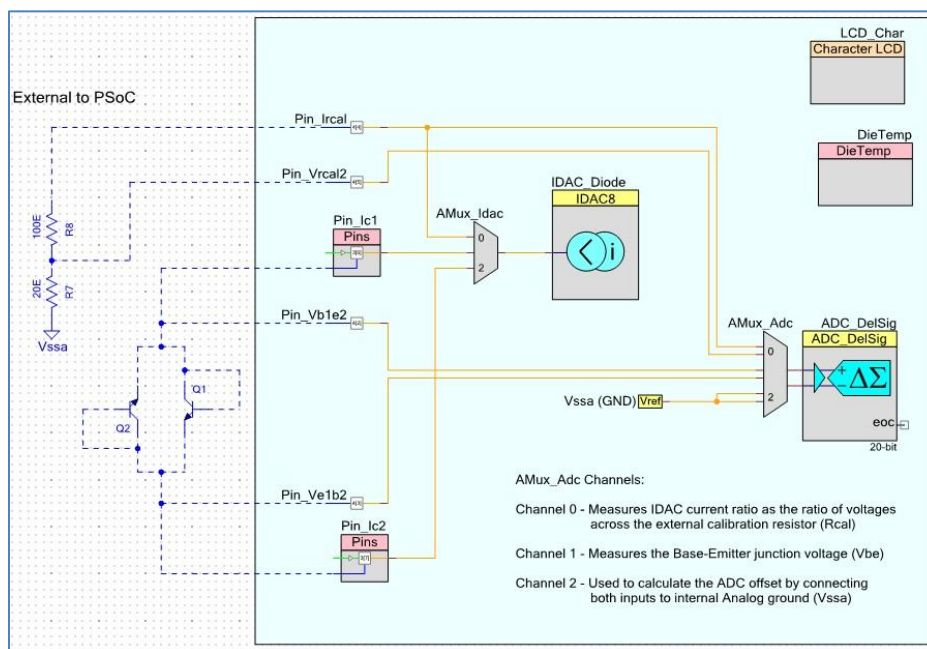
A firmware averaging routine is performed to reduce any noise in temperature measurement. The number of samples used for averaging is decided based on the ADC configuration and system noise level, which is defined in the *SingleDiode.h* file.

Antiparallel Diode Topology Using PSoC 3 and PSoC 5LP

The flexible GPIO pin architecture and the presence of analog multiplexers in PSoC 3 and PSoC 5LP enable the temperature measurement of two independent transistor diodes using only four pins. This is commonly called an "antiparallel diode connection" in which the base junction of one transistor is shorted with the emitter junction of the other transistor and vice versa. This ensures that only one of the transistors is ON at any instant of time for which the temperature can be measured. CY8CKIT-025, the temperature sensor EBK explained in the CY8CKIT-025 Temperature Sensor section, supports the antiparallel diode topology. Figure 13 shows the top design schematic of the project illustrating this implementation. The project *B_AntiParallelDiodes_Kit025* provided with the application note implements the topology given in Figure 13.

Figure 13. Antiparallel Diode Topology for PSoC 3 and PSoC 5LP

Functionality

To measure the temperature of transistor diode Q1, the IDAC output is connected to Pin_Ic1. Pin_Ic2, which is configured in the open-drain drive mode, is driven low by writing a '0' to its data register. This establishes a current flow path through the transistor Q1. The ADC is then used to measure the V_{be} voltage across Q1 to calculate its temperature. During the time Q1 is on, transistor Q2 is off, as its base-emitter junction is reverse biased. After calculating the temperature of Q1, Pin_Ic2 is driven high by writing a '1' to its data register. This cuts off the current flow path through Q1 when not doing the measurement.

To measure the temperature of transistor diode Q2, the IDAC output is connected to Pin_Ic2. Pin_Ic1, which is configured in the open-drain drive mode, is driven low by writing a '0' to its data register. This establishes a current flow path through the transistor Q2. The ADC is then used to measure the V_{be} voltage across Q2 to calculate its temperature. During the time Q2 is on, transistor Q1 is off, as its base-emitter junction is reverse biased. After calculating the temperature of Q2, Pin_Ic1 is driven high by writing a '1' to its data register. This cuts off the current flow path through Q2 when not doing the measurement.

In Figure 13, two extra pins (Pin_Ircal, Pin_Vrcal2) are used for IDAC calibration. In the end application, these two pins can be saved by moving the calibration resistor in series between the pins Pin_Ic1 and Pin_Vb1e2. This is not done in the antiparallel diode project because the CY8CKIT-025 used for demonstrating this project also uses these calibration resistors for other temperature sensors like RTD. So the resistor is not connected in series with the diodes.
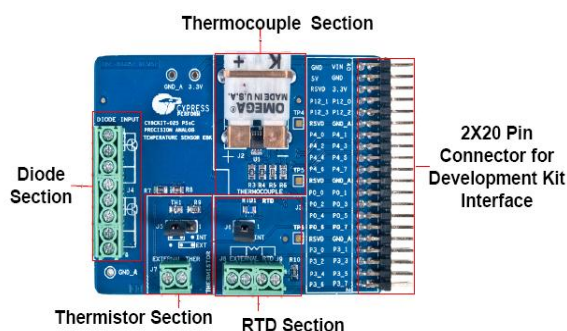
In Figure 13, different sets of pins are used for voltage sensing (Pin_Vb1e2, Pin_Ve1b2) and current carrying paths (Pin_Ic1, Pin_Ic2). This is essentially a four-wire sensing topology, which ensures that any voltage drop across long PCB traces in a remote diode-sensing application does not affect the temperature measurement. See the application note "AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations" for details on PCB layout considerations to be followed in precision analog sensing applications.

CY8CKIT-025 Temperature Sensor EBK

The CY8CKIT-025 PSoC Precision Analog Temperature Sensor Expansion Board Kit (EBK) is used for one of the three code examples provided in the Project Summary section.
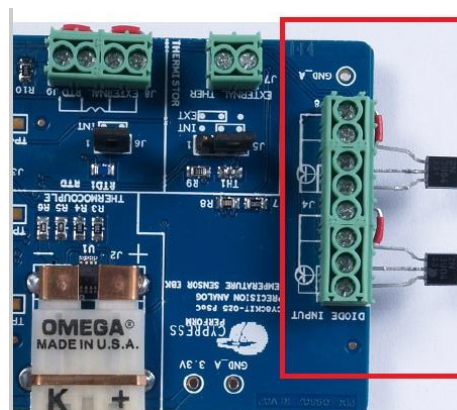
This kit, shown in Figure 14, provides four temperature sensors: thermocouple, thermistor, RTD, and diode. In addition, interface slots let you plug in your own thermocouple, thermistor, RTD, and diode. You can connect the EBK to the development kits available for PSoC 3 and PSoC 5LP.

Figure 14. Precision Analog Temperature Sensor EBK

CY8CKIT-025 comes with two 2N3904 NPN transistor diodes connected in antiparallel fashion, as shown in Figure 15. For more details about the transistor hardware connections, refer to the kit user guide.
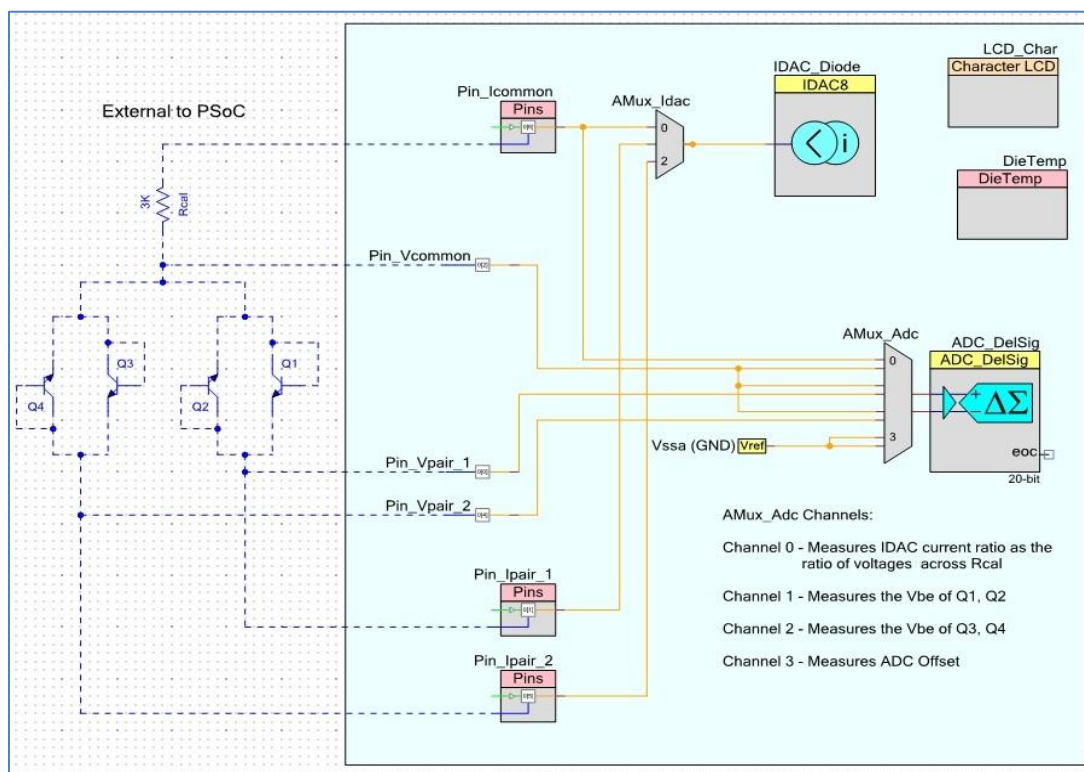
Figure 15. 2N3904 Transistors in CY8CKIT-025

Multiple Antiparallel Diode Topology Using PSoC 3 and PSoC 5LP

The antiparallel diode topology for two diodes can be extended further to measure the temperature of the multiple antiparallel diodes configuration. You can use this to do a low-cost temperature sensing solution of multiple thermal zones in an application using a single PSoC 3 and PSoC 5LP. Figure 16 gives the schematic for measuring the temperature of four diodes (two pairs).

Figure 16. Multiple Antiparallel Diode Topology Using PSoC 3 and PSoC 5LP

In Figure 16, Q1, Q2 transistors form one antiparallel diode pair, and Q3, Q4 form the other pair. The number of pins required in a multiple antiparallel diode topology can be further reduced by sharing one set of current sourcing (Pin_Icommon) and voltage sensing (Pin_Vcommon) pins for all of the diodes, as shown in Figure 16. Note that the other set of current sourcing and voltage sensing pins cannot be shared across multiple diode pairs, since it will lead to the temperature measurement of a diode getting influenced by the other diodes. The project *C_MultipleParallelDiodes* provided with the application note implements the topology given in Figure 16. This project can be easily modified to support more than two diode pairs. This implementation requires (2N + 2) pins for measuring the temperature of N diode pairs or 2N diodes.

Multiple-Diode Sensing Using PSoC 4

The single-diode sensing method can be extended to measure the multiple diodes. You can use this to do a low-cost temperature sensing solution of multiple thermal zones in an application using a single PSoC 4. Antiparallel topology is not used here because the temperature sensing method for PSoC 4 is different from that of PSoC 3 and PSoC 5LP, making antiparallel topology not suitable for PSoC 4. Figure 17 gives the schematic for measuring the temperature of two diodes. More than two diodes can use the same method.

Four-wire sensing is an electrical measuring technique that uses separate pairs of current-carrying and voltage-sensing electrodes to make more accurate measurements than traditional 2-wire sensing. For multiple-diode sensing, the IDAC current flows through AMux_EXT, which is the main difference from single-diode sensing. You cannot add another analog multiplexer before opamp, for there are only two analog buses in PSoC 4; the analog multiplexer resource is limited.

As a result, PSoC 4 cannot do true 4-wire sensing. Fortunately, the internal parasitic resistance of the analog multiplexer can be calibrated in the firmware. Although the wire resistance cannot be calibrated, it is usually very small and ignorable if the diode is mounted on the PCB. The trace resistance can be calculated with the following formula:

$$R = \rho * \frac{L}{T * W}$$

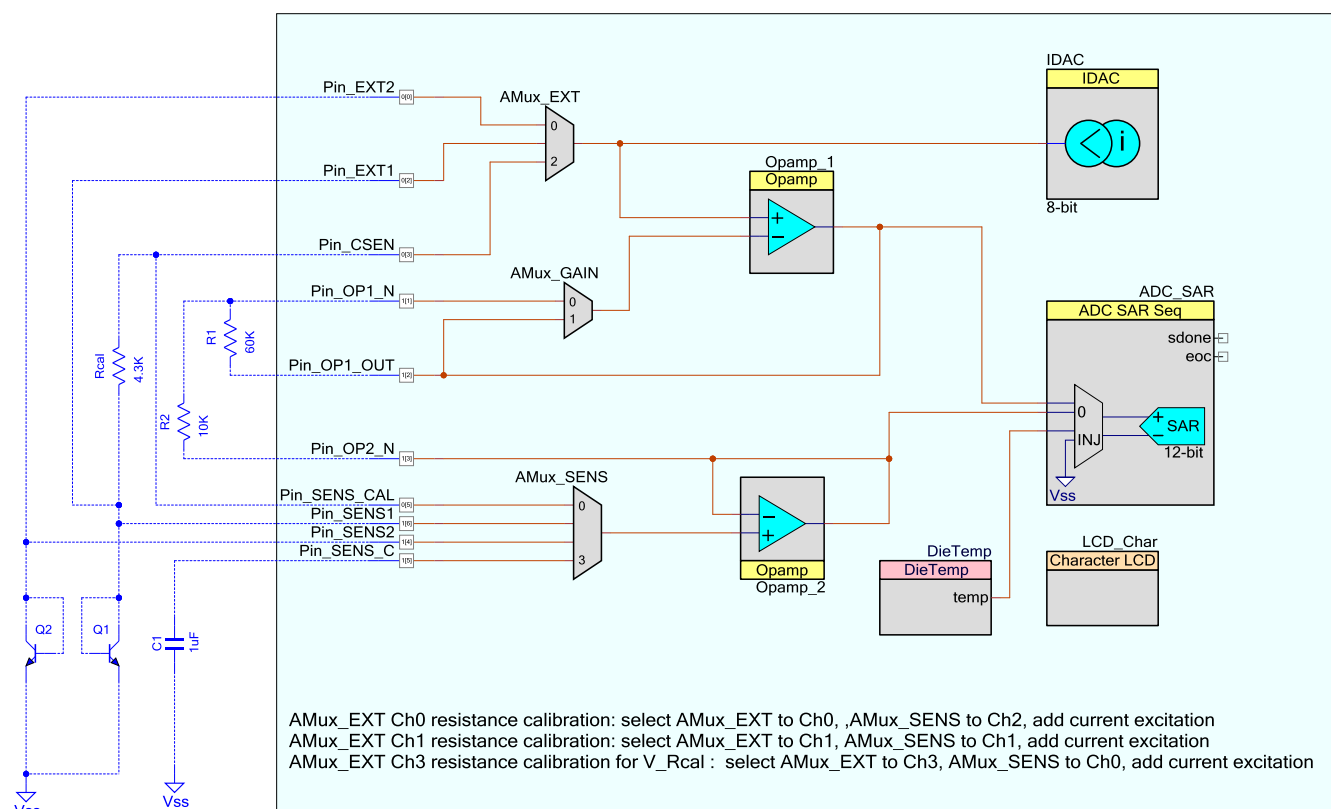ρ: $resistivity$

L: $trace\ length$

W: $trace\ width$

T: $trace\ height$

$resistivity\ of\ copper\ is\ 1.68 * 10^{-8}\ ohm * m$

For example, one trace with 35-μm thickness (1 oz/ft^2), 10-mm trace width, and 1-cm trace length has about 0.0191-Ω resistance.

The ΔV_{be} at a different current changes about 0.25 mV for every 1 °C increase in temperature. A 1-Ω wire resistance introduces about a 0.216-mV error when measuring the V_{be} voltage, which will introduce about a 0.86 °C error. It is recommended that the PCB trace resistance be less than 0.1 Ω. Based on the previous calculation, you can see that the PCB trace resistance is usually small enough. If the trace is long (>5 cm), use of a thicker trace is recommended to minimize the temperature error. If the diode is used over the connector, the wire resistance should be well considered to guarantee the system performance.

Figure 17. Multiple-Diode Sensing Using PSoC 4

The temperature measurement method is similar to that of the single diodes. The only difference is that it requires parasitic resistance calibration for AMux_EXT, according to the following method:
AMux_EXT Ch0 resistance introduces an offset error when measuring the ΔV_{be} of Q2, which can be measured by selecting AMux_EXT to Ch0, AMux_SENS to Ch2. This offset should be measured twice under low current and high current, respectively. The AMux_GAIN should be set to high gain, which is the same as measuring the ΔV_{be} of Q2.

AMux_EXT Ch2 resistance introduces an offset error when measuring the ΔV_{be} of Q1, which can be measured by selecting AMux_EXT to Ch1, AMux_SENS to Ch1. This offset should be measured twice under low current and high current, respectively. The AMux_GAIN should be set to high gain, which is the same as measuring the ΔV_{be} of Q1.

AMux_EXT Ch2 resistance introduces an offset error during the current ratio calibration process, which can be measured by selecting AMux_EXT to Ch3, AMux_SENS to Ch0. Pin_SENSC_CAL is an extra pin added for this

calibration. This offset should be measured twice: at low current and AMux_GAIN set to high gain; at high current and AMux_GAIN set to low gain, which is the same as for current ratio calibration.

Another difference from single-diode sensing is the gain reduction; the reason is to avoid ADC saturation. Using 170 Ω as the typical parasitic resistance for analog multiplex, the offset can be as high as 36.7 mV at high current (216 µA). The maximum ΔV_{be} at 125 °C is 99.5 mV. As in the Selection of Opamp External Resistors section, the maximum value for R1/R2 is 9. So the maximum R1/R2 for multiple-diode sensing can be derived as:

$$(R1/R2)_{max} = \frac{100mV * 9}{136mV} = 6.6$$

In the schematic, 60K and 10K are used because the matched pair resistor is used. See the Selection of Opamp External Resistors section to learn the reason for using the matched pair resistor.

The project *P4_MultiDiodes* provided with the application note implements the method given in Figure 17. You can easily modify this project to support more than two diodes. This implementation requires (2N + 6) pins for measuring the temperature of N diodes.

Design Considerations for PSoC 3 and PSoC 5LP

This section explains the various design considerations for accurate temperature measurement using a transistor diode.

Transistor Selection

The selection of the right transistor is very important for accurate temperature measurement. The CY8CKIT-025 uses the 2N3904 NPN transistor, which is the most commonly used transistor for temperature measurement. The following factors should be considered when choosing a transistor for temperature measurement.

Ideality Factor

The ideality factor (η) of the transistor is involved in temperature measurement as shown in Equations 5 and 6 on page 3. The datasheets of the general-purpose transistors do not provide an ideality factor value. But a correct measurement of the ideality factor is required for accurate temperature measurement. For the 2N3904 transistors, an ideality factor of 1.004 gave accurate results during testing. For other general-purpose transistors, the procedure to calculate the ideality factor is as follows:

1. Assuming an ideality factor $\eta_{assumed}$ (for example, 1.004), measure the diode temperature ($T_{measured}$ in Kelvin) using PSoC.

2. Measure the ambient temperature 'T_{ideal}' (in Kelvin) using an accurate temperature measurement source.

Using the assumed ideality factor($\eta_{assumed}$) and the two temperature parameters ($T_{measured}$, T_{ideal}), the correct ideality factor can be calculated as given by the following equation.

$$Ideality\ Factor,\ \eta_{correct} = \frac{T_{measured}}{T_{ideal}} * \eta_{assumed} \quad \text{Equation 8}$$

It is recommended to perform this test on multiple samples from the same transistor vendor and to compute the average of ideality factors to ensure accuracy of this parameter.

Transistor DC Forward Current Gain

The transistor diode equations used for temperature measurement are based on the assumption that the ratio of the bias currents sourced by the IDAC (emitter current for the transistor) is equal to the ratio of the corresponding collector currents. This is a valid assumption for transistors like 2N3904 that have a constant DC forward current gain (h_{FE}) over the entire bias current operating range (10 µA – 200 µA). If any other transistor is used, you must ensure that the parameter h_{FE} is constant over the bias current range. This can be found by looking at the graph showing the "h_{FE} Vs I_C" variation in the transistor datasheet.

Selection of the IDAC Calibration Resistor

An external resistor (R_{cal}) in series with the diode is used for calibrating the IDAC so as to calculate the IDAC current ratio accurately. This resistor need not be accurate, as the absolute value of the resistance does not matter when taking the ratio of the voltages.

From Equation 5,

Current ratio, N = I_2/I_1 = (V_2 * R_{cal})/(V_1 * R_{cal}) = V_2/V_1

There is a maximum limit on the value of the calibration resistor that can be used. Two factors determine the maximum value of the resistance: IDAC compliance voltage and ADC positive voltage range.

PSoC 3 and PSoC 5LP IDAC compliance voltage is (V_{DDA} − 1). V_{DDA} is the analog supply voltage to PSoC 3 and PSoC 5LP. Add an extra 1 V on top of the IDAC compliance voltage for the worst-case diode voltage drop while calculating the maximum resistance R_a as given in Equation 9.

$$R_a = (V_{dda} - 2)/I_{max} \quad \text{Equation 9}$$

I_{max} is the maximum current output of the IDAC used for transistor biasing, which in this application is 200 µA. For example, V_{DDA} = 3.3 V, I_{max} = 200 µA results in an R_a of 6.5 kΩ.

The maximum positive voltage that can be measured by the ADC also determines the maximum resistance R2 as given in Equation 10.

R2 = (ADC_POSITIVE_VOLTAGE_RANGE) / I_{max}
Equation 10

For the ADC in the ±1.024-V range, positive voltage range is 1.024 V. With I_{max} set at 200 µA, R2 is 5.1 kΩ.

The maximum value of the calibration resistor that can be used is governed by the following relation:

$$R_{cal} < (Minimum\ \{R1, R2\}) - R_{routing} \qquad \text{Equation 11}$$

In Equation 11, R1 and R2 are the resistances calculated as given in Equations 9 and 10. $R_{routing}$ is the internal analog routing resistance of PSoC 3 and PSoC 5LP. This routing resistance is dependent on the analog routing connections in the project. You can find more details on the analog routing resistances in the application note AN58827 – PSoC 3 and PSoC 5 Internal Analog Routing Considerations. A worst-case value of 2.2 kΩ can be assumed for $R_{routing}$ based on the value given in the datasheet. For a V_{dda} of 3.3 V or more, where the ADC range is the limiting factor on R_{cal}, it is recommended to use a 3-kΩ calibration resistor. This ensures that the current ratio can be accurately calculated even when using the lower priced families of PSoC 3 and PSoC 5LP devices, which have only a 12-bit ADC.

Design Considerations for PSoC 4

This section explains the various design considerations for accurate temperature measurement using a transistor diode.

The transistor selection part is the same as for PSoC 3 and PSoC 5LP.

Selection of the IDAC Calibration Resistor

An external resistor (R_{cal}) in series with the diode is used for calibrating the IDAC so as to calculate the IDAC current ratio accurately. This resistor need not be accurate, as the absolute value of the resistance does not matter when taking the ratio of the voltages.

From Equation 5,

Current ratio, $N = I_2/I_1 = (V_2 * R_{cal})/(V_1 * R_{cal}) = V_2/V_1$

There is a maximum limit on the value of the calibration resistor that can be used. The maximum value of the resistance is determined by three factors: IDAC compliance voltage, opamp output voltage range, and ADC positive voltage range.

PSoC 4 IDAC compliance voltage is (V_{DDA} + 0.5). V_{DDA} is the analog supply voltage to PSoC 4. Add an extra 1 V on top of the IDAC compliance voltage for the worst-case diode voltage drop while calculating the maximum resistance R_a as given in Equation 12.

$$R_a = (V_{DDA} - 0.5)/I_{max} \qquad \text{Equation 12}$$

I_{max} is the maximum current output of IDAC used for transistor biasing. For example, V_{DD} = 3.3 V, I_{max} = 216 µA results in an R_a of 12.9 kΩ.

The maximum output voltage for opamp is (V_{DDA} – 0.2). Assuming the diode voltage drop is 1 V, it determines the maximum resistance R_b as follows.

As Figure 7 shows, R1, R2 is the external resistors of the two opamps. V_{1-}, V_{2-} refers to the negative input voltage of opamp1 and opamp 2, respectively.

At low current, the differential opamp gain is set to high: $1 + R1/R2$.

$V_{1-} = 1 + R_{cal}* I_{min}$

$V_{2-} = 1$

$V_{output\ 1} = V_{1-} + (R1/R2)*(V_{1-} - V_{2-})$

$V_{output\ 2} = V_{2-} = 1$

So, $V_{output\ 1} = (1 + R1/R2)*R_{cal}* I_{min} + 1$ \qquad Equation 13

At high current, the differential opamp gain is set to low: 1.

$V_{1-} = 1 + R_{cal}* I_{max}$

$V_{2-} = 1$

$V_{output\ 1} = V_{1-} + (V_{1-} - V_{2-})$

$V_{output\ 2} = V_{2-} = 1$

So, $V_{output\ 1} = 2*R_{cal}* I_{max} +1$ \qquad Equation 14

V_{output} 1 at high current is the worst case. For high current, the gain is set to 1. For example, V_{DD} = 3.3 V, I_{max} = 216 µA results in an R_b of 4.8 kΩ using Equations 13 and 14.

The maximum positive voltage that can be measured by the ADC also determines the maximum resistance R_C as given by Equation 15.

$R_C = (ADC\_POSITIVE\_VOLTAGE\_RANGE) / I_{max}$
Equation 15

For the ADC in the ±1.024-V range, positive voltage range is 1.024 V. With I_{max} set at 216 µA, R_c is 4.7 kΩ.

The maximum value of the calibration resistor that can be used is governed by the following relation:

$$R_{cal} < (Minimum\ \{R_a, R_b, R_c\}) - R_{routing} \qquad \text{Equation 16}$$

In Equation 16, R_a and R_b are the resistances calculated as given in Equations 12 and 14. $R_{routing}$ is the internal analog routing resistance of PSoC 4. This routing resistance is dependent on the analog routing connections in the project. The typical value should be smaller than 200 Ω. In the project *P4_SingleDiode*, use a 4.3-kΩ calibration resistor.

Selection of Opamp External Resistors

The different amplifier is made from the two opamps in PSoC 4, which is used to amplify the ΔV_{be} and voltage across the calibration resistor (V_{Ral}). R1, R2 sets up the gain of the differential amplifier. Also set the common mode voltage on the output of each opamp. It should meet two conditions:

1. The differential output should be less than the SAR ADC reference voltage: 1.024 V.

2. The common mode voltage on the opamp's output should be within (0, V_{dda} – 0.2 V).

Gain = 1 + R1/R2, ΔV_{be_max} = 100 mV at 125 °C

R1/R2_max = 9 according to condition 1.

When measuring the ΔV_{be}, if the gain = 10, the voltage stored in the capacitor is about 0.6 V, and the V_{be} is about 0.7 V. The output on opamp1 is about 1.7 V, and the output on opamp 2 is 0.6 V, both with the common voltage range.

So R1/R2_max = 9, according to conditions 1 and 2.

When measuring V_{Ral}, the IDAC calibration resistor can guarantee the common voltage within the range based on the previous analysis.

R1, R2 accuracy, especially the tracking accuracy (R1/R2 accuracy), is critical to ensure the system performance. To guarantee about 5 °C temperature accuracy, 0.1 percent tracking accuracy is needed. A discrete 0.1 percent tolerance resistor can be expensive. Thus, it is recommended to use the matched pair resistor: R1/2 = 9, ratio tolerance: 0.1 percent. To reduce the AMux_GAIN parasitic resistance effect, a 10-kΩ and 90-kΩ pair is better than a 1-kΩ and 9-kΩ pair. The SOT23 surface mount voltage divider could be an option.

For multiple-diode sensing, the R1/R2 should be reduced to 6 to avoid ADC saturation, because the AMux_EXT introduces offset voltage. For detailed information, please refer to the Multiple-Diode Sensing Using PSoC 4 section.

Performance Measures for PSoC 3 and PSoC 5LP

This section discusses the different factors that affect the accuracy of the diode temperature measurement using PSoC 3 and PSoC 5LP. This includes the error caused by the PSoC components in the design (ADC, IDAC) and also the external transistor diode. The analysis in this section is based on the following equation:

$$T\ (in\ Kelvin) = (V_2 - V_1) * \frac{q}{\ln(N)*k*\eta} \qquad \text{Equation 17}$$

Ideality Factor of the Transistor Diode

The following equation gives the error due to the ideality factor:

$$\Delta T = T_{ideal} - T_{measured}$$

$$\Delta T = T_{ideal} * (1 - \eta_{correct}/\eta_{assumed}) \qquad \text{Equation 18}$$

T_{ideal} is the expected temperature in Kelvin for correct ideality factor $\eta_{correct}$, and $T_{measured}$ is the measured temperature in Kelvin for assumed ideality factor $\eta_{assumed}$. It can be inferred from Equation 18 that the error due to wrong ideality factor increases with increasing temperature. A 0.1 percent error in ideality factor ($\eta_{assumed} = 1.001 * \eta_{correct}$) would cause a measurement error of 0.36 °C at a temperature of 85 °C.

IDAC Current Ratio

The current ratio 'N' is calculated using an external resistor and the internal ADC in PSoC. So, if there is any variation in the output current due to IDAC offset, the INL gets canceled out to the resolution extent permitted by the resistor and the ADC. For example, a 3-kΩ calibration resistor used with a 12-bit ADC can measure current changes to the resolution of 0.17 µA (500 µV / 3 kΩ = 0.17). Here, 500 µV is the resolution of the ADC in 12-bit mode.

The following equation gives the temperature measurement error due to the error in current ratio measurement:

$$\Delta T = T_{ideal} * (1 - (\ln(N_{ideal})/\ln(N_{measured}))) \qquad \text{Equation 19}$$

N_{ideal} is the current ratio for the actual IDAC currents and $N_{measured}$ is the current ratio measured by the external R_{cal} and ADC combination. Note that T_{ideal} should be in Kelvin in Equation 19. With the use of an external calibration resistor and ADC for IDAC current ratio calculation, the error in the calculated current ratio will be due to the ADC measurement error – specifically, the error caused due to the ADC INL. ADC measurement error is discussed in the next section.

ADC Error

The ADC has three sources of error: offset error, gain error, and ADC nonlinearity. From Equation 5, the offset error is canceled by taking the difference of two voltages, V1 and V2.

Gain Error

PSoC 3 and PSoC 5LP Delta Sigma ADC is factory calibrated for a gain error of ±0.2 percent in a subset of ADC configurations, which includes the ±1.024-V configuration used in this implementation. This 0.2 percent gain error also includes the ADC reference error. The 0.2 percent ADC gain error results in a 0.2 percent error in the corresponding temperature. The generic equation given in Equation 20 is for a gain error of k, where the temperature T_{ideal} should be in Kelvin for the error calculation.

$$\Delta T = T_{ideal} - T_{measured} = T_{ideal} * k \qquad \text{Equation 20}$$

The error due to 0.2 percent gain error at 85 °C is 0.72 °C.

If the ambient temperature (temperature of the PSoC device) is different from 25 °C, ADC gain drift causes additional error. The Delta Sigma ADC has a gain drift of 50 ppm/°C. It would be 3,000 ppm or 0.3 percent for an ambient temperature of 85 °C. This causes an error of 1.1 °C based on Equation 17. But if the diode is at a remote location compared to PSoC, then PSoC can be at a lower temperature compared to the diode, in which case the error due to gain drift is less.

ADC INL

The INL of an ADC at any point is the difference between the ideal ADC count and the actual ADC count at that point after gain and offset corrections have been done. The datasheet specifies the maximum INL of all points across process, voltage, and temperature (PVT). The PSoC 3 and PSoC 5LP Delta Sigma ADC has an INL of ±32 least significant bits (LSb) in ±1.024-V mode; 32 LSb corresponds to 62.5 µV for a 20-bit resolution and ±1.024-V range.

Note that the INL error not only affects the measurement of (V2-V1), but also introduces an error in the current ratio measurement because the current ratio is calculated based on the voltage measured by the ADC across Rcal. The maximum positive worst-case error occurs when ADC measurements are affected by INL as described below:

- V2 measured by the ADC is equal to the actual V2 + INL error
- V1 measured by the ADC is equal to the actual V2 – INL error
- The voltage across Rcal when I2 is sourced as measured by the ADC is equal to the actual voltage – INL error
- The voltage across Rcal when I1 is sourced as measured by the ADC is equal to the actual voltage + INL error

Again, note that it is very rare for all these conditions to happen together. Nonetheless, the worst-case error occurs when these do happen together. The Microsoft Excel workbook attached with this application note can be used to estimate this worst-case error.

In the 20-bit mode, considering an ADC INL of ±32 LSB, the error is ±0.75 °C. In the 12-bit mode, the ADC has an INL of ±1 LSB; this corresponds to a temperature error of ±6 °C.

Note that these are worst-case errors, using the worst-case INL across PVT and using it for error calculation. This pessimistic approach indicates the worst-case limits due to INL. In practice, the error due to INL will be much lower.

Summary of Error Sources

Table 3 gives the temperature error due to the various error sources at a measurement temperature of 85 °C. In the table, all error sources except the ideality factor are due to the PSoC signal chain. The errors due to the PSoC signal chain are for worst-case conditions. The Temperature Test section gives the practically observed result of the temperature measurement for the different ADC configurations.

Note that the final error cannot be considered as a summation of all errors; this is because all the errors are correlated. The Microsoft Excel workbook attached with this application note can be used to estimate the combined worst-case error.

Table 3. Temperature Measurement Error Sources

Error Source	Error in 20-Bit ADC Mode	Error in 12-Bit ADC Mode	Comments
ADC Gain Error	±0.72 °C	±0.72 °C	
ADC Gain Drift	±1.1 °C	±1.1 °C	Worst-case error at 85 °C assuming diode and PSoC are in the same thermal zone. This error will be lower for remote diodes.
ADC INL	±0.75 °C	±6 °C	Assuming the worst-case INL specifications for the ADC. Typical value will be much lower.
Ideality Factor (Special)	±0.36 °C	±0.36 °C	For a 0.1 % error in ideality factor at 85 °C. This error is due to the transistor itself and not the PSoC signal chain.

Temperature Test

The temperature measurement accuracy of the different ADC configurations was practically tested in the lab using a Temptronic temperature forcing system and sweeping the temperature of the enclosed chamber from 0 to 100 °C. A MicroTherma measurement device with a thermocouple sensor, placed in the same chamber as the transistor diode, was used as a temperature reference. The results for the different configurations are given in Table 4 and Table 5. Since the resolution in the 12-bit mode was >1 °C, a minimum-maximum routine was implemented to display the maximum and minimum temperatures measured by PSoC for a fixed temperature. This was used in calculating the temperature measurement accuracy given in the following tables.

Table 4. Temperature Results in 12-Bit ADC Mode

Reference T (°C)	Diode Min T (°C)	Diode Max T (°C)	Min Diff (°C)	Max Diff (°C)
10.8	11	13	0.2	2.2
19.4	19.1	21.3	–0.3	1.9
27.2	27.3	28.8	0.1	1.6
35.6	35.5	37.7	–0.1	2.1
47.1	46.3	48.6	–0.8	1.5
57.4	57.2	59.1	–0.2	1.7
65.4	65.1	67	–0.3	1.6
75.5	74.9	76.8	–0.6	1.3
85.6	85.1	87.2	–0.5	1.6
96.6	96	98	–0.6	1.4

Table 5. Temperature Results in 20-Bit ADC Mode

Reference T (°C)	Diode T (°C)	Difference (°C)
8.8	9.1	0.3
18.2	18.5	0.3
28	27.9	–0.1
37.1	37	–0.1
46.3	46.2	–0.1
60.8	60.6	–0.2
69.3	69.2	–0.1
77.3	77.2	–0.1
87.5	87.6	0.1
94.5	94.7	0.2

Performance Measures for PSoC 4

This section discusses the different factors that affect the accuracy of the diode temperature measurement using PSoC 4. This includes the error caused by the PSoC components in the design (ADC, IDAC), the external resistors of the opamps, and the external transistor diode. The analysis in this section is based on the following equation:

$$T \ (in \ Kelvin) = (V_2 - V_1) * \frac{q}{\ln(N) * k * \eta}$$ Equation 21

Ideality Factor of the Transistor Diode

The analysis is the same as for PSoC 3 and PSoC 5LP; see the Ideality Factor section for detailed information. Generally, a 0.1 percent error in ideality factor would cause a measurement error of 0.37 °C or 0.37 K at a temperature of 373 K (100 °C), about 0.4°C at 125 °C.

IDAC Current Ratio

The final temperature measurement accuracy is highly dependent on the excitation current ratio I2/I1. So you need to calibrate the IDAC output current before actual measurement. The basic theory is to measure the voltage drop on Rcal at I1 and I2 and use the actual N = I2/I1 temperature calculation in Equation 21.

The error is mainly due to the ADC INL and the opamp gain used at low current.

Error due to INL:

Rcal = 4.3 kΩ

At I1 = 10.8 μA, use the opamps to gain up the V_{Rcal} from 46 mV to 460 mV.

At I2 = 216 μA, no gain, V_{Rcal} = 928mV.

The 2-LSB INL of ADC, which means a maximum 1-mV voltage measurement error.

$$Error_{I1} = \frac{460 \ mV + 1 \ mV}{460 \ mV} - 1 = 0.2\%$$
$$Error_{I2} = \frac{928m \ V + 1 \ mV}{928m \ V} - 1 = 0.1\%$$

Then the total equivalent gain error caused by the ADC INL in excitation current ratio calibration is +/–0.3 percent.

Error due to the opamp gain: 0.1 percent

So, the I2/I1 total error is about 0.4 percent.

The gain error of ADC does not impact the current ratio calibration because it impacts both I1 and I2 measurement and will be canceled when you divide I1 by I2.

In this case, the final temperature error caused by current ratio calibration is:

$$Error_{Cal} = \frac{In20}{In(20 \times 1.004)} - 1 = 0.001 = 0.14\%$$

As discussed previously, a 0.1 percent error causes a 0.4 °C error, so the total I2/I1 causes a 0.5 °C temperature error using the current ratio calibration.

If you do not use the gain 10 amplifier with 1X current excitation, the 2-LSB INL will cause a 2 percent gain error in ratio calibration. That means about a 2.8 °C temperature error finally.

Opamp Error

When the differential amplifier is set to high gain, the gain is equal to (1 + R1/R2). The R1/R2 ratio tolerance impacts the gain error of the system; it acts as the ADC gain error.

Since the tolerance is small compared to the resistors' value, you can simplify the calculation and use the sum of two tolerances as the worst-case gain error. For example, if you use two 1 percent resistors, the gain error should be 2 percent.

So, if you use 1 percent accuracy resistors, that leads to an 8 °C temperature error at 125 °C, which is unacceptable. It is based on the assumption that the two resistors are totally independent. However, in practice, you can use a matched pair resistor, which includes two resistors in a single package (usually configured as a divider) and has a very good ratio tolerance. Absolute tolerance is not critical.

If you use a 0.1 percent ratio tolerance resistor divider/array, the final temperature error caused by gain stage is 0.4 °C.

The offset calibration process in firmware takes care of the opamp offset.

ADC Error

The ADC has three sources of error: offset error, gain error, and ADC nonlinearity. The offset calibration process in firmware takes care of the ADC offset.

Gain Error

The internal voltage reference is 1 percent, and the ADC gain error is 0.1 percent. Both are considered as the gain error. So, the temperature error caused by ADC in 125 °C is about 4.4 °C.

ADC INL

After the opamp amplification, the ADC INL is small enough to be ignored.

Summary of Error Sources

Table 6 gives the temperature error due to the various error sources. In the table, all error sources except the ideality factor are due to the PSoC signal chain. The errors due to the PSoC signal chain are for worst-case conditions. The Temperature Test section gives the practically observed result of the temperature measurement for the different ADC configurations.

Table 6. Temperature Measurement Error Sources

Error Source	Error at 25 °C	Error at 125 °C	Comments
IDAC Current Ratio	0.4 °C	0.5 °C	Use 10 x gain at low current. INL error calculation is the worst case; in practice, the error should be much smaller.
Opamp Error	0.3 °C	0.4 °C	Use 0.1% ratio tolerance resistor divider.
ADC Gain Error	3 °C	4.4 °C	Use internal ADC reference.
ADC Gain Drift	–	–	–
Ideality Factor (Special)	0.3 °C	0.4 °C	For a 0.1 % error in ideality factor at 100 °C. This error is due to the transistor itself, not to the PSoC signal chain.

Temperature Test

The temperature measurement accuracy of the different ADC configurations was practically tested in the lab using a Temptronic temperature forcing system and sweeping the temperature of the enclosed chamber from 0 to 100 °C. A MicroTherma measurement device with a thermocouple sensor placed in the same chamber as the transistor diode was used as a temperature reference. Table 7 shows the results for the different configurations. A minimum-maximum routine was implemented to display the maximum and minimum temperatures measured by PSoC for a fixed temperature. This was used in calculating the temperature measurement accuracy given in the following table.

Table 7. Temperature Results for PSoC 4

Reference T (°C)	Diode T (°C)	Difference (°C)
1.3	0	−1.3
9.9	8.4	−1.5
19.1	17.9	−1.2
28.5	27.1	−1.4
37.6	36.4	−1.2
47	45.8	−1.2
56.5	55.4	−1.1
67.4	66.2	−1.2
77.1	76	−1.1
86.7	85.6	−1.1
96.8	95.9	−0.9

Project Summary

The *AN60590.cywrk* workspace provided with the application note contains six code examples for diode temperature measurement as follows.

These three projects are applicable to PSoC 3 and PSoC 5LP.

- *A_SingleDiode:* This project implements a single diode temperature measurement according to the implementation shown in Figure 2. This implementation is recommended for customer end applications, but it does not work with the CY8CKIT-025, which does not have the calibration resistor in series with the diode.

- *B_AntiParallelDiodes_Kit025:* This project implements the antiparallel diode topology shown in Figure 13 and is designed to work with CY8CKIT-025.

- *C_MultipleParallelDiodes:* This project implements the multiple antiparallel diode topology shown in Figure 16. This project does not work with the CY8CKIT-025 since it supports only two diodes.

The following two projects are applicable to PSoC 4. For the analog routing resource difference, they do not work with the CY8CKIT-025.

- *P4_SingleDiode:* This project implements single-diode temperature measurement according to the implementation shown in Figure 7.

- *P4_MultiDiodes:* This project implements multiple-diode temperature measurement according to the implementation shown in Figure 17.

To include the *math.h* library for the PSoC 4 and PSoC 5LP GCC compiler, go to **Project** > **Build Settings** and in the ARM GCC – Linker – General tab, add the letter "m" in the Additional Libraries option. This configuration has already been done in the projects described in this application note.

Summary

This application note explained how the powerful analog architecture in PSoC 3, PSoC 4, and PSoC 5LP enables temperature measurement using general-purpose transistors. PSoC 3 and PSoC 5LP target the accurate diode temperature measurement field; PSoC 4 targets the medium accurate diode temperature measurement field.

PSoC 3, PSoC 4, and PSoC 5LP also have the capability to do multiple-diode temperature measurements using a minimum number of pins. PSoC 3, PSoC4, and PSoC 5LP are well suited to do the system management controller functions by performing control actions based on the temperature measured, enabling a true system-on-chip solution.

Related Application Notes

- AN75511 – PSoC 3/PSoC 5LP – Temperature Measurement with a Thermocouple

- AN66477 – PSoC 3 and PSoC 5LP – Temperature Measurement with a Thermistor

- AN70698 – PSoC 3 and PSoC 5LP – Temperature Measurement with an RTD

- AN58827 – PSoC 3 and PSoC 5LP Internal Analog Routing Considerations

- AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations

- AN58304 – PSoC 3 and PSoC 5 – Pin Selection for Analog Designs

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2900858	VVSK	03/29/2010	New Application Note.
*A	3156112	VVSK	01/31/2011	Updated project for FCS. Changed title to specify AN is for PSoC 3 / PSoC 5. Changed Associated Part Family to reflect new PSoC 5 part numbering. Minor text edits.
*B	3287533	VVSK	06/20/2011	Updated the Projects for CY8CKIT-025. Added new section on using Multiple transistor diodes.
*C	3442928	VVSK	11/19/2011	Project Updates for PSoC Creator 2.0. Updated template.
*D	3814122	VVSK	11/21/2012	Updated title to read "PSoC® 3 and PSoC 5LP - Temperature Measurement with a Diode – AN60590" Updated Associated Part Family as "All PSoC 3 and PSoC 5LP parts" Updated Software Version as "PSoC® Creator™ 2.1 SP1 or later" Updated Abstract Updated Introduction (Updated contents in the section, added Table 1) Updated The Diode Equation (Updated Measuring Diode Temperature (updated contents in the section), added Transistor as Diode) Updated Measuring Diode Temperature Using PSoC 3 and PSoC 5LP (Updated Functionality Updated Component Configuration (Updated Current DAC (IDAC) Configuration, updated ADC Configuration) Added Firmware Details Removed 4-Wire Measurement Technique Removed Choosing the Right Analog Pins Removed Diode Temperature Measurement Project Removed Transistor Selection Removed Selection of the IDAC Calibration Resistor Removed Error Budget Analysis Update with PSoC 4 contents Renamed CY8CKIT-025 for Diode Temperature Measurement‖ as CY8CKIT-025 Temperature Sensor and updated the contents in the same section. Added Multiple Antiparallel Diode Topology Added Design Considerations for PSoC 4 Added Performance Measures for PSoC 4 Updated Project Summary Replaced "PSoC 5" with "PSoC 5LP" in all instances across the document
*E	3991824	VVSK	05/06/2013	No technical updates. Completing Sunset Review
*F	4210595	JCHE	12/05/2013	Updated PSoC 4 contents about diode measuring
*G	4219451	JCHE	12/13/2013	Added the associated project files
*H	4678523	VVSK	03/05/2015	Updated the projects to PSoC Creator 3.1 CP1. Updated the "Performance Measures for PSoC 3, PSoC 5LP" section Provided an Excel sheet to calculate the performance Sunset review

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*I	5741525	AESATMP9	05/18/2017	Updated logo and copyright.

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